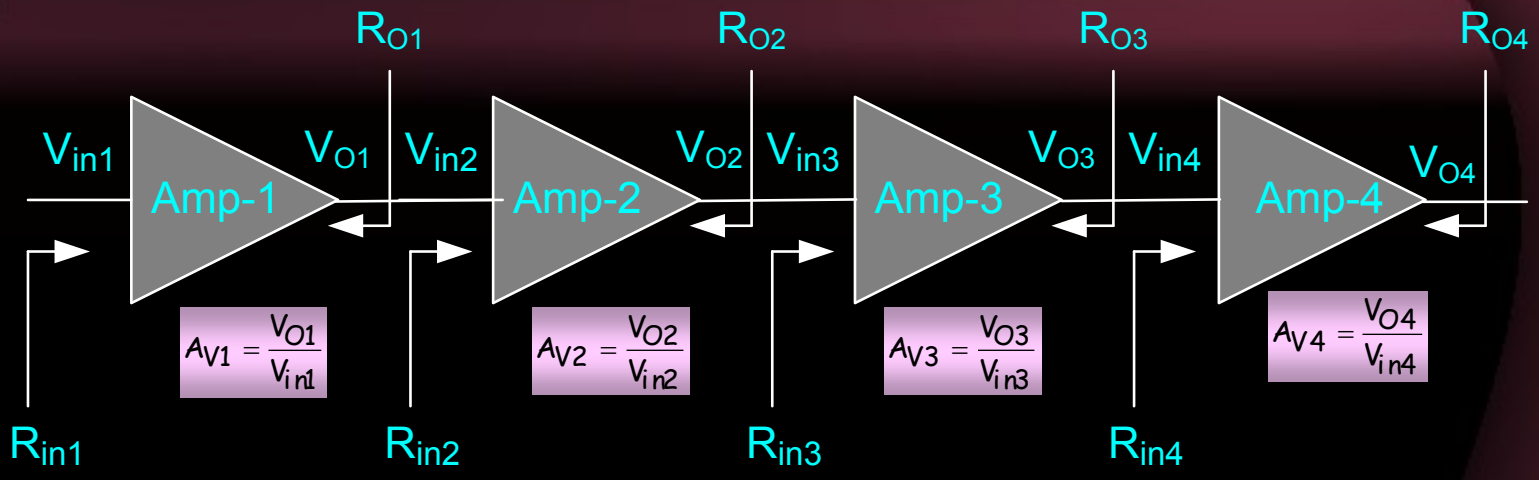
4. Design of Multistage Amplifiers

4.1 Multistage RC Coupled Amplifiers

4.2 FET-BJT 2-stage RC Coupled Amplifiers

4.3 FET-BJT 3-stage RC Coupled Amplifiers

4.1 Multistage RC Coupled Amplifiers



Cascaded Multistage Amplifiers

Note that in multistage amplifiers, (a) V_O of the preceding stage becomes V_{in} of the following stage, example $V_{O1} = V_{in2}$, (b) R_{in} of the following stage becomes R_L of the preceding stage, example $R_{L1} = R_{in2}$, (c) Overall gain is the product of gain of every stage. So the design depends upon the available data between stages. For example, without knowing R_{in2} of the second stage, design is not possible to meet the voltage gain of the first stage.

4.2 FET-BJT 2-stage RC Coupled Amplifiers

Design Example

Draw the circuit and design the following 2-stage RC coupled amplifier. First stage is a JFET self-bias CS amplifier circuit. Design the parameters of the JFET(I_{GSS}, I_{DSS} and V_P,) and V_{DD} for required R_G=20MΩ , A_v = -12 and R_D = R_{L1} = R_{in2} =2kΩ. Assume V_D=V_{DD}/2=10V

The above FET amplifier is RC coupled to a second stage (CE) amplifier circuit whose specifications are: β=200, V_{CC} = 10V, optimum output voltage design, R_C= R_L = 2kΩ, R_E = 0.4kΩ, Design bias resistances R_1 and R_2.

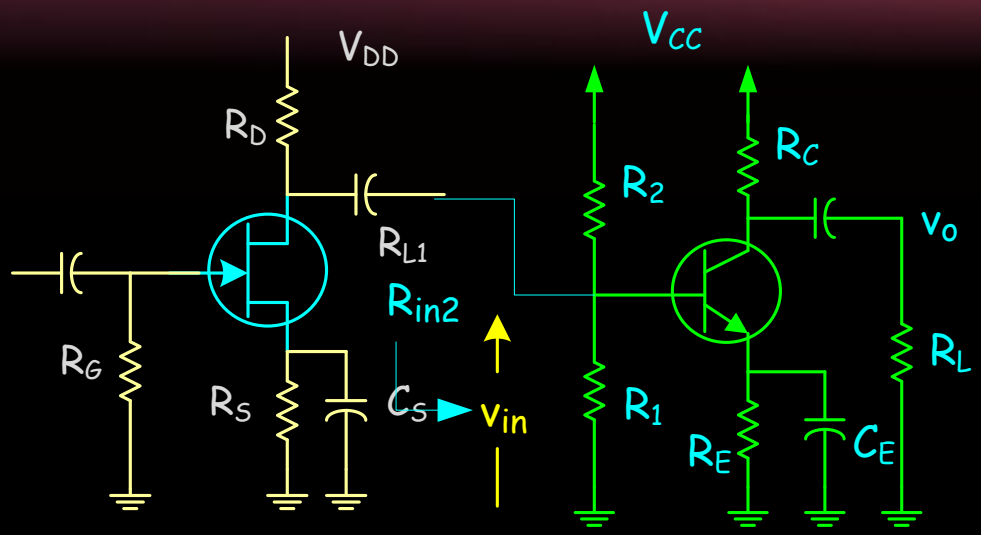
Overall performance

What is the total voltage gain from the input of the first stage to the output of the second stage?

Find undistorted output voltage swing at second stage output and

The possible maximum input voltage at the first stage.

Draw Circuit to be designed



Self Bias CS Amp.
R_G=20MΩ , A_v = -12 and R_D = R_{L1} = R_{in2} =2kΩ. Assume V_D=V_{DD}/2=10V

CE Amp. β=200, V_{CC}=10V, optimum output voltage design, R_C= R_L=2kΩ, R_E = 0.4kΩ

Because $R_{L1} = R_{in2} = 2k\Omega$ is available, design is possible for the first stage voltage gain and also design of R_{B2} of the second stage. Therefore the design can start with the first FET stage as follows;

Given; CS Amp. $R_G = 20M\Omega$, $A_v = -12$ and $R_D = R_{L1} = R_{in2} = 2k\Omega$. Assume $V_D = V_{DD}/2 = 10V$

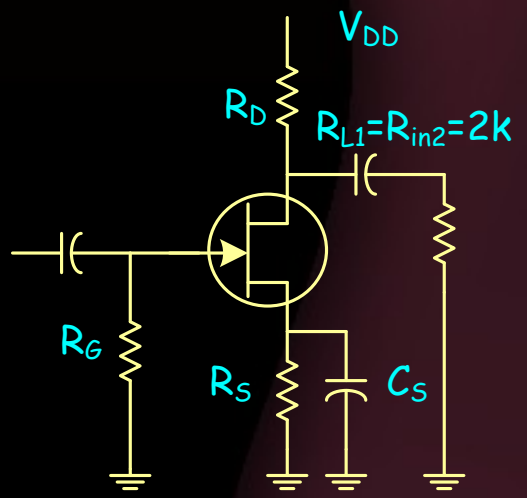
$$A_v = -g_m(R_D // R_L) = -12 \Rightarrow -g_m = \frac{-12}{2k // 2k} = 12mS$$

$$\text{Opt. } g_m = 12mS = 1.42\frac{I_{DSS}}{|V_P|} \Rightarrow (1)$$

$$\text{Opt. } V_{GS} = 0.3|V_P| = I_D R_S = \frac{I_{DSS}}{2} R_S \Rightarrow |V_P| = \frac{I_{DSS}}{0.6} R_S \Rightarrow (2)$$

Take V_P from (2) and put it in (1),

$$12 = 1.42\frac{I_{DSS}}{\frac{I_{DSS}}{0.6} R_S} = \frac{1.42 \times 0.6}{R_S} \Rightarrow R_S = \frac{1.42 \times 0.6}{12} k = \underline{\underline{0.071k}}$$



$$V_{DD} - I_D R_D = V_D = 10V = \frac{V_{DD}}{2} \Rightarrow V_{DD} = \underline{\underline{20V}} \therefore I_D = \frac{V_D}{R_D} = \frac{10}{2k} = 5mA \Rightarrow I_{DSS} = 2I_D = \underline{\underline{10mA}}$$

$$\therefore V_{GS} = 0.3V_P = -I_D R_S \Rightarrow V_P = \frac{-5mA \times 0.071k}{0.3} = -1.83V \approx \underline{\underline{-2V}}$$

$$R_G = 20M = \frac{0.1|V_P|}{I_{GSS}} \Rightarrow I_{GSS} = \frac{0.1|V_P|}{20M} = \frac{0.1 \times 2V}{20M} = \underline{\underline{10nA}}$$

Designed $R_S = 71\Omega$,

$V_{DD} = 20V, I_D = 5mA$

FET data $\Rightarrow I_{GSS} = 10nA$,

$I_{DSS} = 10mA, V_p = -2V$

Because R_{in2} =2kΩ is available, design is possible for the R_{B2} of the second stage.

Given; CE Amp. β=200, V_{CC}=10V, optimum output voltage design, R_C= R_L=2kΩ, R_E = 0.4kΩ

$$I_C = \frac{V_{CC}}{R_{ac}+R_{dc}} = \frac{10}{1k+2.4k} = 2.94mA$$

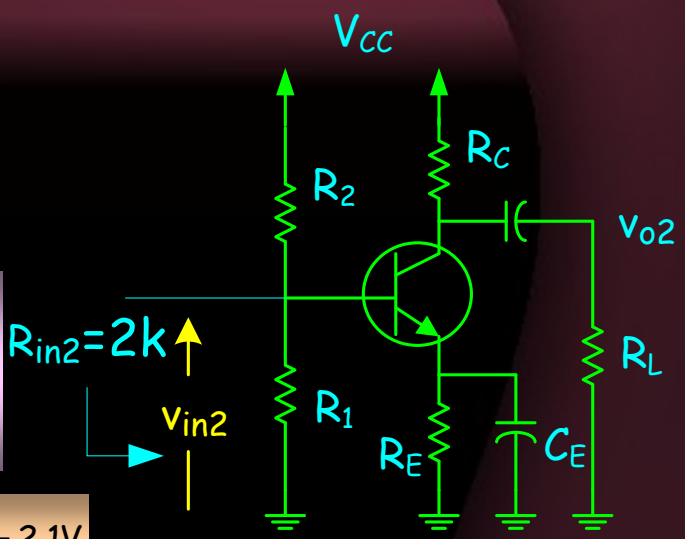
$$r_e = \frac{26}{I_C} = \frac{26}{2.94} = 8.84\Omega \Rightarrow \beta r_e = 200\times 8.84 = 1768\Omega$$

$$\therefore R_B // \beta r_e = R_B // 1768\Omega = R_{in2} = 2000\Omega \Rightarrow R_B = \frac{1768\times 1500}{2000-1768} = 15.24k$$

$$V_{BB} = I_B R_B + 0.7 + I_C R_E = I_C\left(R_E + {}^{R_B}\!/_{\beta}\right) + 0.7 = 2.94\left(0.4 + {}^{15.24}\!/_{200}\right) + 0.7 = 2.1V$$

$$R_1 = \frac{R_B}{1-\left({}^{V_{BB}}\!/_{V_{CC}}\right)} = \frac{15.24}{1-\left({}^{2.1}\!/_{10}\right)} = 19.29k$$

$$R_2 = R_B\frac{V_{CC}}{V_{BB}} = \frac{15.24\times 10}{2.1} = 72.57k$$



Designed R_1 = 19.25kΩ,
R_2 = 72.57kΩ
I_C = 2.94mA

Overall performance

What is the total voltage gain from the input of the first stage to the output of the second stage?

Find undistorted output voltage swing at second stage output and

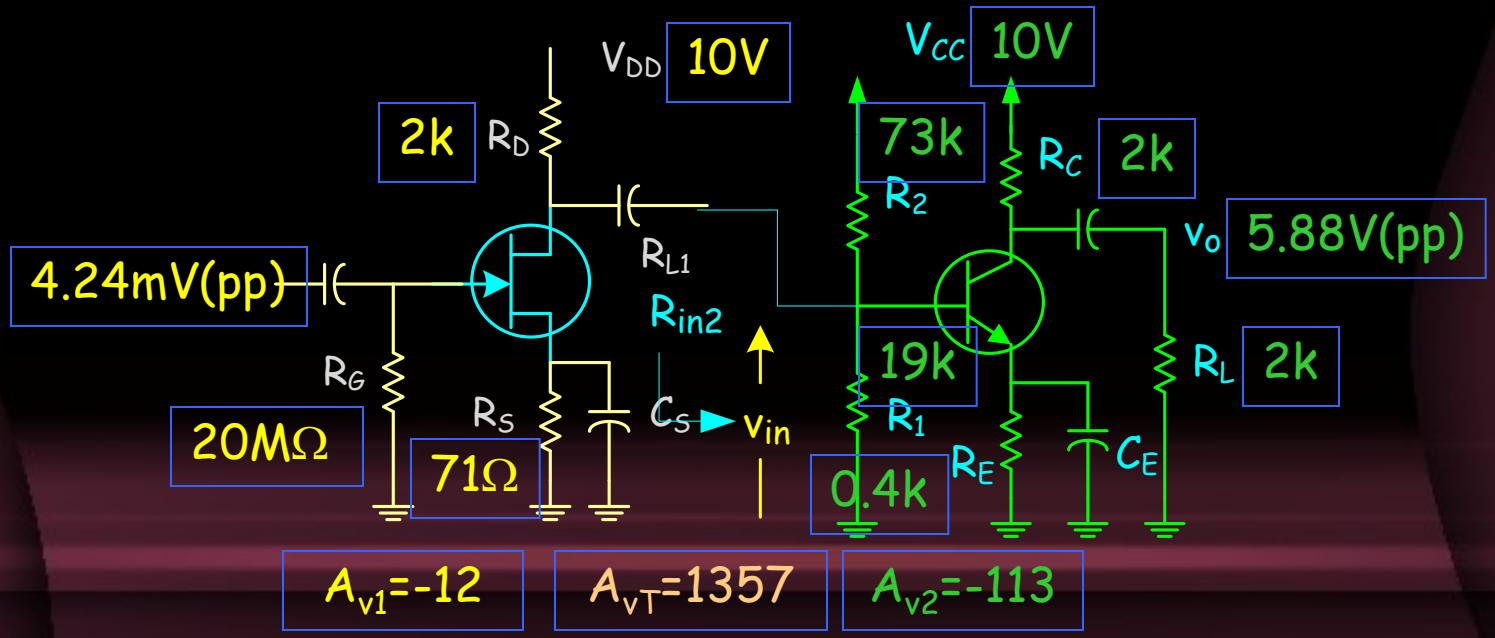
The possible maximum input voltage at the first stage.

$$A_{v2} = \frac{-R_C // R_L}{r_e} = \frac{-1000}{8.84} = -113.12$$

$$A_{v1} = -12 \Rightarrow \# A_{vT} = -12 \times (-113.12) = \underline{\underline{1357.44}}$$

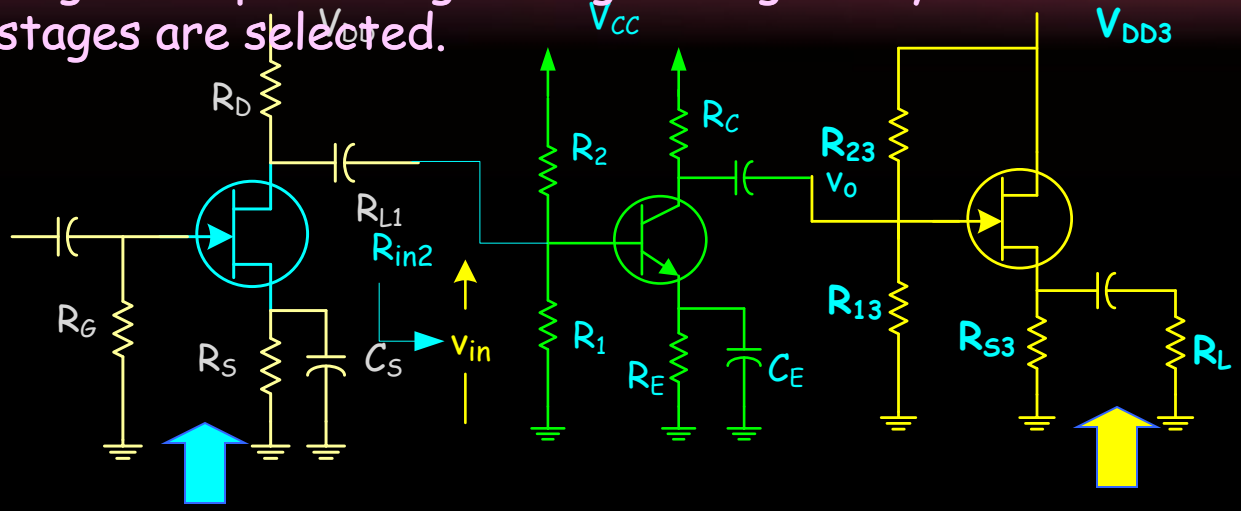
$$v_{o2}(pp) = 2I_{C2}R_{ac} = 2 \times 2.94mA \times 1k = 5.88V$$

$$\# \text{Maxmum } v_{in1}(pp) = \frac{V_{o2}(pp)}{A_{vT}} = \frac{5.8V}{1357.44} = 0.00424V = 4.24mV$$



4.3 FET-BJT-FET 3-stage- RC Coupled Amplifiers

To design an amplifier having (a) very high R_{in} & (b) very high voltage gain & (c) very large signal output voltage swing driving a very low load resistance, following stages are selected.

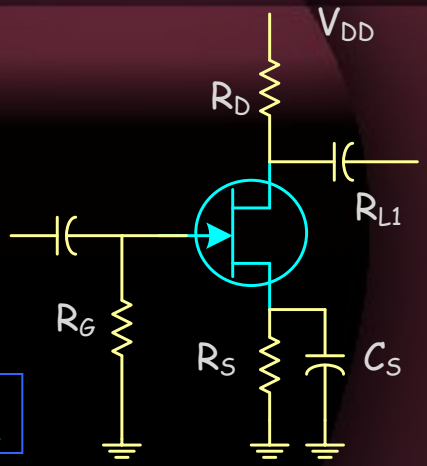


Self bias CS Amp. To provide very high R_{in} but small signal V_o since it is a preamplifier stage Take A_V = -12

CE Amp. For high A_v
Take R_C=2kΩ R_{in3} = 20kΩ
For maximum voltage transfer from 2nd stage to 3rd stage

SF Amp. To provide high R_{in3} and Voltage divider bias to provide large output voltage swing to drive R_{S3}= R_L = 1000Ω

Draw and Design R_G , R_S , $R_D = R_L$ and V_{DD} of the first stage JFET self-bias CS amplifier circuit. FET data is given as I_{GSS}=300nA, I_{DSS}=5mA and V_P=-3V, The required specification is $V_D=V_{DD}/2$ and A_v = -12



$$R_G = \frac{0.1V_P}{I_{GSS}} = \frac{0.3}{300nA} = \underline{\underline{1M\Omega}}$$ ← R_G

$$\text{Opt. } gm = 1.42\frac{I_{DSS}}{|V_P|} = 1.42\frac{5mA}{3} = 2.367(mA/V)$$

$$A_v = -g_m(R_D // R_L) = -12 \Rightarrow R_D = R_L = 2\frac{12}{2.367}k = \underline{\underline{10.13k\Omega}}$$ ← $R_D = R_L$

$$\text{Opt. } I_D = (I_{DSS}/2) = (5mA/2) = 2.5mA$$

$$\text{Opt. } V_{GS} = 0.3V_P = 0.3\times(-3) = -0.9V$$

$$\therefore V_{GS} = -0.9V = -I_D R_S \Rightarrow R_S = \frac{0.9}{2.5mA} = 0.36k = 360\Omega$$ ← R_S

$$V_{DD} - V_D = I_D R_D \Rightarrow \frac{V_{DD}}{2} = 2.5mA\times 10.13k$$

$$\therefore V_{DD} = \underline{\underline{50.65V}}$$ ← V_{DD}

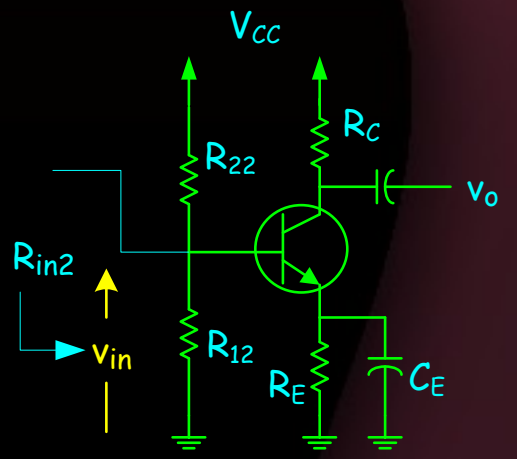
Draw and design second stage (CE) amplifier circuit
Given specifications are: $\beta = 200$, $V_{CC} = 10V$, $R_C = 2\ k\Omega$, $R_L = 20\ k\Omega$, $R_E = 0.4k\Omega$, $R_{in} = 10.3k\ \Omega$. Design bias resistances R_1 and R_2,
find voltage gain,and undistorted output voltage swing of this stage.

$$R_{ac} = R_C // R_{in3} = 2k // 20k = 1.8k$$
$$I_C = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{10}{1.8k + 2.4k} = 2.38mA$$

R_G

$$r_e = \frac{26}{I_C} = \frac{26}{2.38} = 10.92\Omega \Rightarrow \beta r_e = 200 \times 10.92 = 2.184k\Omega$$
$$\therefore R_B // \beta r_e = R_B // 2.184k\Omega = R_{in} = 10.3k\Omega \Rightarrow R_B = \frac{10.3 \times 2.184}{10.3 - 2.184} = 2.77k$$

$$V_{BB} = I_B R_B + 0.7 + I_C R_E = I_C\left(R_E + {}^{R_B}\!/_{\beta}\right) + 0.7$$
$$= 2.38\left(0.4 + {}^{2.77}\!/_{200}\right) + 0.7 = 1.68V$$



$$R_{12} = \frac{R_B}{1 - \left({}^{V_{BB}}\!/_{V_{CC}}\right)} = \frac{2.77k}{1 - \left({}^{1.68}\!/_{10}\right)} = 3.33k$$

$$R_{22} = R_B \frac{V_{CC}}{V_{BB}} = \frac{2.77k \times 10}{1.68} = 16.49k$$

R_{12} R_{22}

$$v_{o2}(pp) = 2 I_C R_{ac} = 2 \times 2.38mA \times 1.8k = 8.57V$$

V_{o2} (pp)

$$A_{v2} = \frac{-R_C // R_L}{r_e} = \frac{-1800}{10.92} = -164.8$$

A_{v2}

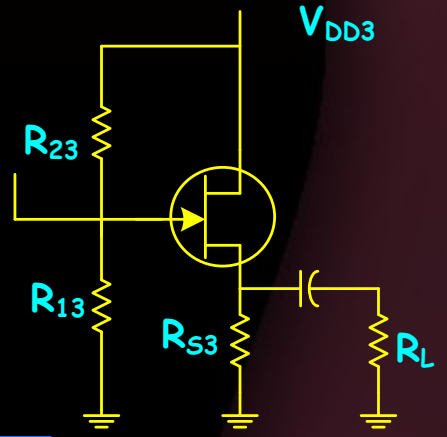
Draw and design R_{13} , R_{23} , and V_{DD3} of the third stage JFET voltage-divider bias SF amplifier circuit if the FET data is I_{GSS}=1μA, I_{DSS}=10mA and V_P=-3V, The required specification is $V_S=V_{DD}/2$ to drive a load of $R_S = R_L$ 1kΩ
Find R_o of your amplifier and # maximum input voltage at the first stage.

$$R_{in3} = R_{13}//R_{23} = 20k = R_G < \frac{0.1V_P}{I_{GSS}} = \frac{0.3}{1\mu A} = 0.3M = \underline{\underline{300k\Omega}}$$

Check R_{in3} < 300k with I_{GSS}=1μA

$$\text{Opt. } I_D = (10mA/2) = 5mA \Leftrightarrow \text{Opt. } V_{GS} = 0.3\times(-3) = -0.9V$$

$$\text{Opt. } gm = 1.42\frac{I_{DSS}}{|V_P|} = 1.42\frac{10mA}{3} = 4.734(mA/V)$$



$$I_{D3}R_S = \frac{V_{DD3}}{2} = 5mA\times 1k = 5V \Rightarrow V_{DD} = 2\times 5 = 10V$$

V_{DD3}

$$V_{GG} = V_{GS} + I_D R_S \Rightarrow -0.9 + 5 = 4.1V$$

$$R_{13} = \frac{R_G}{1-\frac{V_{GG}}{V_{DD}}} = \frac{20k}{1-\frac{4.1}{10}} = 33.9k\Omega$$

$$R_{23} = R_G\frac{V_{DD}}{V_{GG}} = 20k\frac{10}{4.1} = 48.8k\Omega$$

R_{13} R_{23}

$$A_{v3} = \frac{4.734(R_S//R_L)}{1+4.734\times(R_S//R_L)} = \frac{4.734mA\times 1k}{1+4.734mA\times 1k} = 0.825$$

$$AvT = (-12)(-164)(0.825) = 1623.6$$

A_{vT}

$$V_{o3} = 2I_{D3}R_{ac3} = 2\times 5mA\times 0.5k = 5V$$

$$V_{in1}(pp) = \frac{5}{A_{vT}} = \frac{5}{1623.6} = 0.003V = 3mV$$

V_{in1} (pp)

$$R_o = R_S//(1/g_m) = 1k//(1/4.734)k = 1k//0.211k = 174\Omega$$

R_o < 1k so it can drive R_L=1kΩ load easily

Overall performance

Find A_{vT} of your amplifier and # maximum input voltage at the first stage and # check R_o whether it can drive R_L=1kΩ load easily.

$$A_{v3} = \frac{4.734(R_S // R_L)}{1 + 4.734 \times (R_S // R_L)} = \frac{4.734mA \times 1k}{1 + 4.734mA \times 1k} = 0.825$$

$$AvT = (-12)(-164)(0.825) = 1623.6$$

A_{vT}

$$V_{o3} = 2I_{D3}R_{ac3} = 2 \times 5mA \times 0.5k = 5V$$

$$V_{in1}(pp) = \frac{5}{A_{vT}} = \frac{5}{1623.6} = 0.003V = 3mV$$

V_{in1} (pp)

$$R_o = R_S //(1/g_m) = 1k //(1/4.734)k = 1k // 0.211k = 174\Omega$$

R_o < 1k so it can drive R_L=1kΩ load easily