SECTION B

NMOS & CMOS inverters and Gates

Lamda Base rule.

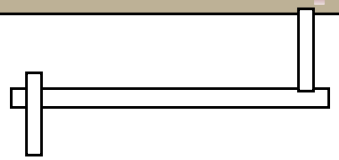
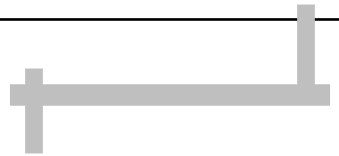
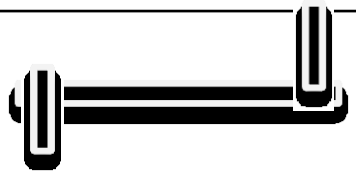
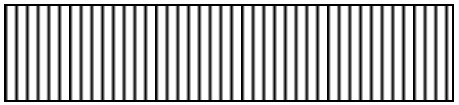
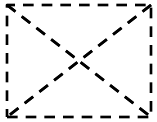
Topic Covered

- **NMOS & CMOS INVERTER AND GATES :** NMOS & CMOS inverter – Determination of pull up /
- pull down ratios – Stick diagram – Lamda based rules – Super buffers – BiCMOS & steering logic

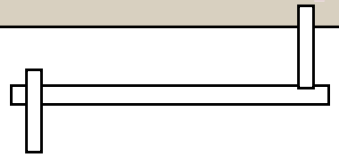
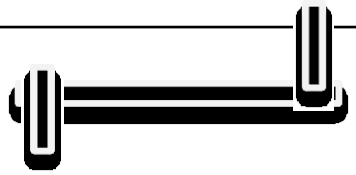
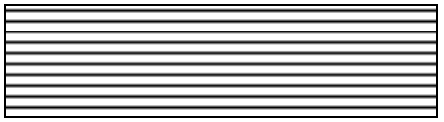
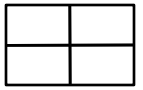
Stick Diagrams

- VLSI design aims to translate circuit concepts onto silicon
- stick diagrams are a means of capturing topography and layer information - simple diagrams
- Stick diagrams convey layer information through color codes (or monochrome encoding)

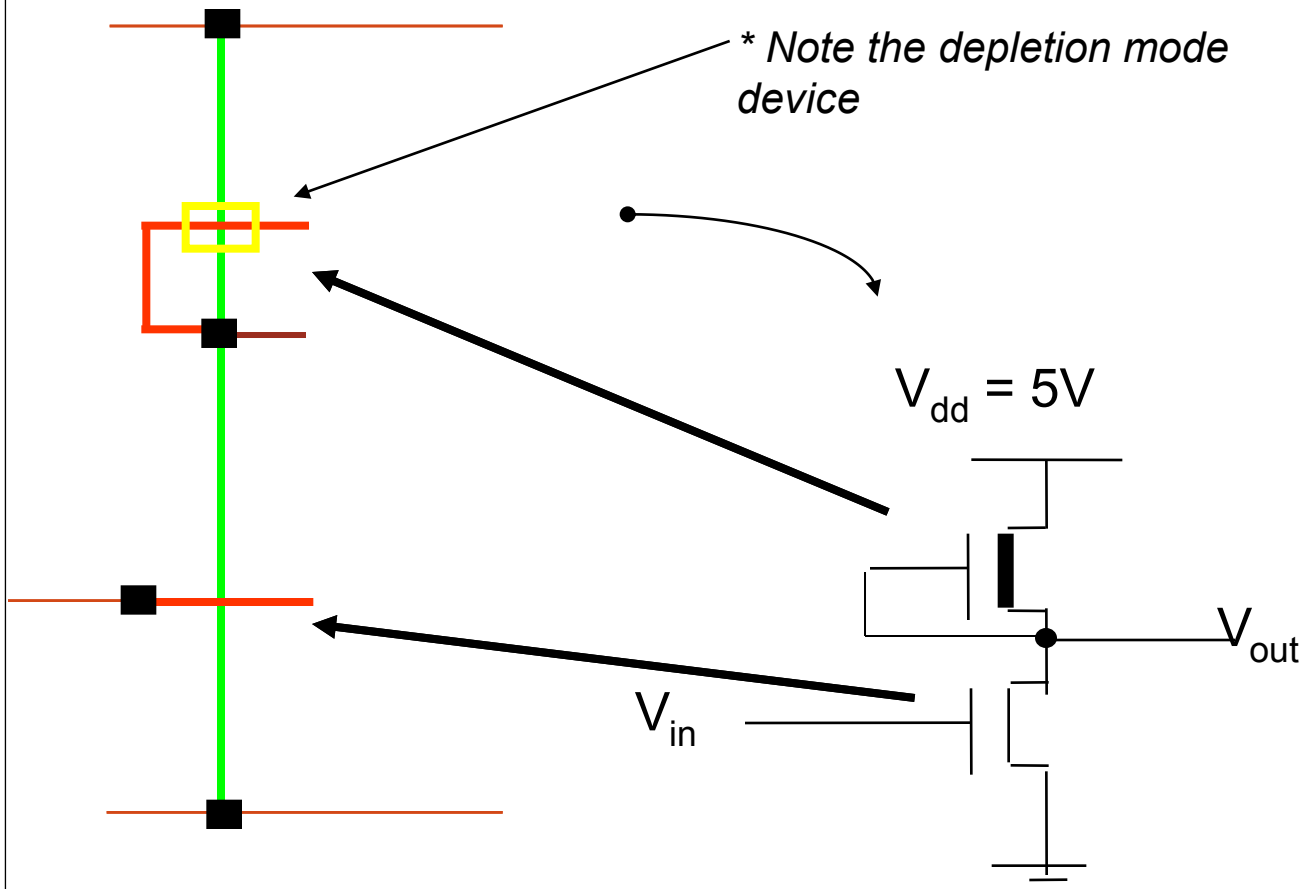
Encoding for nMOS process

Stick Encoding	Layer	Mask Layout Encoding
	Thinox	
	Polysilicon	
	Metal1	
	Contact cut	
NOT applicable	Overglass	
	Implant	
	Buried contact	

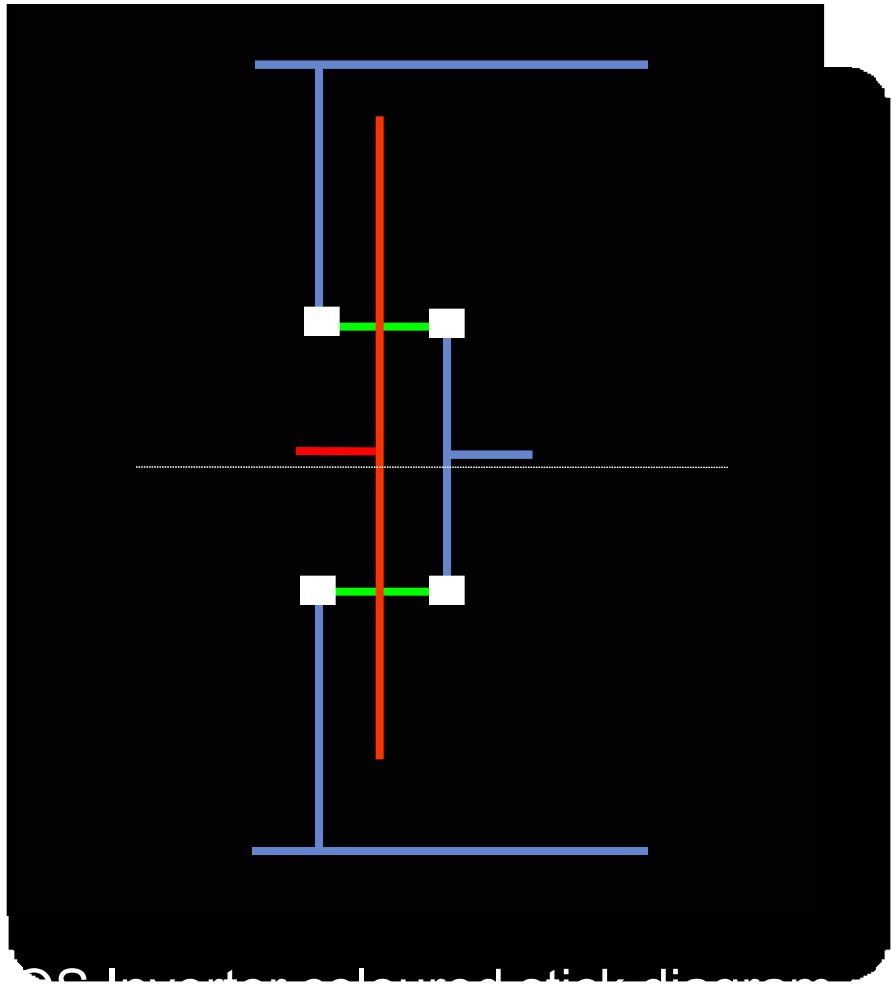
Encoding for pMOS process

Stick Encoding	Layer	Mask Layout Encoding
	**P-Diffusion**	
Not Shown in Stick Diagram	**P+ Mask**	
	**Metl2**	
	**VIA**	
Demarcation Line 	**P-Well**	
	**Vdd or GND CONTACT**	

For reference : an nMOS Inverter coloured stick diagram

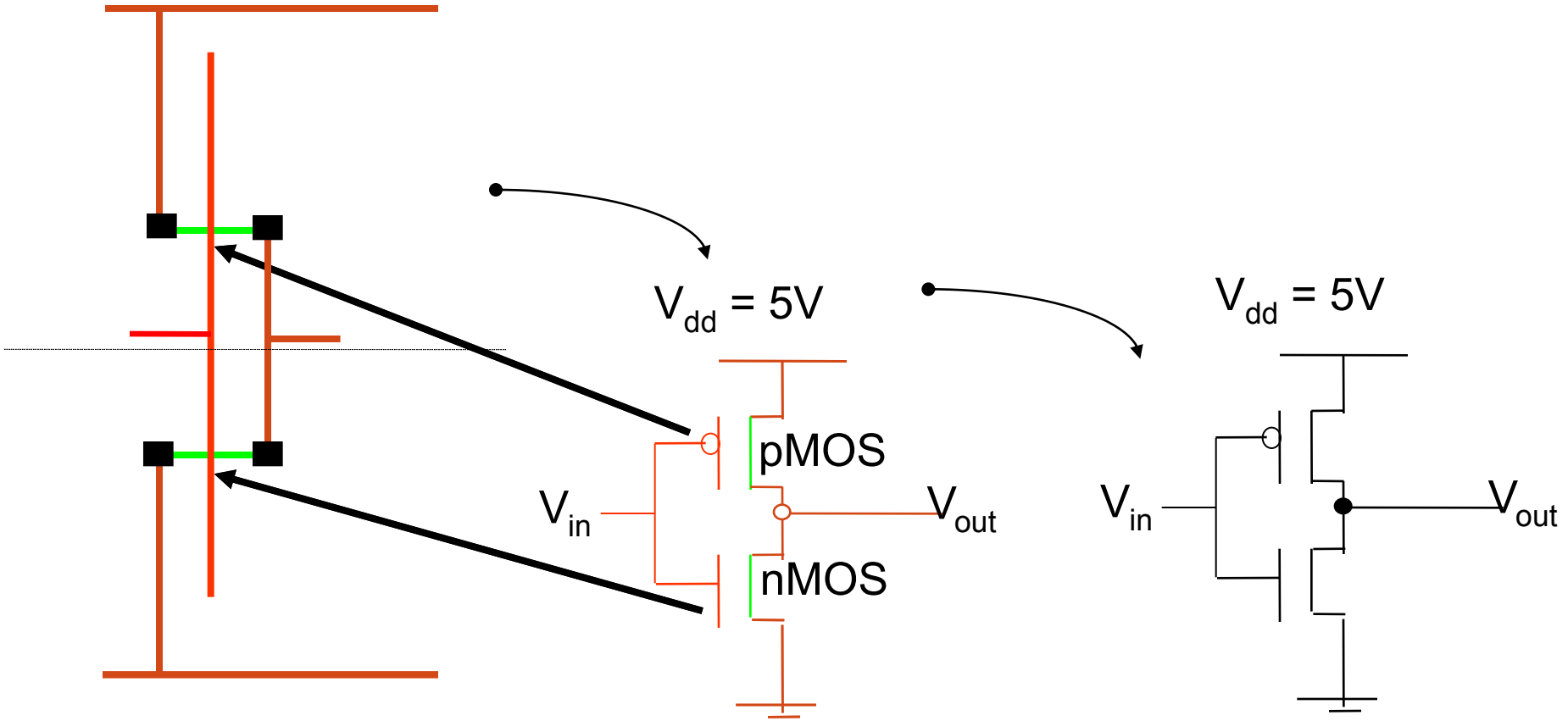


Only metal and polysilicon can cross the dimarcation line.



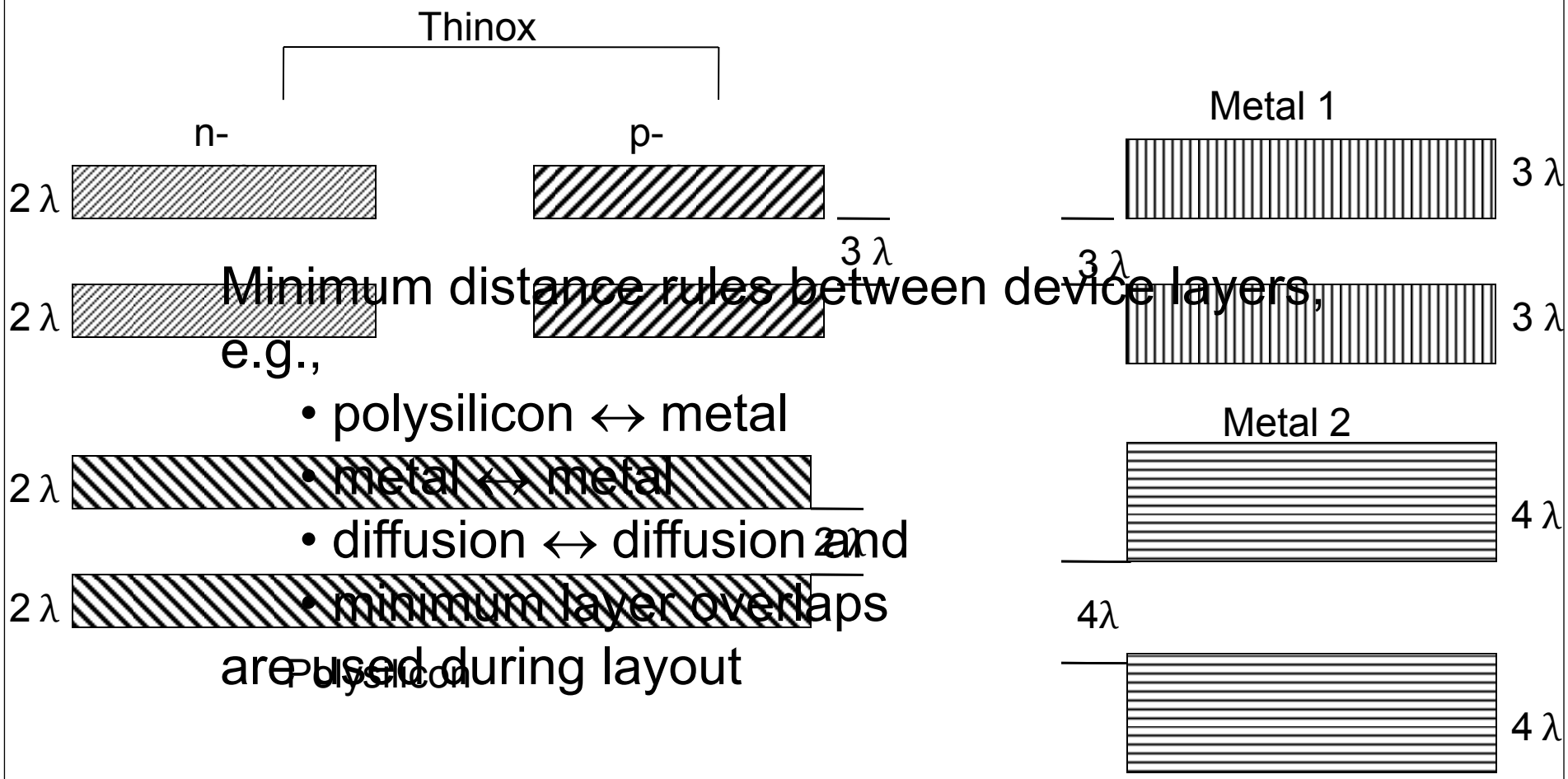
CMOS Inverter coloured stick diagram

Stick diagram -> CMOS transistor circuit



All paths in all layers will be dimensioned in λ units and subsequently λ can be allocated an appropriate value compatible with the feature size of the fabrication process.

TRANSISTOR DESIGN RULES

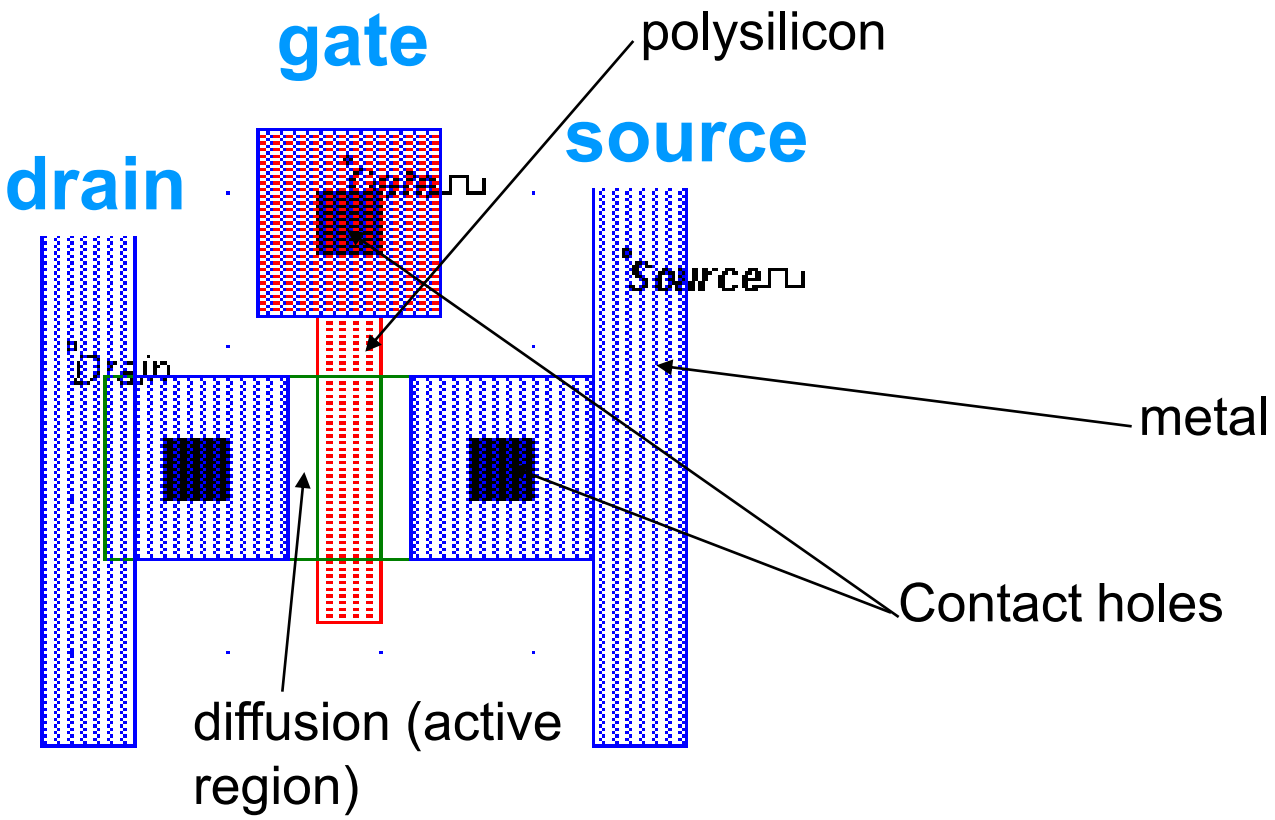


Minimum distance rules between device layers, e.g.,

- polysilicon ↔ metal
- metal ↔ metal
- diffusion ↔ diffusion and
- minimum layer overlaps

are used during layout

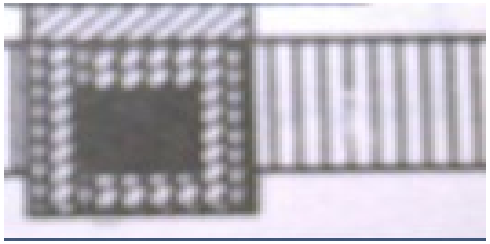
nMOS transistor mask representation

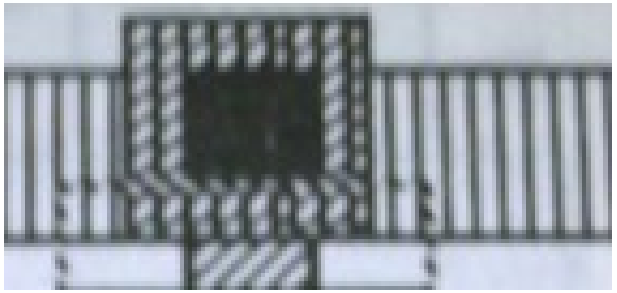


Contact Cuts

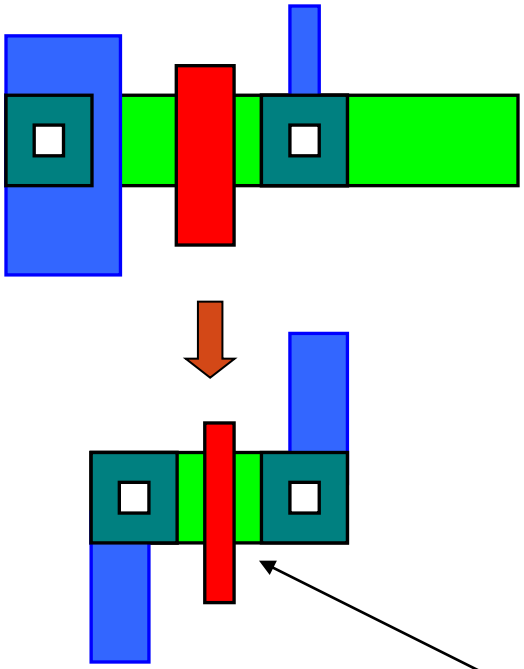
- Three possible approaches –

1. Poly to Metal
2. Metal to Diffusion
3. Buried contact (poly to diff) or butting contact (poly to diff using metal)

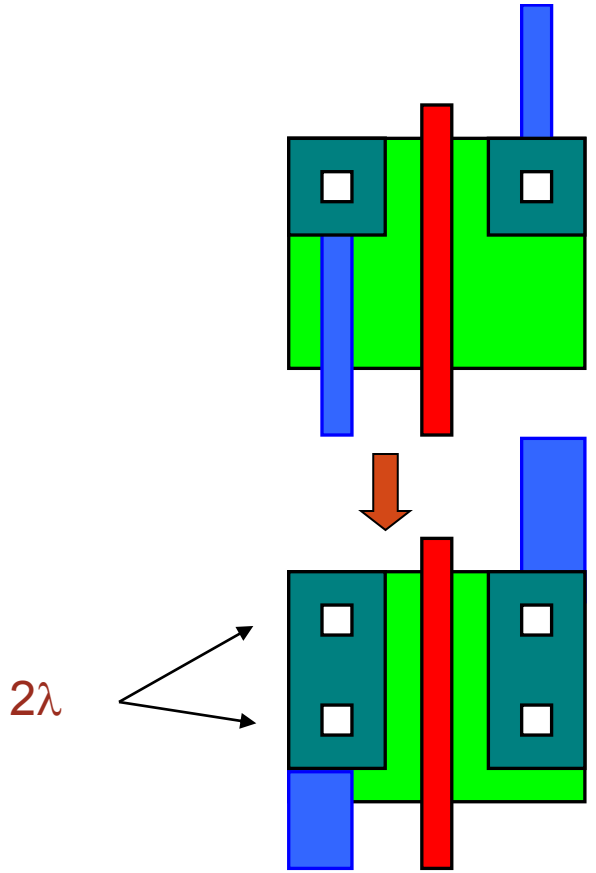




Layout Design rules & Lambda (λ)

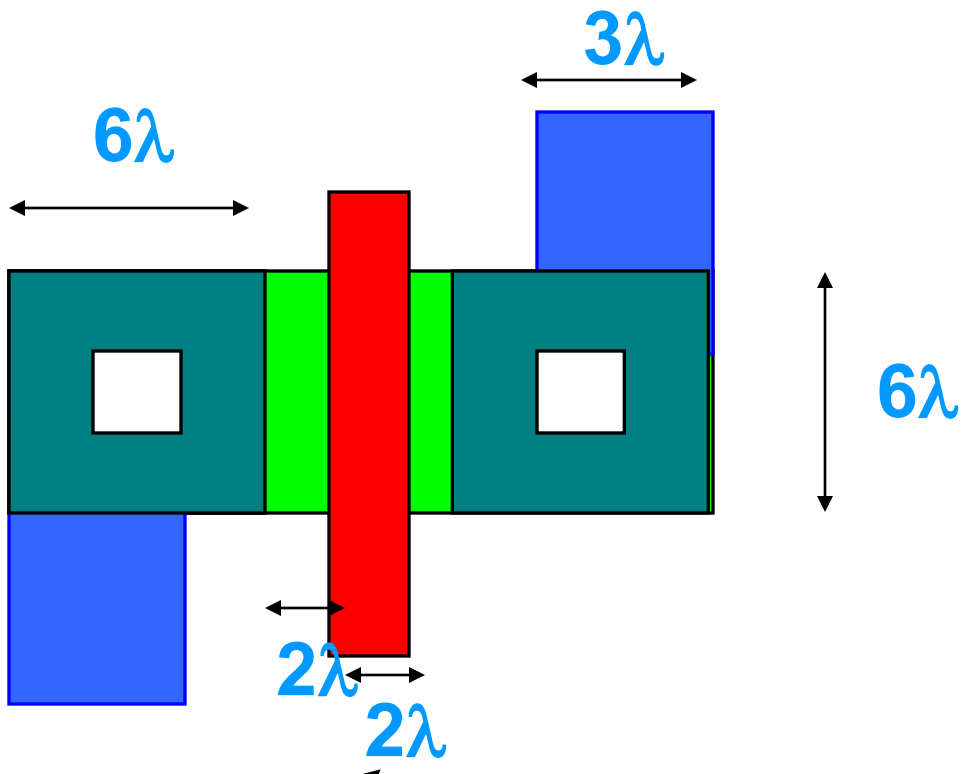


- Minimize spared diffusion
- Use minimum poly width (2λ)



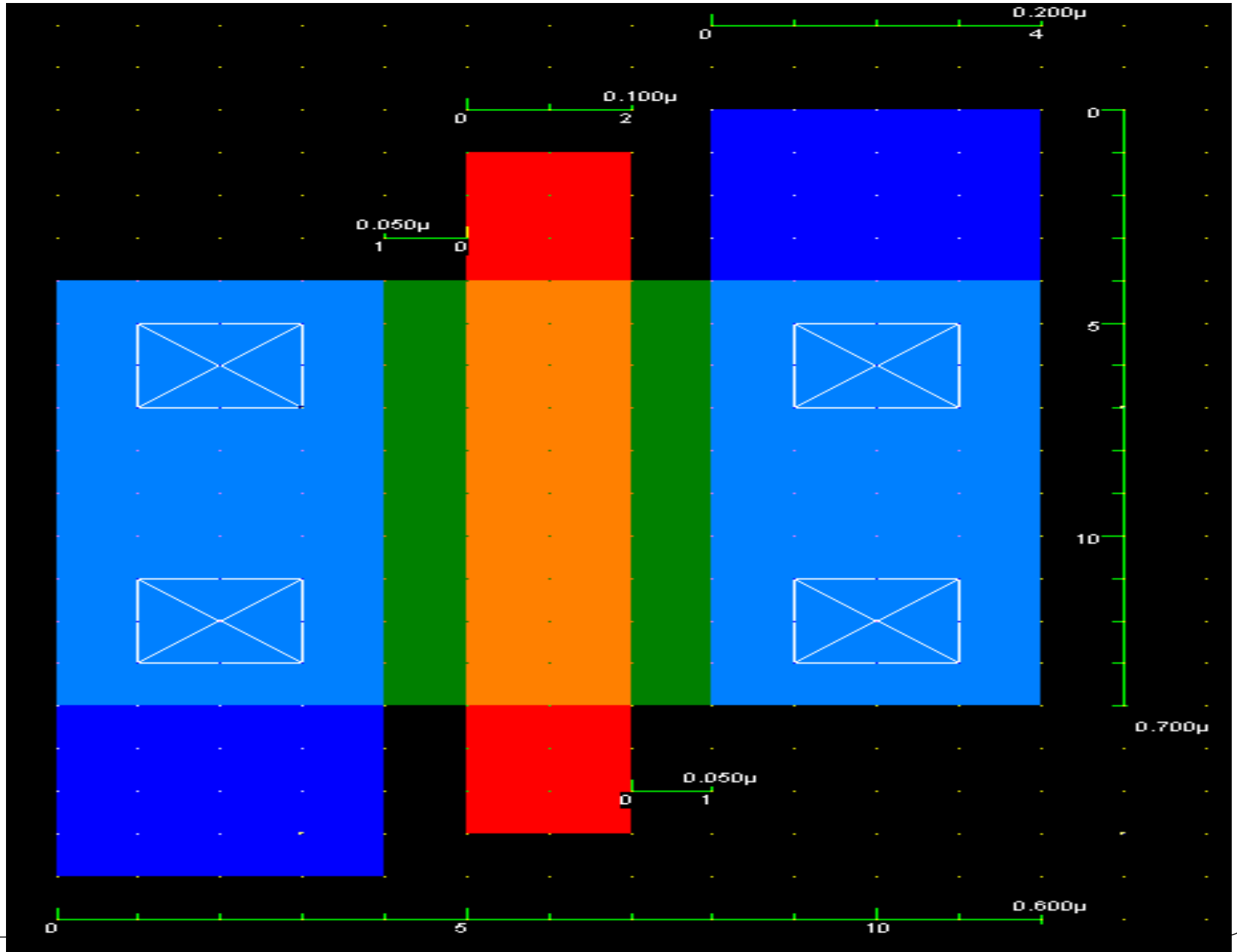
- Width of contacts = 2λ
- Multiply contacts

Layout Design rules & Lambda (λ)

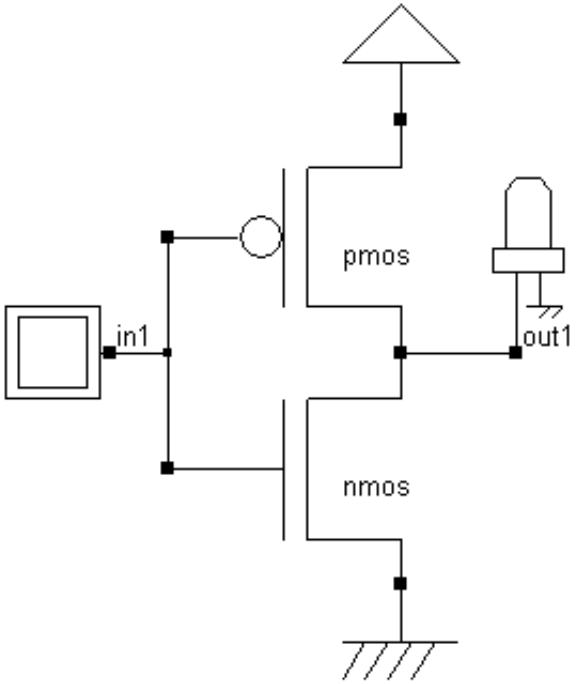


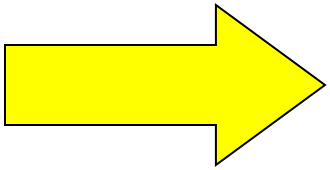
All device mask dimensions are based on multiples of λ, e.g., polysilicon minimum width = 2λ. Minimum metal to metal spacing = 3λ

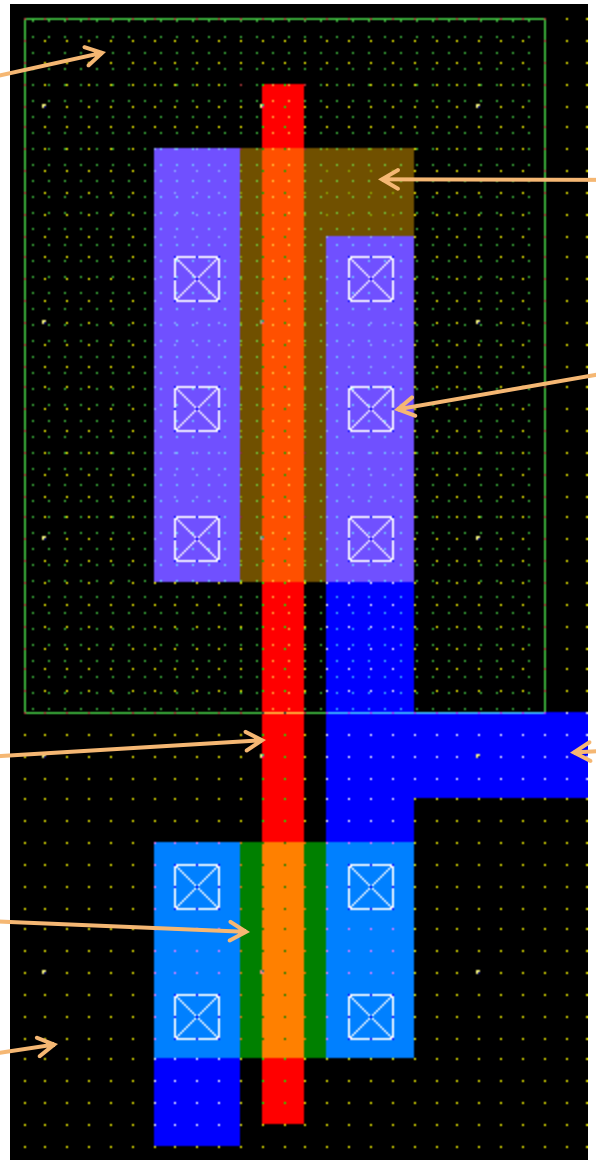
Layout Design rules & Lambda (λ)



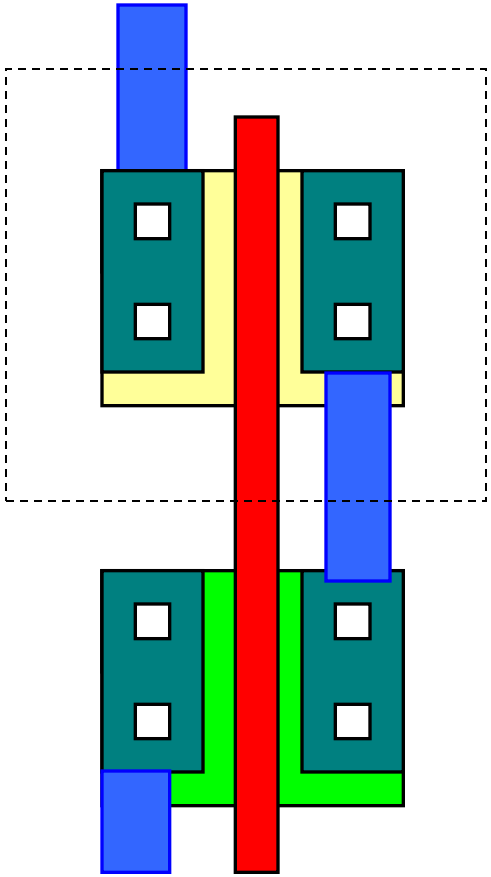
CMOS Layout


pmos
in1
out1
nmos

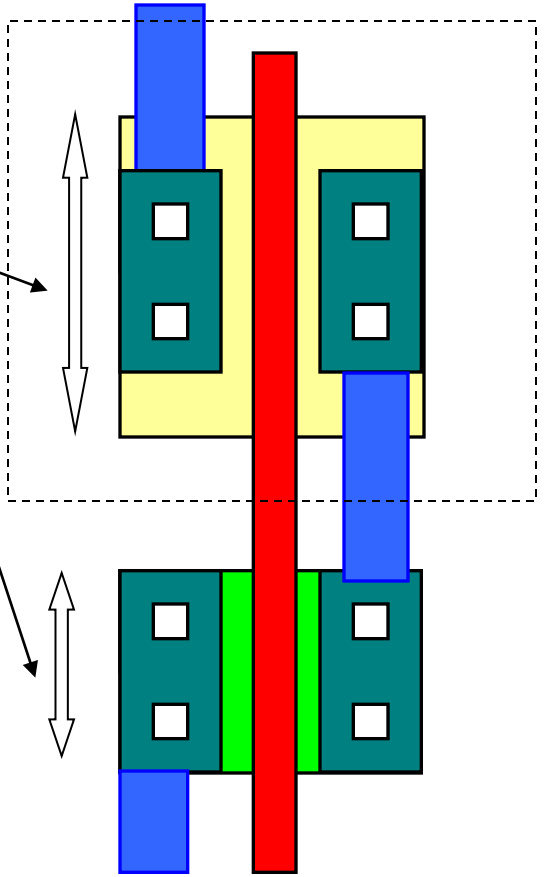



N Well
P diff
Contacts
Poly
Metal
N diff
P Substrate

Layout Design rules & Lambda (λ)



Width of pMOS should be twice the width of nMOS



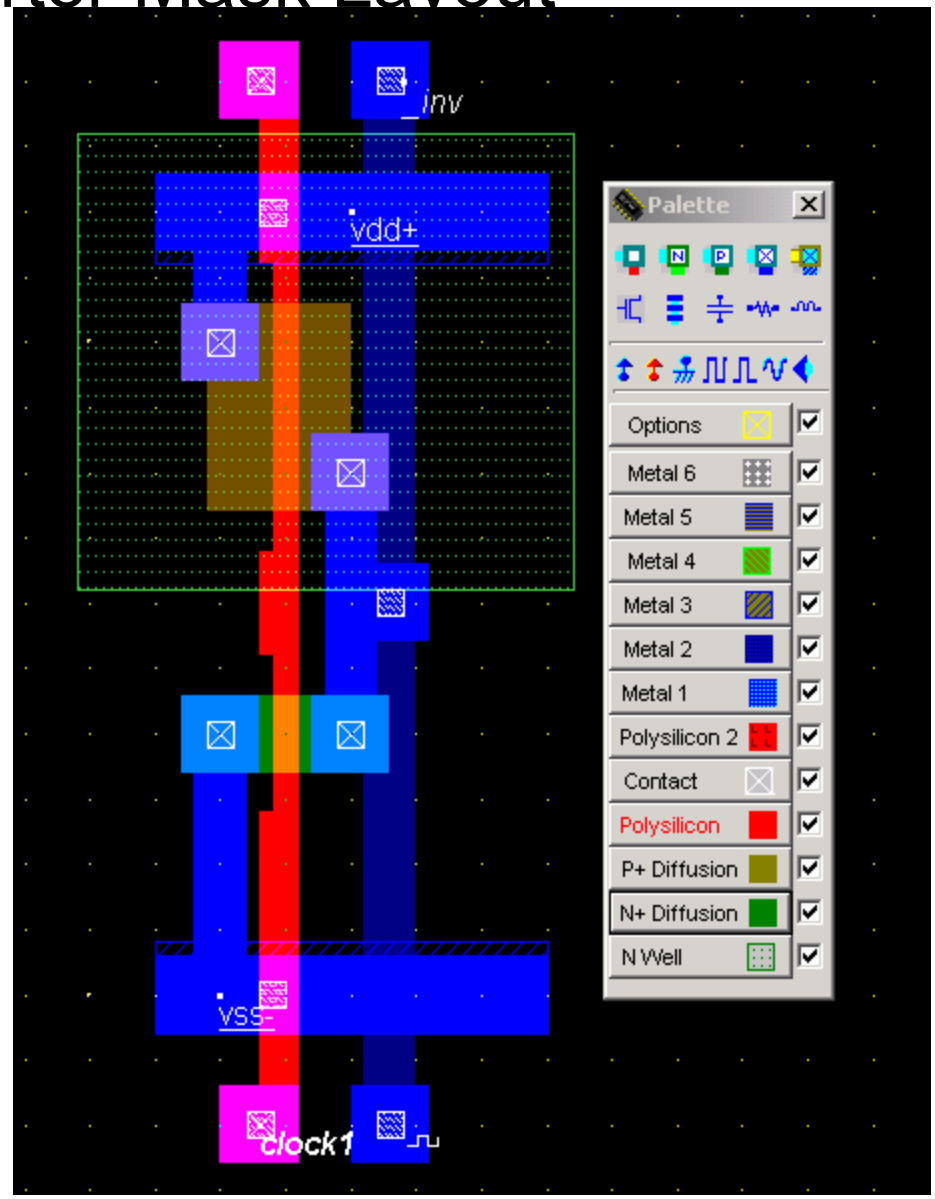
- Same N and P alters symmetry

- L min
- Wpmos=2 Wnmos

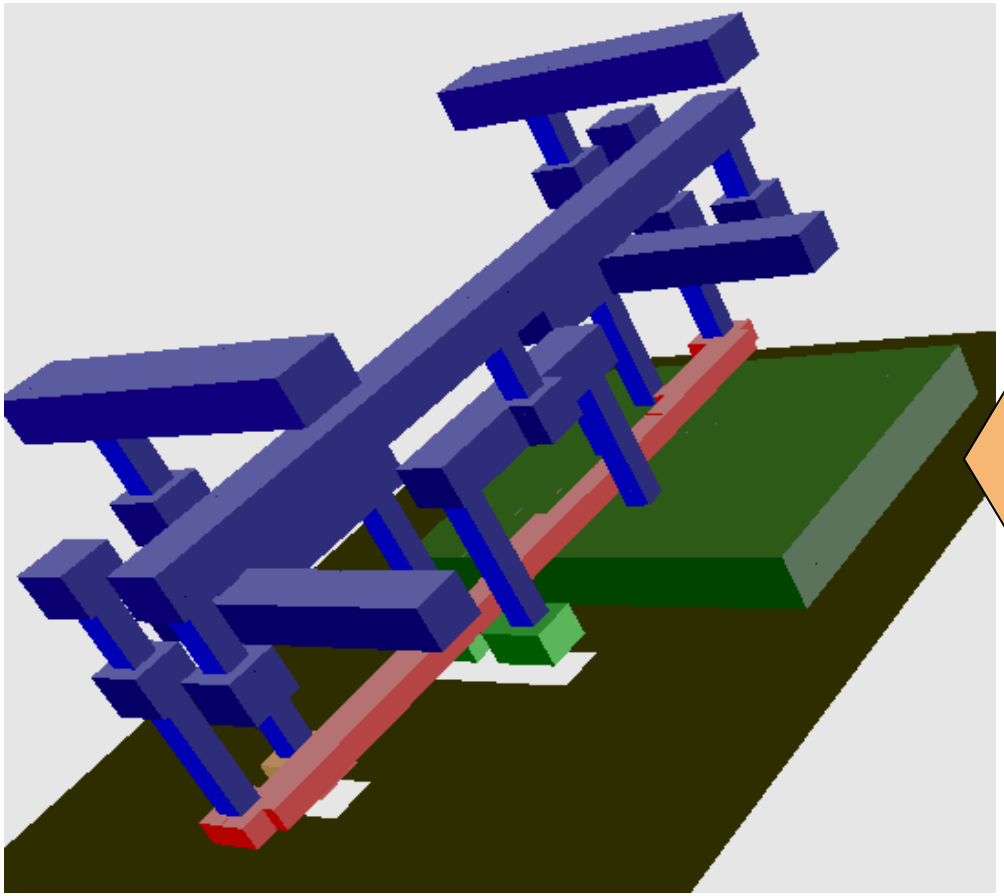
Lambda Based Design Rules

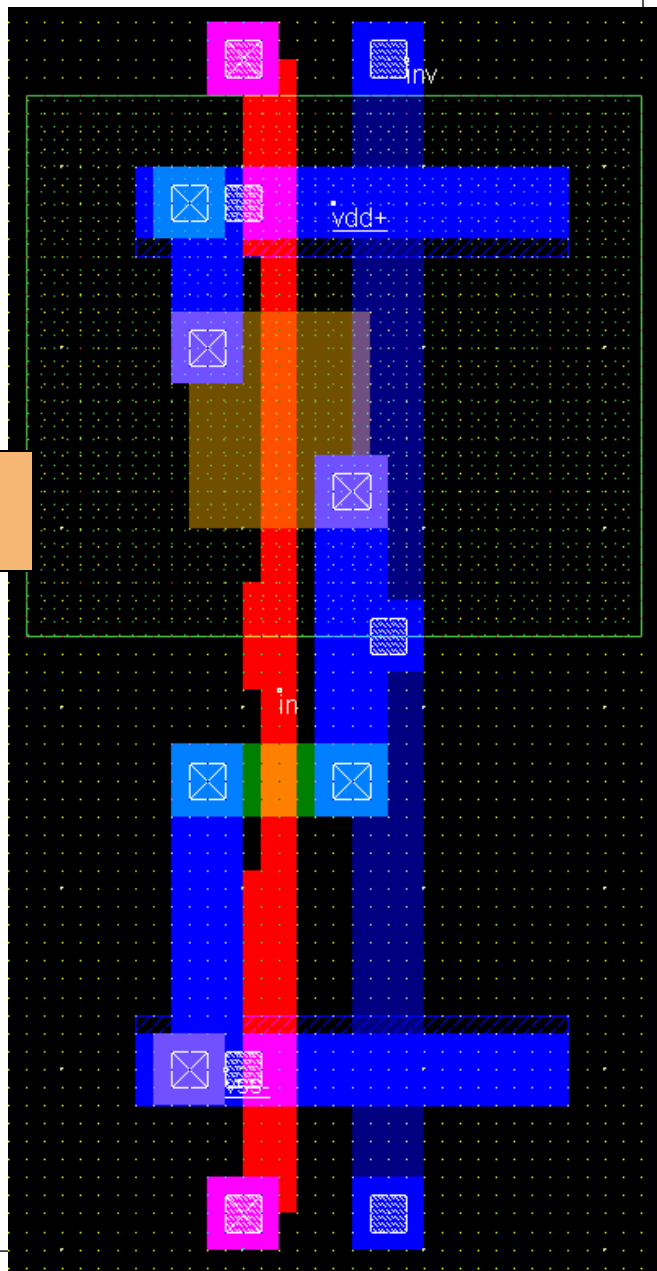
- Design rules based on single parameter, λ
- Simple for the designer
- Wide acceptance
- Provide feature size independent way of setting out mask
- Minimum feature size is defined as 2 λ
- Used to preserve topological features on a chip
- Prevents shorting, opens, contacts from slipping out of area to be contacted

CMOS Inverter Mask Layout



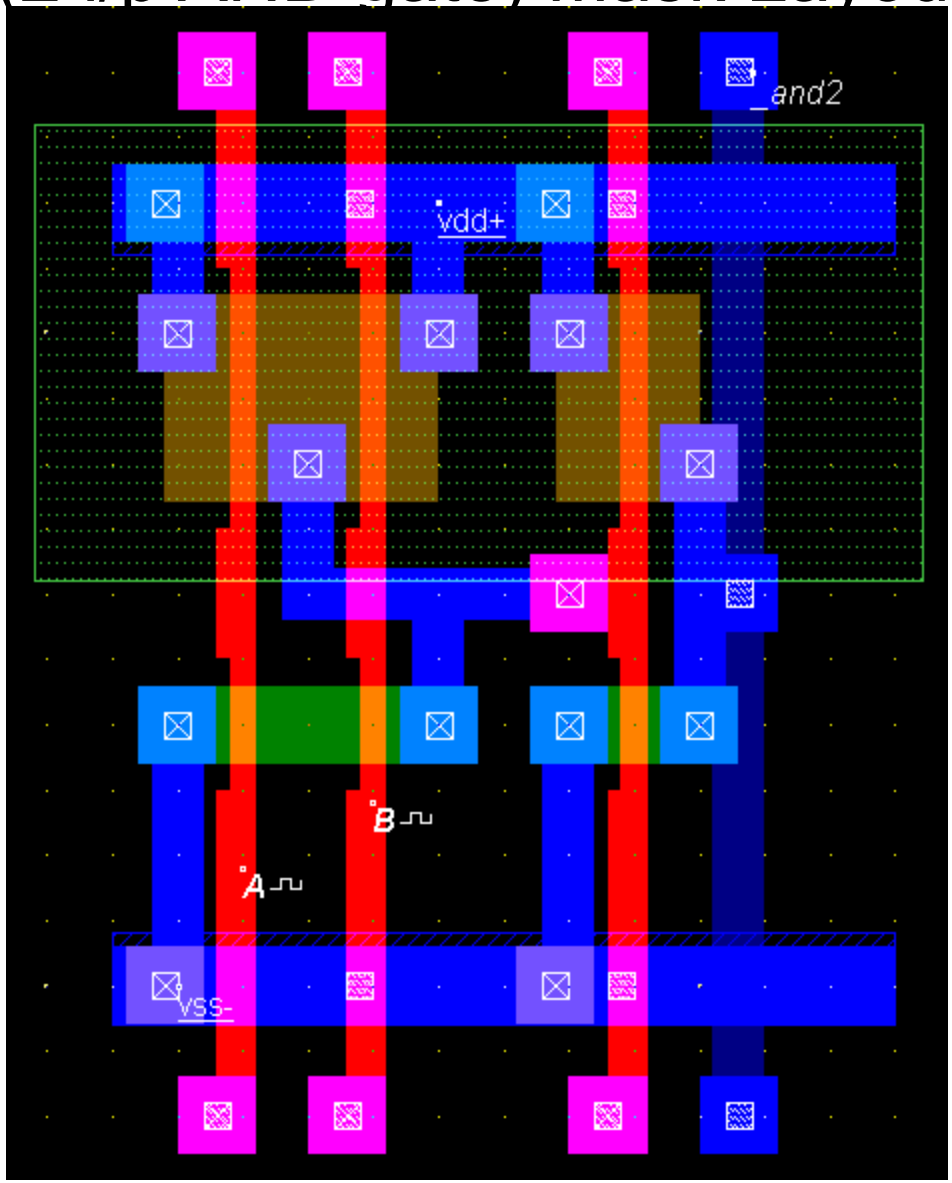
MOS Layout Design



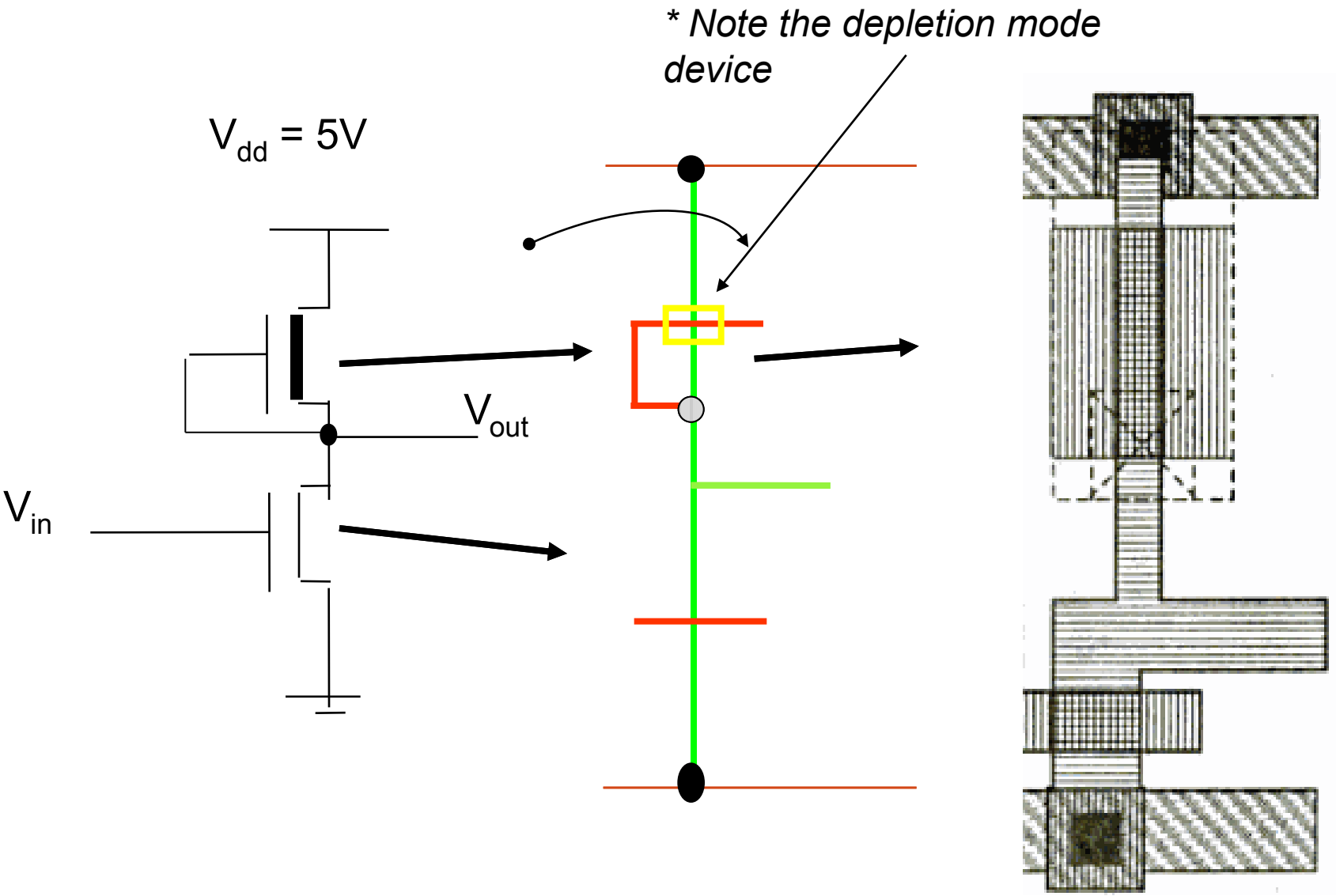


- CMOS IC are designing using stick diagrams.
- Different color codes for each layer.
- Lamda/micron grid.

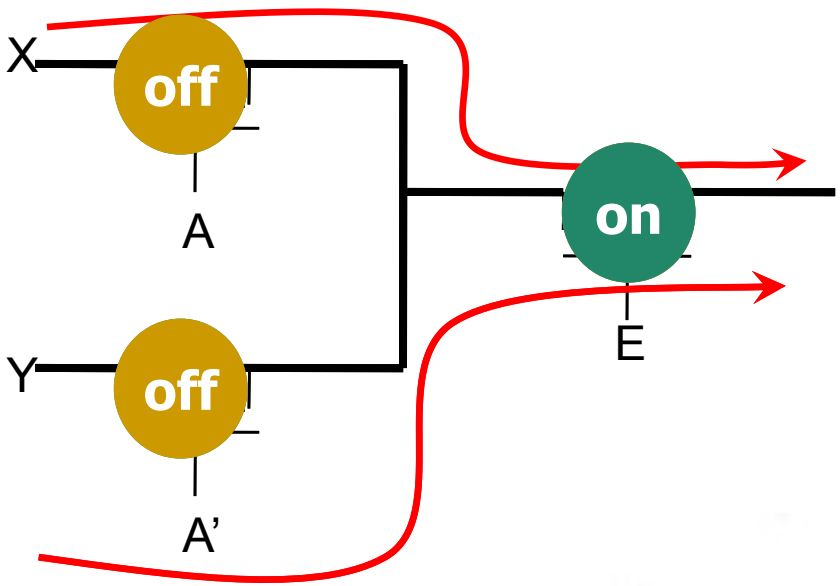
CMOS AN2 (2 i/p AND gate) Mask Layout

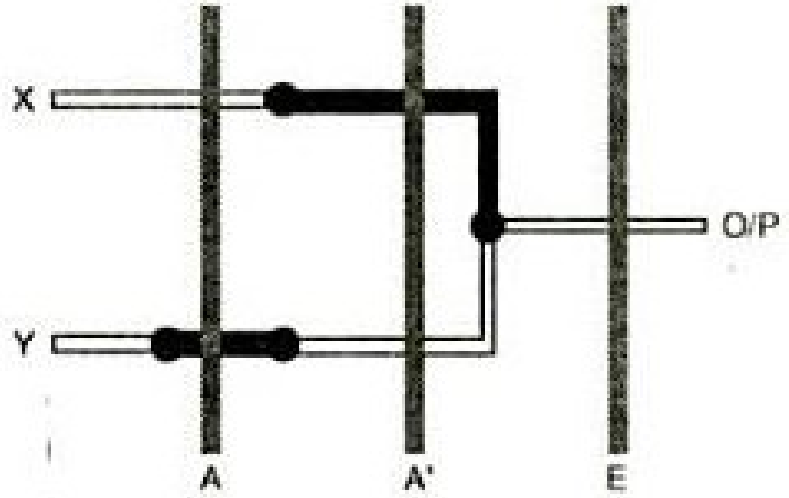


nMOS Inverter coloured stick diagram



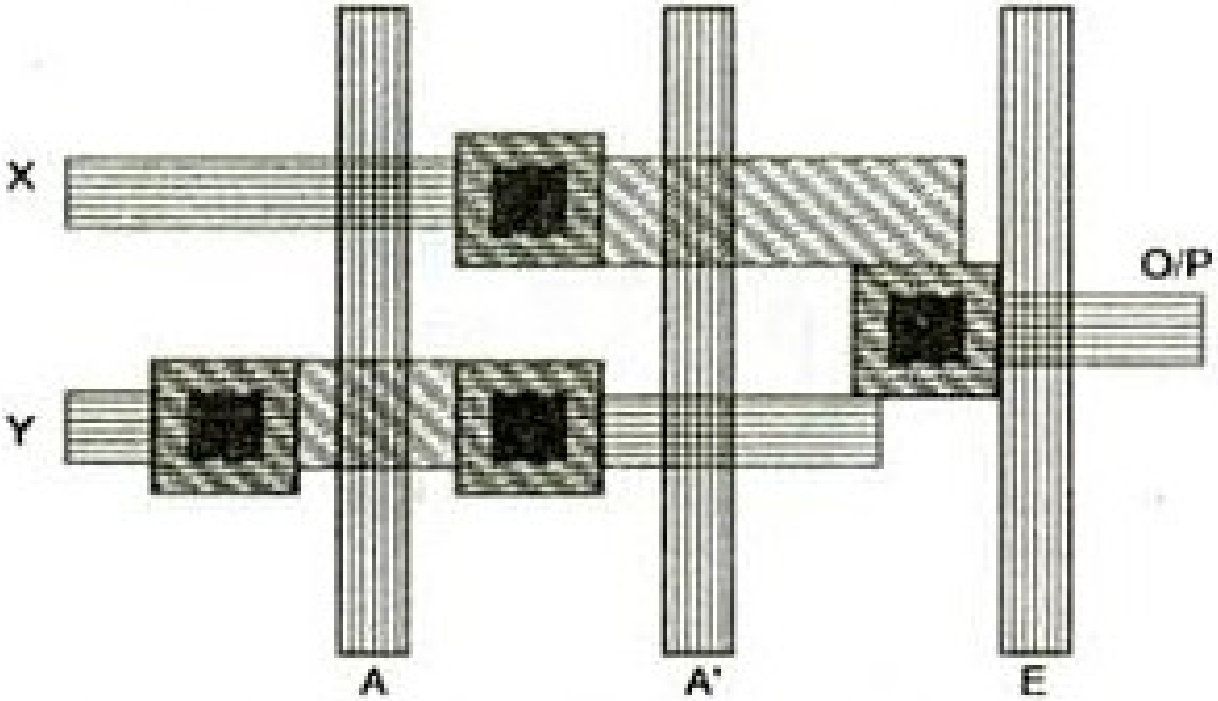
Two-way selector with enable



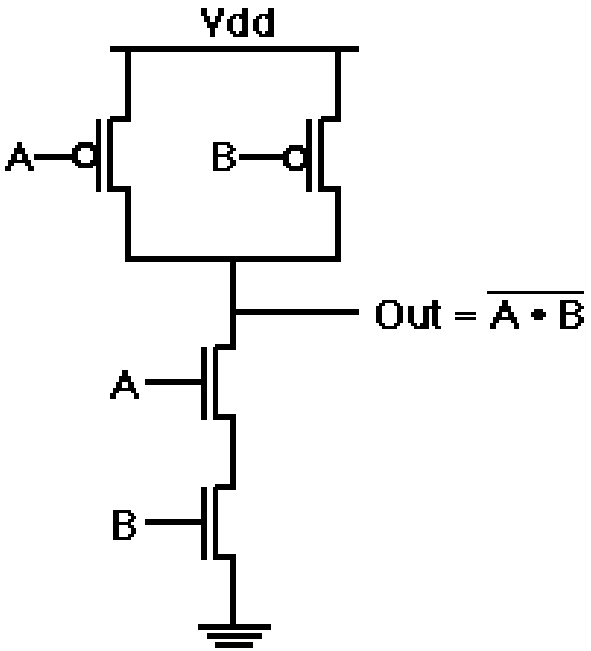


E=0

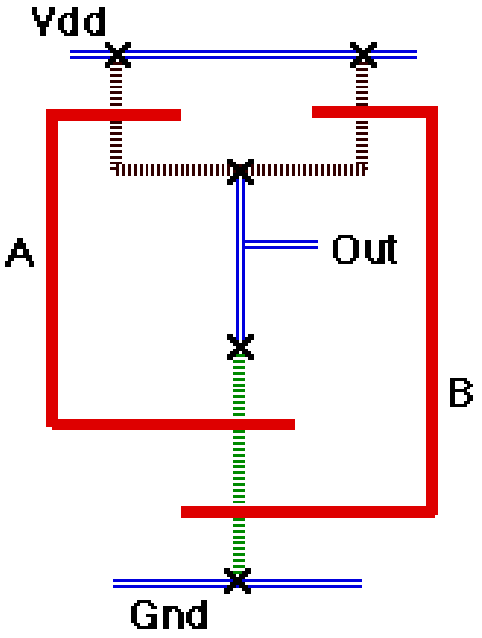
A=0|1



Static CMOS NAND gate



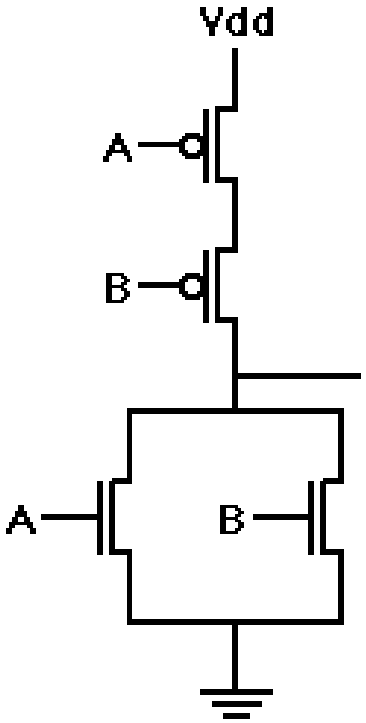
A	B	$\overline{A \bullet B}$
0	0	1
0	1	1
1	0	1
1	1	0



1. Pull-down: Connect to ground if A=1 AND B=1

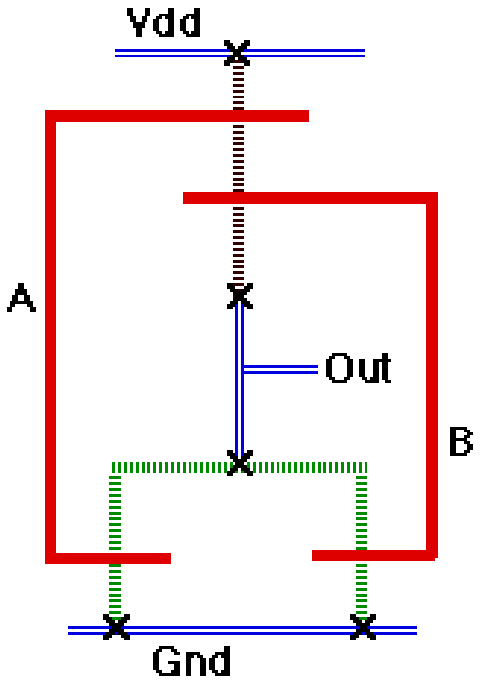
2. Pull-up: Connect to Vdd if A=0 OR B=0

Static CMOS NOR gate



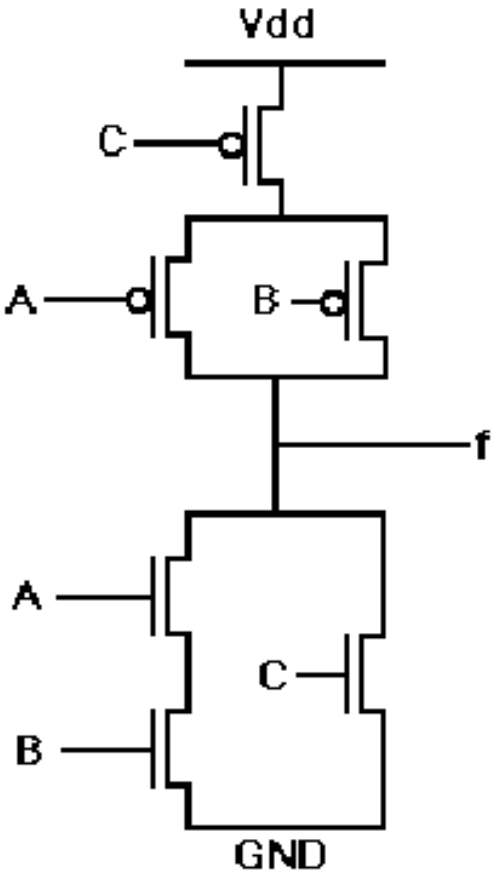
Out = $\overline{A+B}$

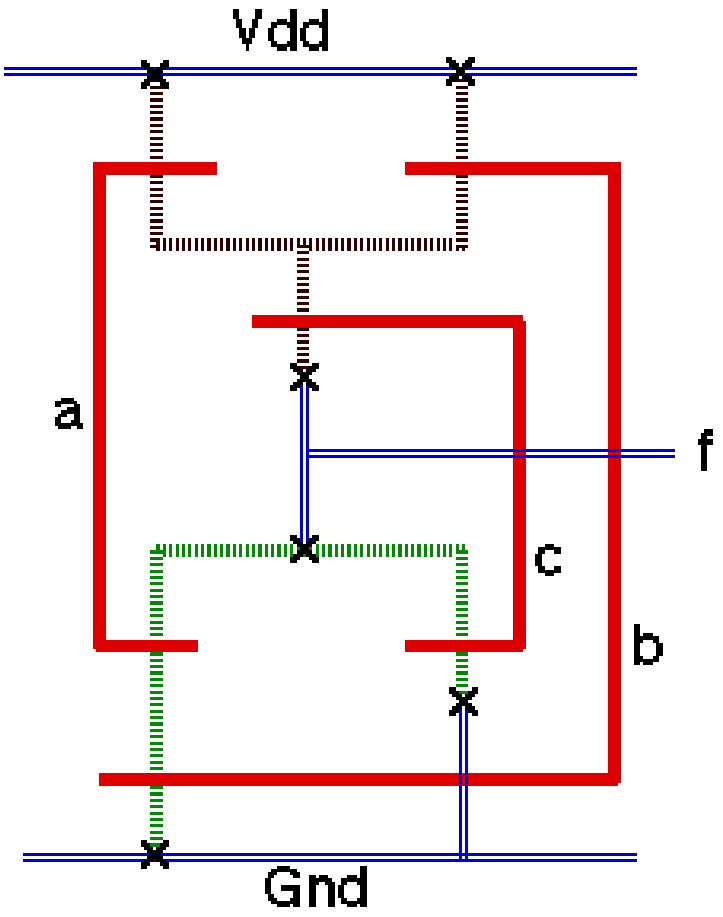
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



1. Pull-down: Connect to ground If A=1 <u>OR</u> B=1
2. Pull-up: Connect to Vdd If A=0 <u>AND</u> B=0

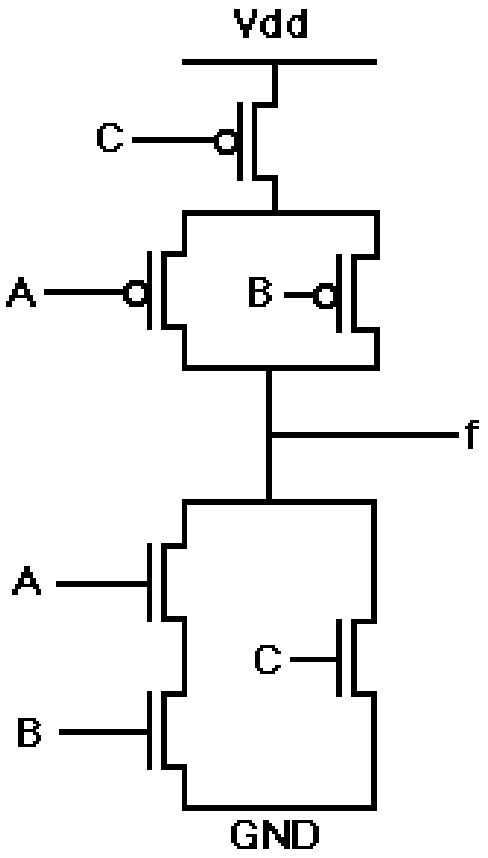
Static CMOS Design Example Layout

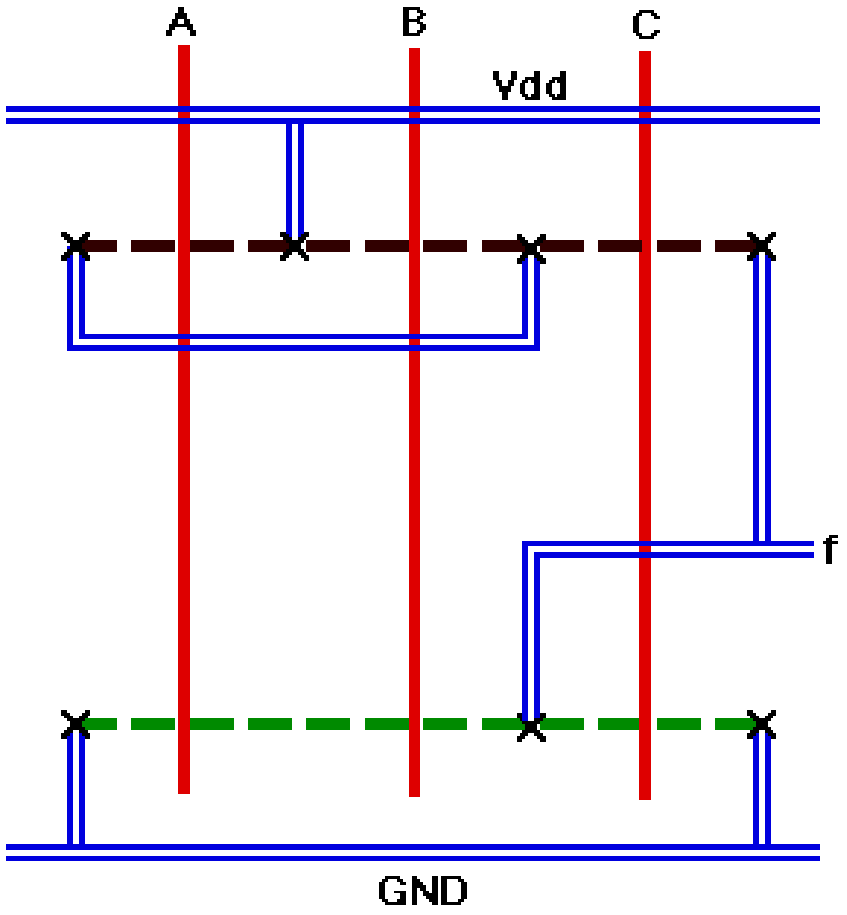




Example: $f = \overline{a \cdot b + c}$

Layout 2 (Different layout style to previous but same function being implemented)





Example: $f = \overline{a \cdot b + c}$

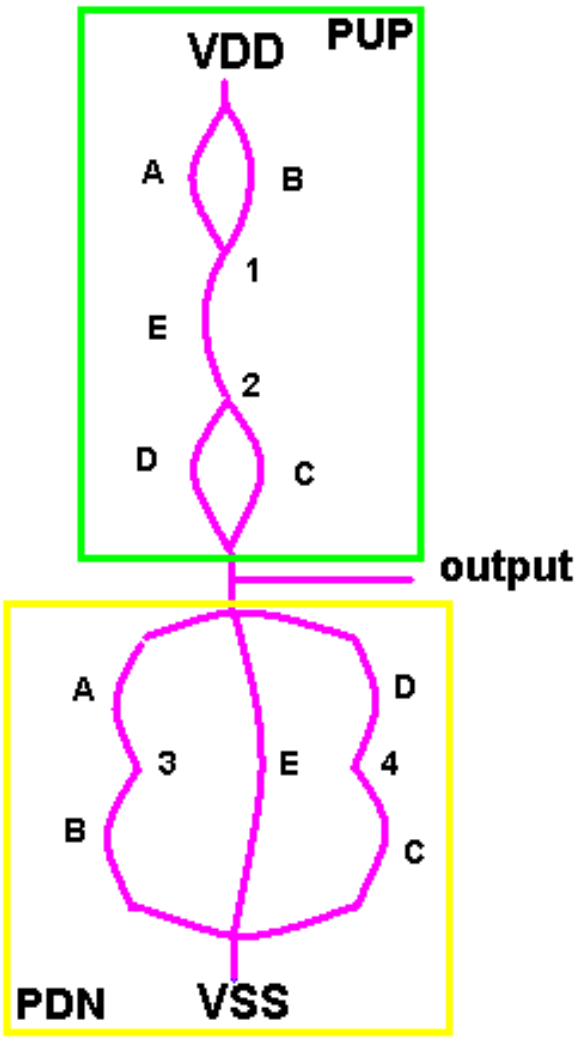
Complex logic gates layout

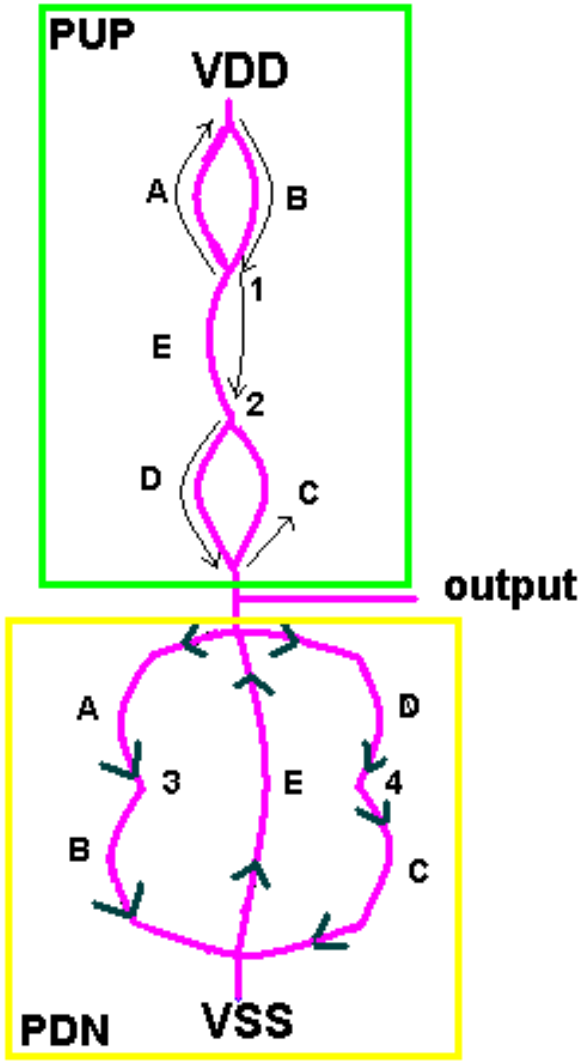
- Ex—~~F=AB+E+~~CD
- Eulerpaths
- Circuit to graph (convert)

1) Vertices are source/Drain connections
2) Edges are transistors

- Find p and n Eulerpaths

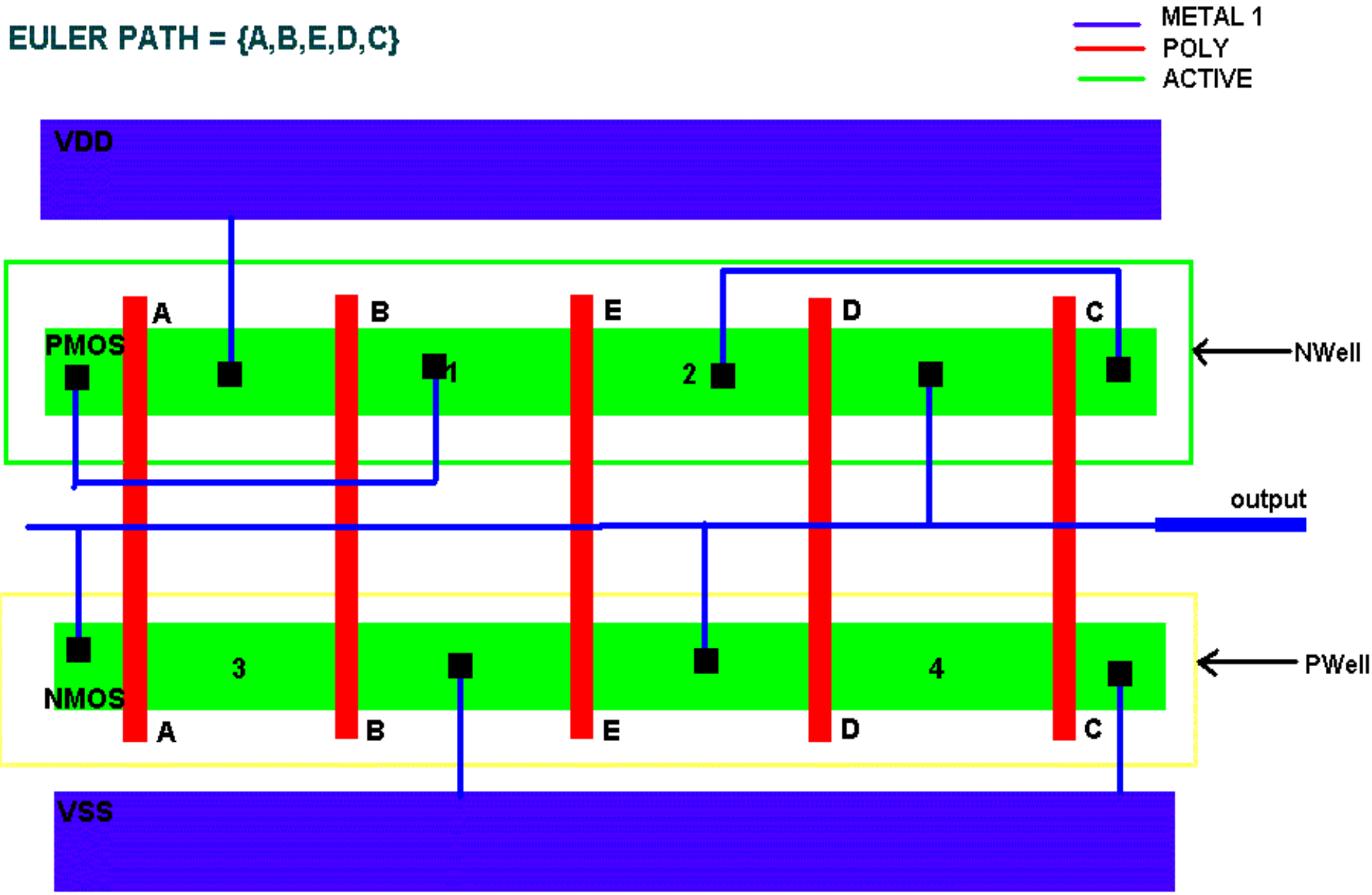
F = (AB)+E+(CD)

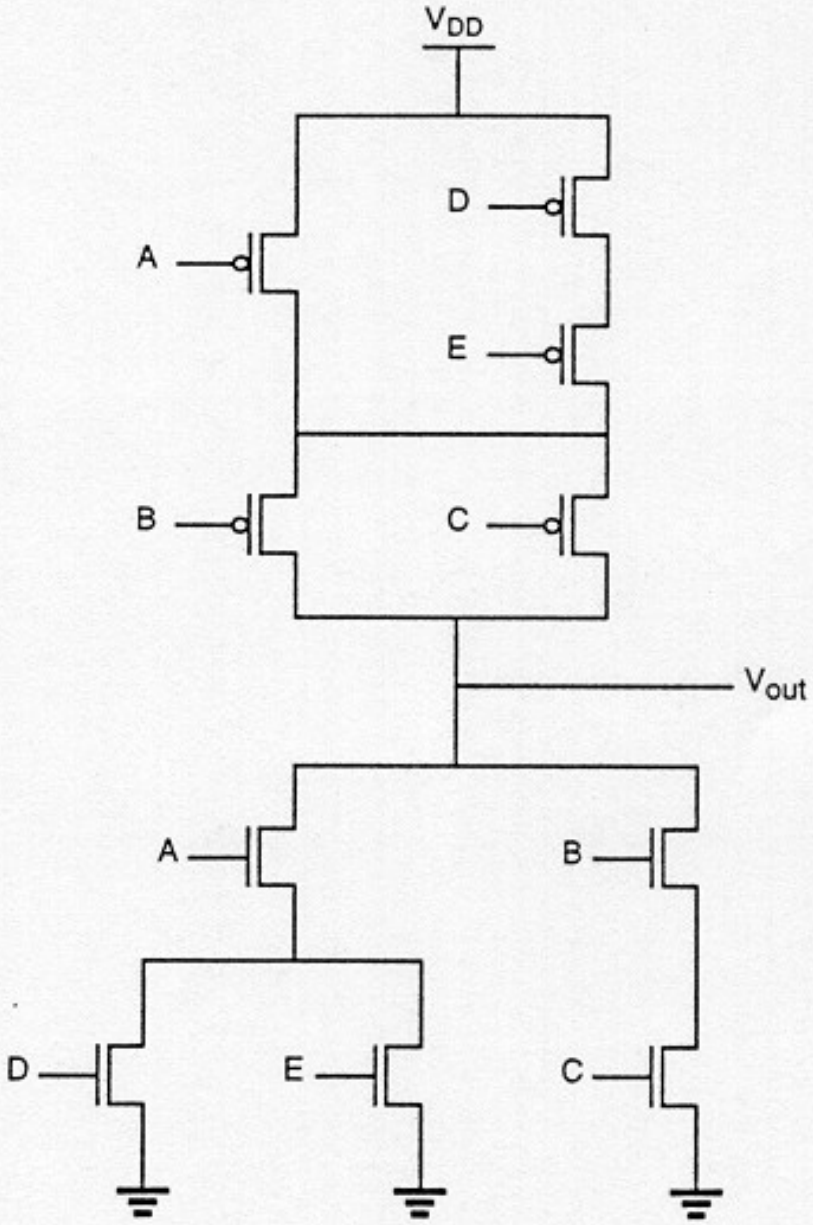


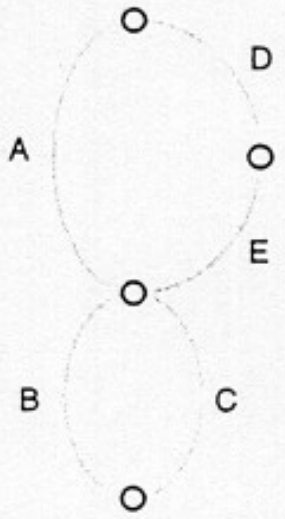


EULER PATH = {A,B,E,D,C}

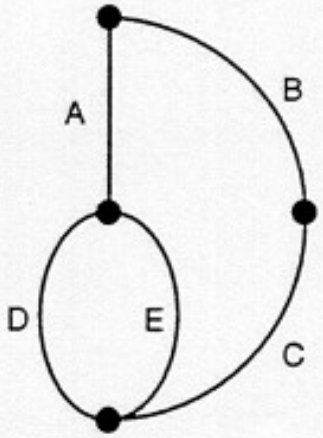
EULER PATH = {A,B,E,D,C}



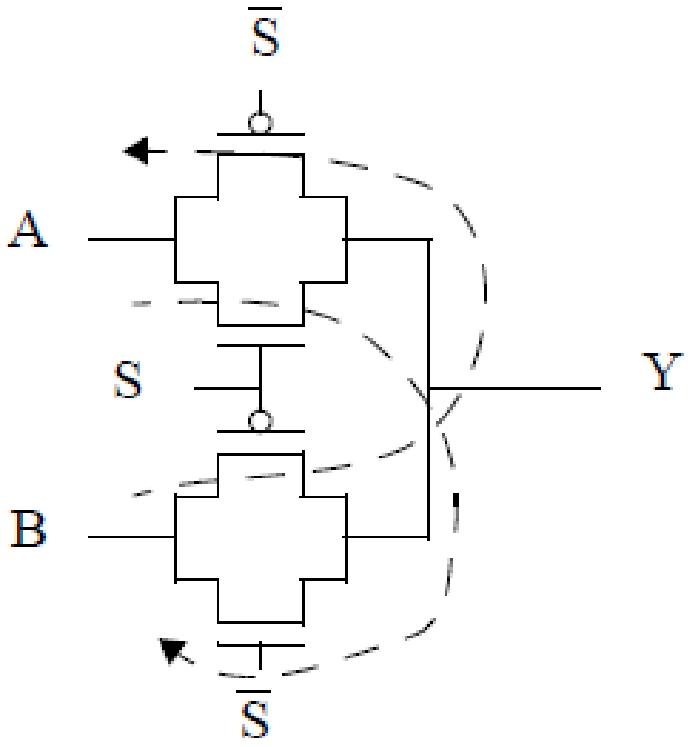


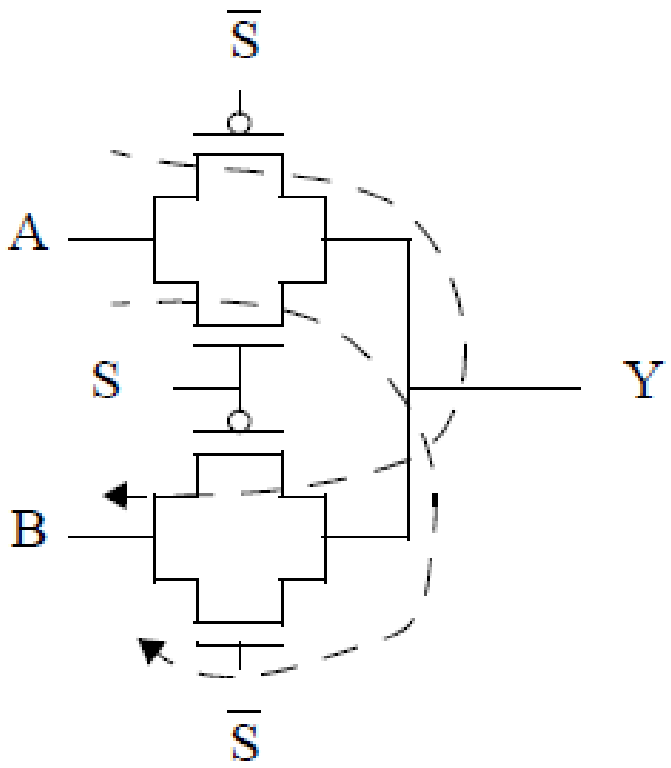


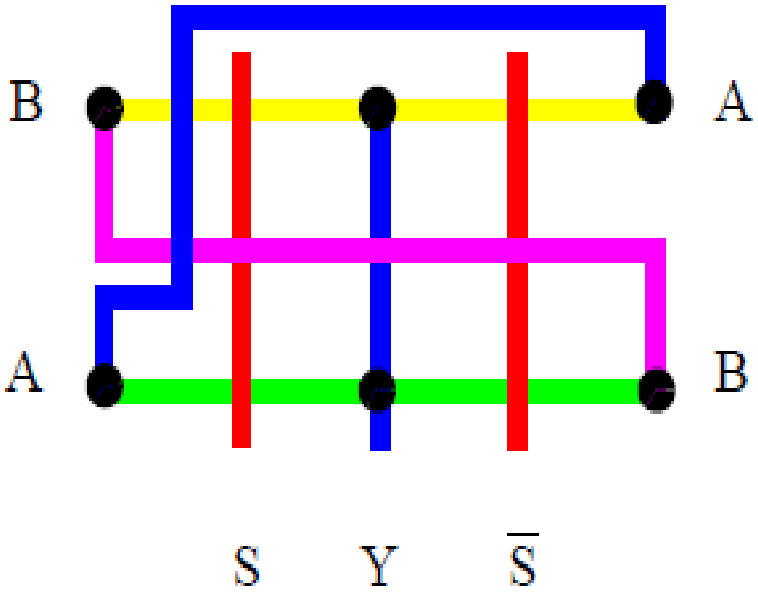
pMOS network graph

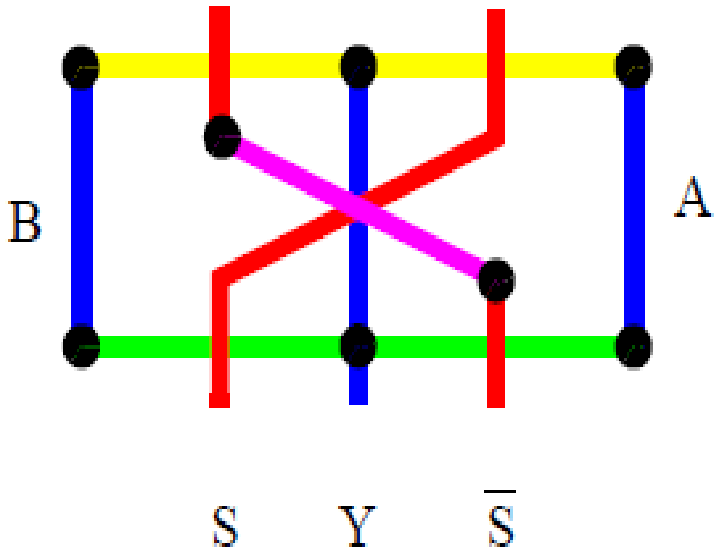


nMOS network graph


$\overline{S}$
A
S
Y
B
$\overline{S}$


$\overline{S}$
A
S
Y
B
$\overline{S}$

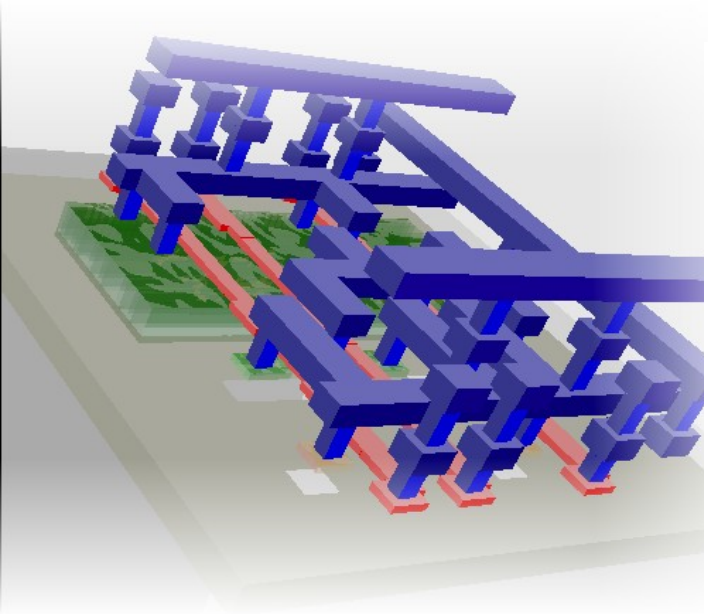

B
A
A
B
S
Y
$\overline{S}$

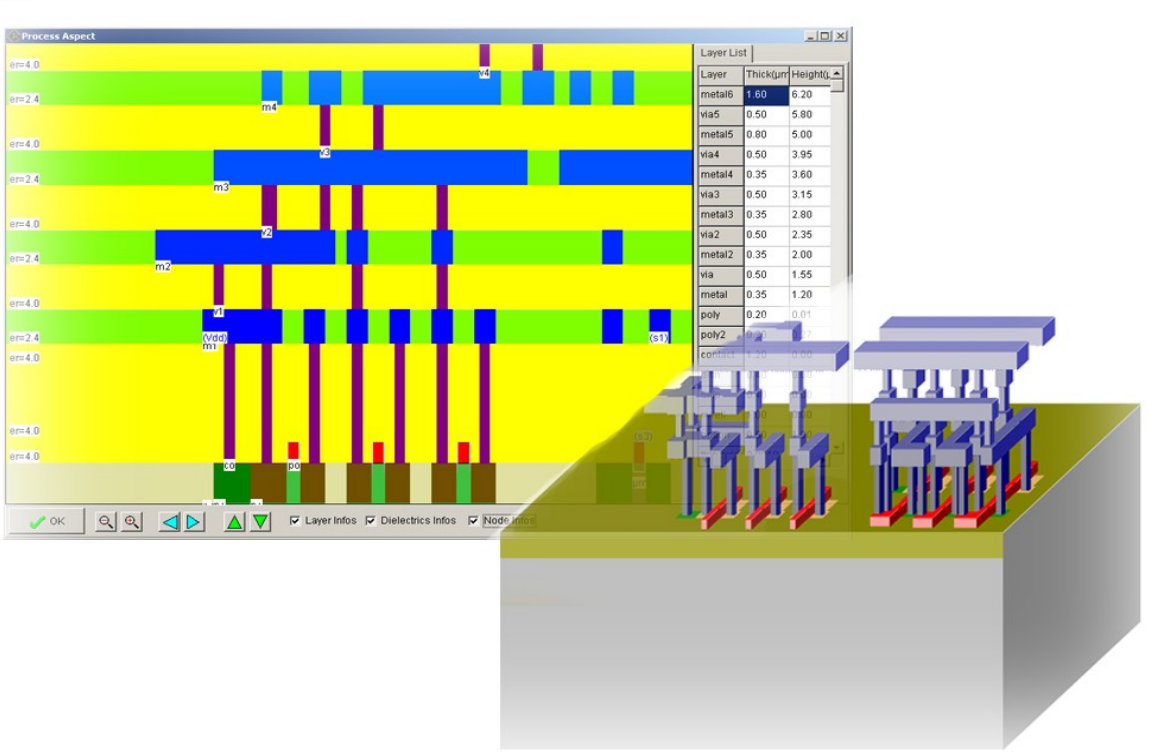

B
A
S
Y
$\overline{S}$

VirtuosoFab

Touch the deep submicron technology

- 3D fabrication process simulator with cross sectional viewer.
- Step-by-step 3-D visualization of fabrication for any portion of layout.





2D Cross Section

NMOS Transistor