NMOS & CMOS inverters and Gates
Lamda Base rule.
Topic Covered

- NMOS & CMOS INVERTER AND GATES:
  - NMOS & CMOS inverter – Determination of pull up / pull down ratios
  - Stick diagram – Lamda based rules – Super buffers – BiCMOS & steering logic
Stick Diagrams

- VLSI design aims to translate circuit concepts onto silicon
- Stick diagrams are a means of capturing topography and layer information - simple diagrams
- Stick diagrams convey layer information through color codes (or monochrome encoding)
<table>
<thead>
<tr>
<th>Stick Encoding</th>
<th>Layer</th>
<th>Mask Layout Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Thinox</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Polysilicon</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Metal1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Contact cut</td>
<td></td>
</tr>
<tr>
<td>NOT applicable</td>
<td>Overglass</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Implant</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Buried contact</td>
<td></td>
</tr>
<tr>
<td>Stick Encoding</td>
<td>Layer</td>
<td>Mask Layout Encoding</td>
</tr>
<tr>
<td>----------------</td>
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<td>----------------------</td>
</tr>
<tr>
<td><img src="image1" alt="Stick Encoding" /></td>
<td>P-Diffusion</td>
<td><img src="image2" alt="Mask Layout" /></td>
</tr>
<tr>
<td>Not Shown in Stick Diagram</td>
<td>P+ Mask</td>
<td><img src="image3" alt="Mask Layout" /></td>
</tr>
<tr>
<td><img src="image4" alt="Stick Encoding" /></td>
<td>Metl2</td>
<td><img src="image5" alt="Mask Layout" /></td>
</tr>
<tr>
<td><img src="image6" alt="Stick Encoding" /></td>
<td>VIA</td>
<td><img src="image7" alt="Mask Layout" /></td>
</tr>
<tr>
<td><img src="image8" alt="Stick Encoding" /></td>
<td>Demarcation Line</td>
<td></td>
</tr>
<tr>
<td><img src="image9" alt="Stick Encoding" /></td>
<td>P-Well</td>
<td><img src="image10" alt="Mask Layout" /></td>
</tr>
<tr>
<td><img src="image11" alt="Stick Encoding" /></td>
<td>Vdd or GND CONTACT</td>
<td></td>
</tr>
</tbody>
</table>
For reference: an nMOS Inverter coloured stick diagram

*Note the depletion mode device*

$V_{dd} = 5V$

$V_{in}$

$V_{out}$
Only metal and polysilicon can cross the dimarcation line.
Stick diagram -> CMOS transistor circuit

$V_{dd} = 5V$

$V_{in}$

$V_{out}$

$pMOS$

$nMOS$
All paths in all layers will be dimensioned in $\lambda$ units and subsequently $\lambda$ can be allocated an appropriate value compatible with the feature size of the fabrication process.
Minimum distance rules between device layers, e.g.,

- polysilicon ↔ metal
- metal ↔ metal
- diffusion ↔ diffusion and
- minimum layer overlaps are used during layout
nMOS transistor mask representation

gate

polysilicon

metal

Contact holes

diffusion (active region)

drain

source
Contact Cuts

- Three possible approaches –
  1. Poly to Metal
  2. Metal to Diffusion
  3. Buried contact (poly to diff) or butting contact (poly to diff using metal)
Minimize spared diffusion

Use minimum poly width ($2\lambda$)

- Minimize spared diffusion
- Use minimum poly width ($2\lambda$)

Width of contacts = $2\lambda$
- Multiply contacts
All device mask dimensions are based on multiples of $\lambda$, e.g., polysilicon minimum width = $2\lambda$. Minimum metal to metal spacing = $3\lambda$. 
Layout Design rules & Lambda ($\lambda$)
Layout Design rules & Lambda ($\lambda$)

- Same N and P alters symmetry

Width of pMOS should be twice the width of nMOS

- L min
- Wpmos=2 Wnmos
Lambda Based Design Rules

- Design rules based on single parameter, $\lambda$
- Simple for the designer
- Wide acceptance
- Provide feature size independent way of setting out mask
- Minimum feature size is defined as $2 \lambda$
- Used to preserve topological features on a chip
- Prevents shorting, opens, contacts from slipping out of area to be contacted
CMOS Inverter Mask Layout
MOS Layout Design

- CMOS IC are designed using stick diagrams.
- Different color codes for each layer.
- Lambda/micron grid.
CMOS AN2 (2 i/p AND gate) Mask Layout
nMOS Inverter coloured stick diagram

$V_{dd} = 5V$

*Note the depletion mode device*
Two-way selector with enable

E = 0
A = 0|1
1. Pull-down: Connect to ground if $A=1$ AND $B=1$

2. Pull-up: Connect to $V_{dd}$ if $A=0$ OR $B=0$
**Static CMOS NOR gate**

\[
\text{Out} = \overline{A + B}
\]

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>(A + B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

1. **Pull-down:** Connect to ground if \(A=1\) **OR** \(B=1\)

2. **Pull-up:** Connect to \(Vdd\) if \(A=0\) **AND** \(B=0\)
Static CMOS Design Example Layout

Example: \( f = a \cdot b + c \)
Layout 2 (Different layout style to previous but same function being implemented)

Example: \( f = \frac{a \cdot b + c}{ } \)
Complex logic gates layout

- $\text{Ex} \rightarrow F = AB + E + CD$
- Eulerpaths
- Circuit to graph (convert)
  1. Vertices are source/Drain connections
  2. Edges are transistors

- Find p and n Eulerpaths
F = (AB) + E + (CD)

EULER PATH = \{A, B, E, D, C\}
EULER PATH = \{A,B,E,D,C\}
VirtuosoFab

- 3D fabrication process simulator with cross sectional viewer.
- Step-by-step 3-D visualization of fabrication for any portion of layout.

Touch the deep submicron technology
2D Cross Section
NMOS Transistor

- Metal Layer
- Contacts
- Poly
- N Diffusion