

## Number System and Codes

- Q.1 Which of the following are analog quantities, and which are digital?  
(a) Number of atoms in a sample of material  
(b) Altitude of an aircraft  
(c) Pressure in a bicycle tire
- Q.2 Convert the following binary numbers to their equivalent decimal values.  
(a)  $11001_2 = \underline{\hspace{2cm}}_{10}$   
(b) 1001.1001  
(c) 10011011001.10110
- Q.3 Using 3 bits, show the binary counting sequence from 000 to 111.
- Q.4 What is the maximum number that we can count up to using 10 bits?
- Q.5 How many bits are needed to count up to a maximum of 511?
- Q.6 Suppose that the decimal integer values from 0 to 15 are to be transmitted.  
(a) How many lines will be needed if parallel representation is used?  
(b) How many will be needed if serial representation is used?
- Q.7 Convert these binary numbers to decimal.  
(a) 10110 (b) 1111010111  
(c) 10001101 (d) 10111111
- Q.8 Convert the following decimal values to binary.  
(a) 37 (b) 205  
(c) 511 (d) 2313
- Q.9 Convert each of the binary values from Q7 to octal.
- Q.10 Convert each of the binary values from Q7 to hex.
- Q.11 Convert each of the following decimal numbers to octal.  
(a) 59 (b) 65536  
(c) 255 (d) 919
- Q.12 Convert each of the following octal numbers to decimal.  
(a) 57 (b) 65536  
(c) 255 (d) 1004
- Q.13 Convert each of the octal values from Q12 to binary.
- Q.14 Convert each of the octal values from Q12 to hex.
- Q.15 List the octal numbers in sequence from  $165_8$  to  $200_8$ .
- Q.16 When a large decimal number is to be converted to binary, it is sometimes easier to convert it first to octal, and then from octal to binary. Try this Procedure for  $2313_{10}$ , compare it with the procedure used in Problem Q.7. (d) and comment.
- Q.17 Convert these hex values to decimal  
(a) 92 (b) 2C0  
(c) 1A6 (d) 7FF  
(d) 37FD
- Q.18 Convert each of the hex values from Q7 to binary.
- Q.19 Convert each of the hex values from Q7 to octal.
- Q.20 Convert these decimal values to hex.  
(a) 75 (d) 25,619  
(b) 314 (e) 4095  
(c) 2048

- Q.21 In most microcomputers the addresses of memory locations are specified in hexadecimal. These addresses are sequential numbers that identify each memory circuit.
- (a) A particular microcomputer can store an 8-bit number in each memory location. If the memory addresses range from  $0000_{16}$  to  $FFFF_{16}$ , how many memory locations are there?
- (b) Another microcomputer is specified to have 4096 memory locations. What range of hex addresses does this computer use?
- Q.22 List the hex numbers in sequence from 280 to 2A0.
- Q.23 Encode these decimal numbers in BCD
- (a) 47 (b) 1204  
(c) 187 (d) 962
- Q.24 How many bits are required to represent the decimal numbers in the range from 0 to 999 using straight binary code? Using BCD code?
- Q.25 The following numbers are in BCD. Convert them to decimal.
- (a) 1001011101010010 (b) 000110000100  
(c) 0111011101110101 (d) 010010010010
- Q.26 Represent the statement “X = 25/Y” in ASCII code (excluding quotes). Attach an even-parity bit.
- Q.27 Attach an event-parity bit to each of the ASCII codes for Q19 and give the result in hex.
- Q.28 The following code groups are being transmitted. Attach an *even* – parity bit to each group.
- (a) 10110110  
(b) 00101000  
(c) 11110111
- Q.29 Convert the following decimal numbers to BCD code and then attach an *odd* - parity bit.
- (d) 74 (c) 165  
(e) 34 (d) 9201
- Q.30 In certain digital system, the decimal numbers from 000 through 999 are represented in BCD code. An *odd*-parity bit is also included at the end of each group. Examine each of the code groups below and assume that each one has just been transferred from one location to another. Some of the groups contain errors. Assume that *no more than* two errors have occurred for each group. Determine which of the code groups have a single error and which of them *definitely* have a double error. (*Hint*: Remember that this is a BCD code.)
- (f) 1001010110000  
(b) 0100011101100  
(c) 0111110000011  
(d) 1000011000101

## Binary Algebra

- Q 1. Add the following in binary. Check result by doing addition in decimal.
- (a)  $1010 + 1011$
  - (b)  $111 + 0011$
  - (c)  $1011.1101 + 11.1$
  - (d)  $0.1011 + 0.1111$
  - (e)  $10011011 + 10011101$
- Q 2. Represent each of the following signed decimal numbers in the 2's complement system. Use a total of 8 bits including sign bit.
- (a) +32
  - (b) -14
  - (c) +63
  - (e) -1
  - (f) -128
  - (g) +169
- Q 3. Each of the following numbers represents a signed decimal number in the 2's complement system. Determine the decimal value in each case.
- (a) 01101
  - (b) 11101
  - (c) 01111011
  - (d) 10011001
  - (e) 0111111
  - (f) 100000
  - (g) 111111
  - (h) 1000001
- Q 4. (a) What range of signed decimal values can be represented using 12 bits including sign bit?  
(b) How many bits would be required to represent decimal numbers from -32,768 to +32,767?
- Q 5. List, in order, all of the signed numbers that can be represented in 5 bits using the 2's complement system.
- Q 6. Represent each of the following decimal values as 5 bit signed binary values. Then negate each one.
- (a) +7
  - (b) -12
  - (c) +15
  - (d) -1
- Q 7. What is the range of unsigned decimal values that can be represented in 10 bits? What is the range of signed decimal values using the same number of bits?
- Q 8. The reason why the sign –magnitude method for representing signed numbers is not used in most computers can readily be illustrated by performing the following.
- (a) Represent +12 in 5 bits using the sign –magnitude form.
  - (b) Represent -12 in 5 bits using the sign –magnitude form.
  - (c) Add the two binary numbers and note that the sum does not look anything like zero.
- Q 9. Perform the following operations in the 2's complement system. Use 8 bits (including sign bit) for each number. Check your results by converting the binary result back to decimal
- a. Add +9 to +6.
  - b. Add +14 to -17.
  - c. Add +19 to -24.
  - d. Add -48 to -80.
  - e. Subtract +16 from +17.

- f. Subtract +21 from -13.
- g. Subtract -36 from -15.
- h. Add +17 to -17.
- i. Subtract -17 from -17.

- Q 10. Perform the following operations in the 2's complement system. Use 8 bits (including sign bit) for each number. Show that overflow occurs in each case
- a. Add +9 to +6.
  - b. Add +14 to -17.

- Q 11. Multiply the following pairs of binary numbers and check by doing multiplication in decimal.
- (a) 111 x 101
  - (b) 1011 x 1011
  - (c) 101.101 x 110.010
  - (d) .1101x .1011

- Q 12. Perform the divisions. Check the results by doing division in decimal.
- (a) 1100 ÷ 100
  - (b) 111111 ÷ 1001
  - (c) 10111 ÷ 100
  - (d) 10110.1101 ÷ 1.1

- Q 13. Add the following decimal numbers after converting each to its BCD code
- |             |               |
|-------------|---------------|
| (a) 74 + 23 | (c) 147 + 380 |
| (b) 58 + 37 | (d) 385 + 118 |

- Q 14. Find the sum of each of the following pairs of hex numbers.
- (a) 3E91 + 2f93
  - (b) 91B + 6F2
  - (c) ABC + DEF

- Q 15. Perform the following subtractions on the pairs of hex numbers.
- (a) 3E91 - 2F93
  - (b) 91B - 6F2
  - (c) F000 - .EFFF

- Q 16. The owner's manual for a certain personal computer states that the computer has usable memory locations at the following hex addresses: 0200 through 03FF, and 4000 through 7FD0. What is the total number of available memory locations?

- Q 17. In working with microcomputers it is often necessary to move binary numbers from an 8-bit register to a 16 bit register. Consider the numbers 01001001 and 10101110, which represent +73 and -82, respectively, in the 2's-complement system. Determine the 16-bit representations for these decimal numbers.

- Q 18. Read the statement below concerning an OR gate. At first they may appear to be valid, but after some thought you should realize that neither one is *always* true. Prove this by showing example to refute each statement.
- (a) If the output waveform from an OR gate is the same as the waveform at one of its inputs, the other input is being held permanently LOW.
  - (b) If the output waveform from an OR gate is always HIGH, one of the inputs is being held permanently HIGH.
- Q 19. How many different sets of input conditions will produce a HIGH output from a five-Input OR gate?
- Q 20. For each of the following expression, construct the corresponding logic circuit, using AND and OR gates and INVERTERS.
- (a)  $x = \overline{AB(C+D)}$
  - (b)  $z = \overline{(A+B+\overline{CDE})} + \overline{BCD}$
  - (c)  $y = \overline{(M+N+\overline{PQ})}$
  - (d)  $x = \overline{(W+PQ)}$
  - (e)  $z = MN(P + \overline{N})$

Q 21. Apply the input waveforms of figure 3-47 to a NOR gate and draw the output waveform.

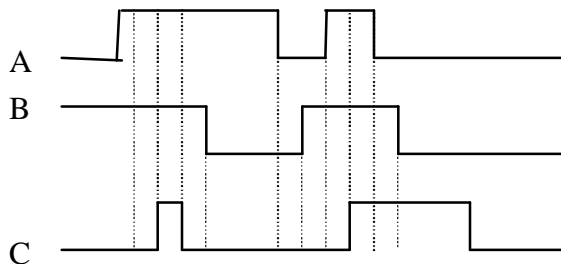
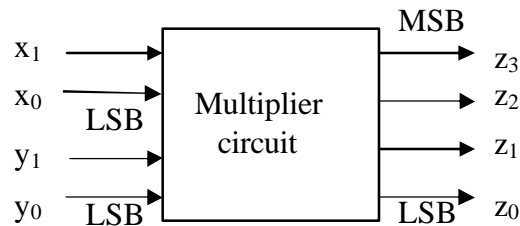


Figure 3.47

- Q 22. Repeat Q 21 with the C input held permanently LOW. Then repeat for C held Permanently HIGH.
- Q 23. Repeat Q 21 for a NAND gate.
- Q 24. Repeat Q 22 for a NAND gate.
- Q 25. Modify the circuit that were constructed in Q 20 so that only NAND gates and NOR gates are used.

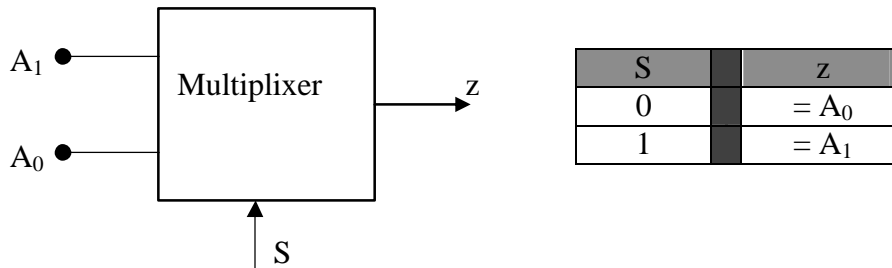
## Combinational Logic Circuit

- Q 1. Write the truth table for a half adder (inputs A and B; outputs Sum and Carry). From the truth table design a logic circuit that will act as a half adder.
- Q 2. Define each of the following terms.
- (a) Full adder
  - (b) 2's – complement
  - (c) Arithmetic-logic unit
  - (d) Sign bit
  - (e) Overflow
  - (f) Accumulator
  - (g) Parallel adder
  - (h) Look-ahead carry
  - (i) Negation
  - (j) B-register
- Q 4. Figure 4-49 represents a multiplier circuit that takes 2-bit binary numbers  $x_1, x_0$  and  $y_1, y_0$  and produces an output binary number  $z_3, z_2, z_1, z_0$  that is equal to the arithmetic product of the two input numbers. Design the logic circuit for the multiplier. (Hint :The logic circuit will have four inputs and four outputs)



**Figure 4.49**

- Q 5. Design a logic circuit that has two signal inputs  $A_1$  and  $A_0$  and a control input  $S$  so that it functions according to the requirements given in Figure 4-51. This type of circuit is called a multiplexer.



**Figure 4-51**

- Q 6. Figure 4-48 represents a relative magnitude detector that takes two 3 bit binary numbers  $x_2, x_1, x_0$  and  $y_2, y_1, y_0$  and determines whether they are equal and, if not, which one is larger. There are three outputs, defined as follows:

1.  $M = 1$  only if the two input numbers are equal.
2.  $N = 1$  only if  $x_2x_1x_0$  is greater than  $y_2y_1y_0$ .
3.  $P = 1$  only if  $y_2y_1y_0$  is greater than  $x_2x_1x_0$ .

Design the logic circuitry for this detector. The circuit has six inputs and three outputs and is therefore much too complex to handle using the truth-table approach.

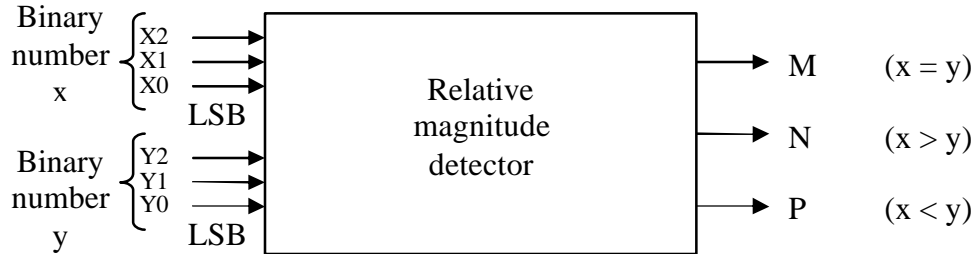


Figure 4-48

Q 7. Determine the input conditions needed to produce  $x=1$  in figure 4.47.

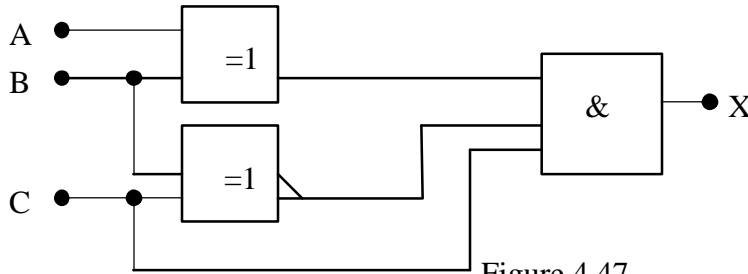


Figure 4.47

Q 8. Simply the following expressions using Boolean algebra.

- (a)  $x = ABC + \bar{A}C$
- (b)  $y = (Q + R)(\bar{Q} + \bar{R})$
- (c)  $w = ABC + \bar{A}\bar{B}C + \bar{A}$
- (d)  $q = \overline{RST(R + S + T)}$
- (e)  $x = \bar{A}\bar{B}\bar{C} + \bar{A}BC + ABC + A\bar{B}\bar{C} + A\bar{B}C$
- (f)  $z = (B + \bar{C})(\bar{B} + C) + \bar{A} + B + \bar{C}$
- (g)  $y = \overline{(C + D)} + \bar{A}C\bar{D} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C\bar{D} + AC\bar{D}$

Q 9. Simplify the circuit of Figure 4.41 using Boolean algebra.

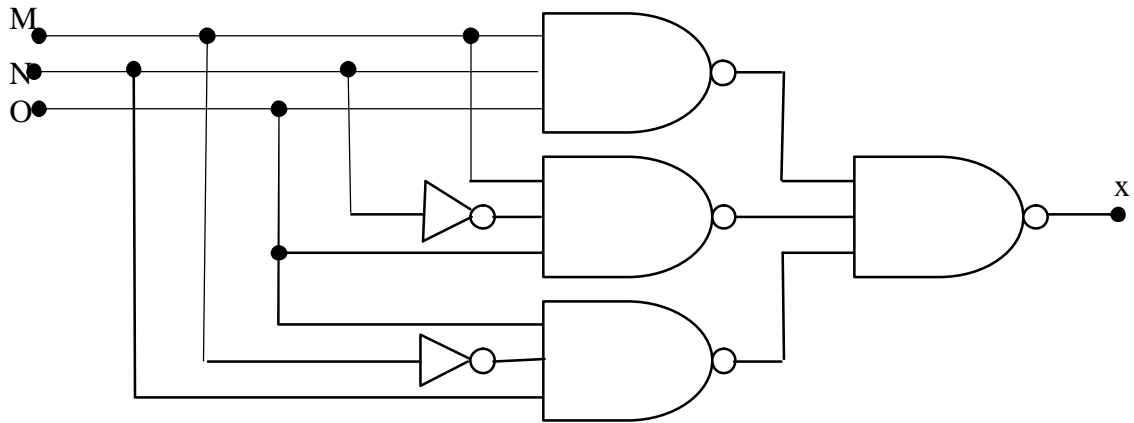


Figure 4.41

- Q 10. Change each NAND gate in Q 9 to a NOR gate and simplify the circuit using Boolean algebra.
- Q 11. Design the logic circuit corresponding the truth table shown in Table 4-8.

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 4.8

- Q 12. Design a logic circuit whose output is HIGH *only* when a majority of inputs  $A$ ,  $B$  and  $C$  are LOW.
- Q 13. Three photocells are being illuminated by three different flashing lights. The lights are supposed to be flashing in sequence so that at no time should all three lights be on at the same time or off at the same time. Each photocell is used to monitor one of the lights, and each photocell is in a circuit that produces a LOW output voltage when the photocell is dark and a HIGH output voltage when the photocell is illuminated. Design a logic circuit that has as its inputs the photocell circuit outputs and which produces a HIGH output whenever the three lights are all *on* or all *off* at the same time .
- Q 14. A 4-bit binary number represented as  $A_3 A_2 A_1 A_0$ , where  $A_3 A_2 A_1$ , and  $A_0$  represent the individual bits with  $A_0$  equal to the LSB. Design a logic circuit that will produce a HIGH output whenever the binary number is greater than 0010 and less than 1000.
- Q 15. Implement the circuit of Q 11 using all NAND gates.



- Q 16. Implement the circuit of **Q 12** using all NAND gates.
- Q 17. Implement the expression  $z = D + ABC + AC$  using ANDs, ORs, and INVERTERS; then convert to all NAND gates.
- Q 18. Simplify the expression of **Q 8(e)** using the K map.
- Q 19. Simplify the expression of **Q 8(g)** using the K map.
- Q 20. Simplify the expression of **Q 14** using the K map.
- Q 21. Redo **Q 13** using EX-OR or EX-NOR gates and one other gate.
- Q 22. Design a logic circuit that will allow input signal A to pass through to the output only when control input B is LOW while control input C is High otherwise, the output is LOW.
- Q 23. Design a circuit that will inhibit the passage of an input signal only when control inputs B, C and D are all HIGH; the output is to be HIGH in the inhibited condition.
- Q 24. Design a logic circuit that controls the passages of a signal A according to the following requirements:
2. Output X will equal A when control inputs B and C are the same.
  3. X will remain HIGH when B and C are different.
- Q 25. Determine the minimum expression for each K map in Figure 4-43 .

	C'D	C'	C	CD
A'B	1	1	1	1
A'B	1	1	0	0
AB	0	0	0	1
AB'	0	0	1	1

(a)

	C'D	C'	C	CD
A'B	1	0	1	1
A'B	1	0	0	1
AB	0	0	0	0
AB'	1	0	1	1

(b)

	C'	C
A'B	1	1
A'B	0	0
AB	1	0
AB'	1	X

(c)

**Figure 4-43**

- Q 26. A full adder can be implemented in many different ways. Figure 6-20 shows how one may be constructed from two half adders. Construct a truth table for this arrangement and verify that it operates as a FA.

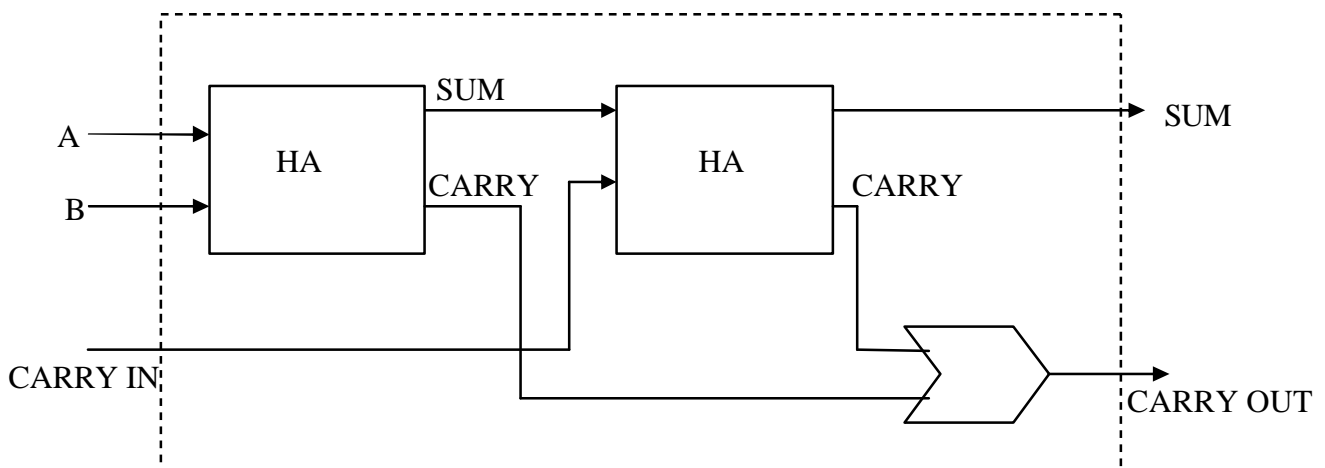


Figure 6-20

Full adder

## Sequential Logic Circuits

- Q 1. An 8-MHz square wave clocks a 5-bits ripple counter. What is the frequency of the last FF? What is the duty cycle of this output waveform?
- Q 2. Repeat the above problem if the input has a 20percent duty cycle.
- Q 3. Assume that the 5-bit binary counter starts in the 00000 state. What will be the count after 144 input pulses?
- Q 4. Use J-K flip-flops and any other necessary logic to construct a MOD-24 a synchronous counter.
- Q 5. Show how a 74293 counter can be used to produce a 1.2-kpps output from an 18-kpps input.
- Q 6. Show how two 74293s can be connected to divide an input frequency by 60 while producing a symmetrical square-wave output.
- Q 7. (a) Draw the diagram for a MOD-16 down counter.  
(b) Construct the state transition diagram.  
(c) If the counter is initially in the 0110 state, what state will it be in after 37 clock pulses?
- Q 8. A 4-bit ripple counter is driven by a 20-MHz clock signal. Draw the wave-forms at the output of each FF if each FF has  $t_{pd} = 20\text{ns}$ . Determine which counter states, if any, will not occur because of the propagation delays.
- Q 9. (a) What is the maximum clock frequency that can be used with the counter of problem 8?  
(b) What could  $f_{\max}$  be if the counter were expanded to 6 bits?
- Q 10. (a) Draw the circuit diagram for a MOD-64 parallel counter.  
(b) Determine  $f_{\max}$  for this counter if each FF has  $t_{pd} = 20\text{ ns}$  and each gate has  $t_{pd} = 10\text{ns}$ .
- Q 11. Show how to connect two 74193s to form an 8-bit counter that divides the clock frequency by 100. Use the  $\overline{TC}_D$  output of one 74193 stage as the clock for second 74193 stage. Connect the parallel data inputs so that the combined counter presets at  $100_{10}$ . Note that the counter is to be preset when both stages are simultaneously at their end counts.
- Q 12. (a) Design a synchronous counter that has the following sequence: 000, 010, 101, 110, and repeat . The undesired (unused) states 001, 011, 100 and 111 must always go to 000 on the next CLOCK pulse.  
(b) Redesign the counter of part (a) without any requirement on the unused states; that is, their NEXT states can be don't cares. Compare with the design from (a).
- Q 13. Draw the diagram for a 5-bit ring counter using J-K flip-flops.
- Q 14. Draw the diagram for a MOD – 10 Johnson counter using J-K flip-flops and determine its counting sequence. Draw the decoding circuit needed to decode each of the 10 states. This is not a BCD counter.
- Q 15. Show how to connect two 74178a as an 8-bit ring counter.
- Q 16. A certain clocked FF has minimum  $t_s = 20\text{ ns}$  and  $t_h = 5\text{ ns}$ . How long must the control inputs be stable prior to the active clock transition?

- Q 17. Draw a circuit diagram for the synchronous parallel transfer of data from one 3-bit register to another using J-K flip-flops.
- Q 18. (a) How many FFs are required to build a binary counter circuit that counts from 0 to 1023?  
 (b) Determine the frequency at the output of the last FF of this counter for a ninput clock frequency of 2MHz.  
 (c) What is the counter's MOD number?  
 (d) If the counter is initially at zero, what count will it hold after 2060 pulses?
- Q 19. A certain counter is being pulsed by a 256-KHz clock signal. The output frequency from the last FF is 2MHz.  
 (a) Determine the MOD number.  
 (b) Determine the counting range.
- Q 20. A photodetector circuit is being used to generate a pulse each time a customer walks into a certain establishment. The pulses are fed to an 8-bit counter. The counter is used to count these pulses as a means for determining how many customers have entered the store. After closing the store, the proprietor checks the counter and finds that it shows a count of  $00001001_2 = 9_{10}$ . He knows that this is incorrect, because there were many more than nine people in his store. Assuming that the counter circuit is working properly, what could be the reason for the discrepancy?
- Q 21. Draw the state transition diagram for a MOD-16 counter.
- Q 22. Show how to use a 74LS14 Schmitt-trigger INVERTER to produce an approximate square wave with a frequency of 10 kHz.
- Q 23. Design a 555 free-running oscillator to produce an approximate square wave at 40 kHz. C should be kept at 100 pF or greater.
- Q 24. Assuming that  $Q = 0$  initially, apply the  $x$  and  $y$  waveforms of figure 5.68 to the SET and CLEAR inputs of a NAND latch and determine the  $Q$  and  $\bar{Q}$  waveforms.
- Q 25. Invert the  $x$  and  $y$  waveforms of Figure 5-68, apply them to the SET and CLEAR inputs of a NOR latch, and determine the  $Q$  and  $\bar{Q}$  waveforms. Assume that  $Q = 0$  initially.

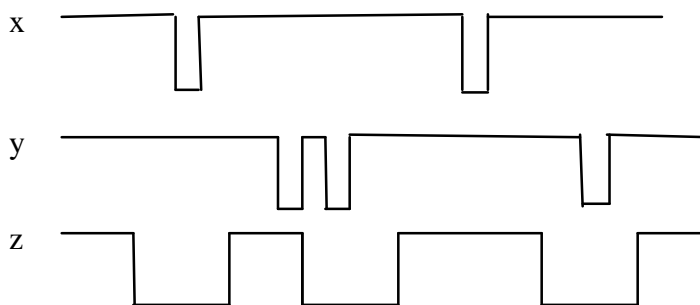
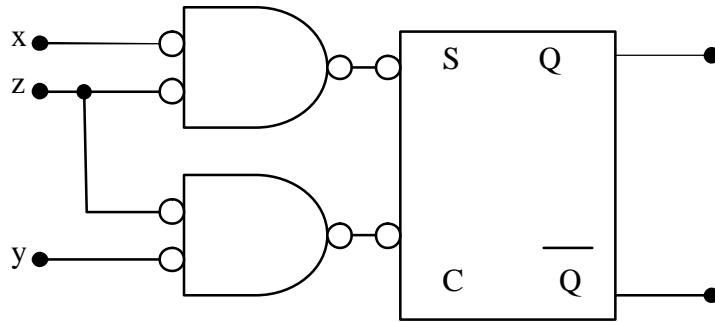


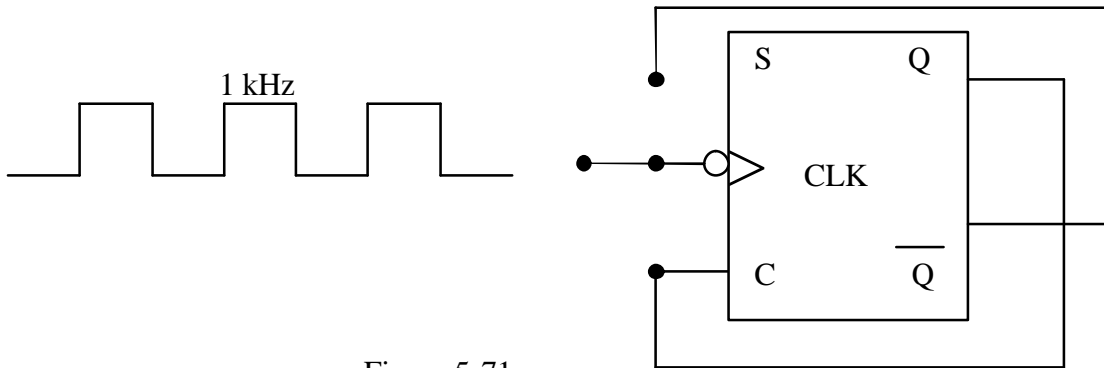
figure 5.68

- Q 26. The waveforms of Figure 5-68 are connected to the circuit of Figure 5-69. Assume that  $Q = 0$  initially, and determine the  $Q$  waveform.



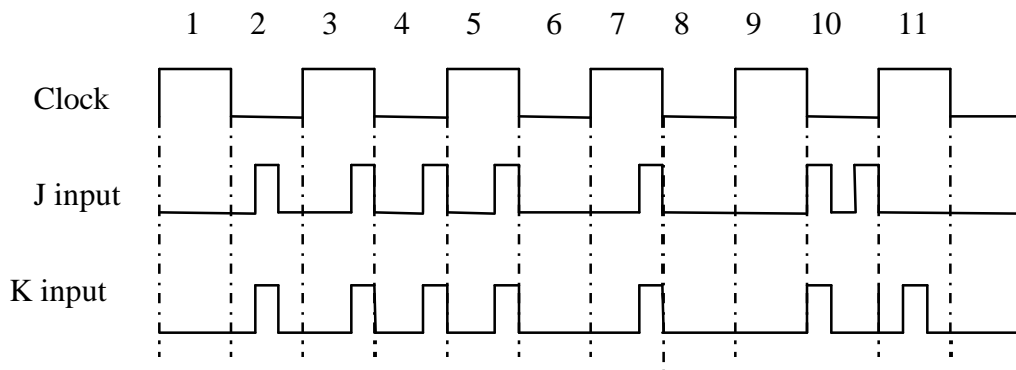
**Figure 5-69**

- Q 27. A *toggle* FF is one that has a single input and operated in such a way that the FF output changes state for each pulse applied to its input. The clocked S-C flip-flop can be wired to operate in the toggle mode, as shown in figure 5-71. The waveform applied to the *CLK* input is a 1 – kHz Square wave. Verify that this arrangement operates in the toggle mode; then determine the  $Q$  output waveform. Assume that  $Q = 0$  initially.



**Figure 5-71**

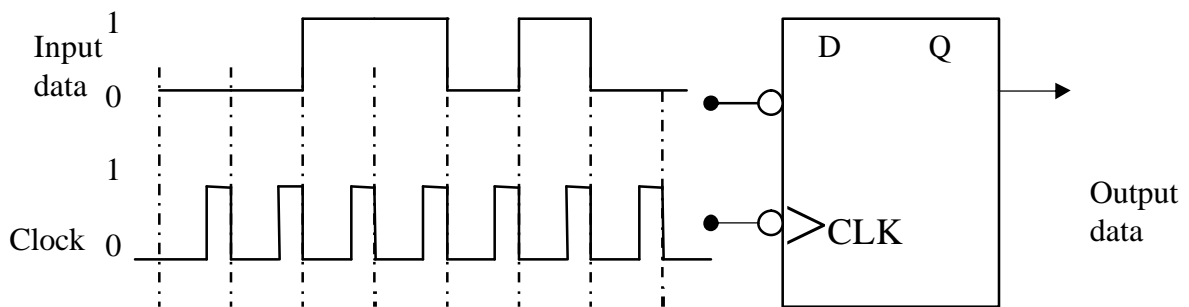
- Q 28. The waveforms shown in figure 5-72 are to be applied to two different FFs: (a) positive –edge-triggered K-K; (b) negative –edge-triggered J-K. Draw the  $Q$  waveform response for each of these FFs, assuming that  $Q = 0$  initially . Assume that each FF has  $T_h = 0$ .



**Figure 5-72**

Q 29.

A D FF is sometimes used to *delay* a binary waveform so that the binary information appears at the input. (a) Determine the Q waveform in Figure 5-73 and compare it with the waveform. Note that it is delayed from the input by one clock period. (b) How can a delay of two clock periods be obtained?



**Figure 5-73**

\* Assume  $t_H(\min) = 0$

Q 30. An edge-triggered D flip-flop can be made to operate in the toggle mode by connecting it as in Figure 5-74. Assume that  $Q = 0$  initially and determine the Q waveform.

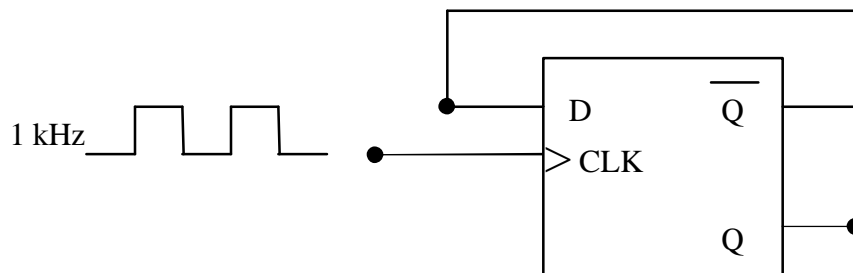


Figure 5-74 D flip-flop connected toggle.

Q 31. Compare the operation of the D latch with a negative –edge –triggered D flip-flop by applying the waveforms of Figure 5-75 to each and determining the Q waveforms.

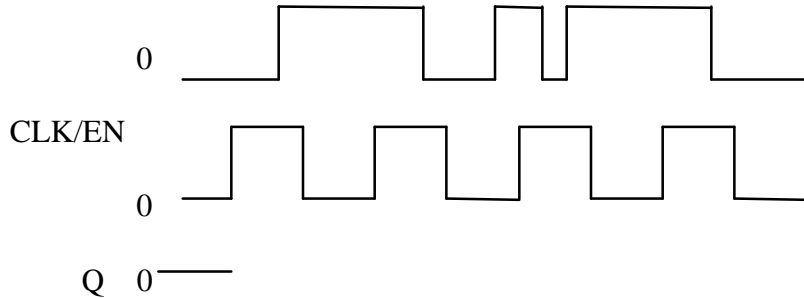


Figure 5-75

Q 32.

Determine the Q waveform for the FF in figure 5-76. Assume that  $Q = 0$  initially and remember that the asynchronous inputs override all other inputs

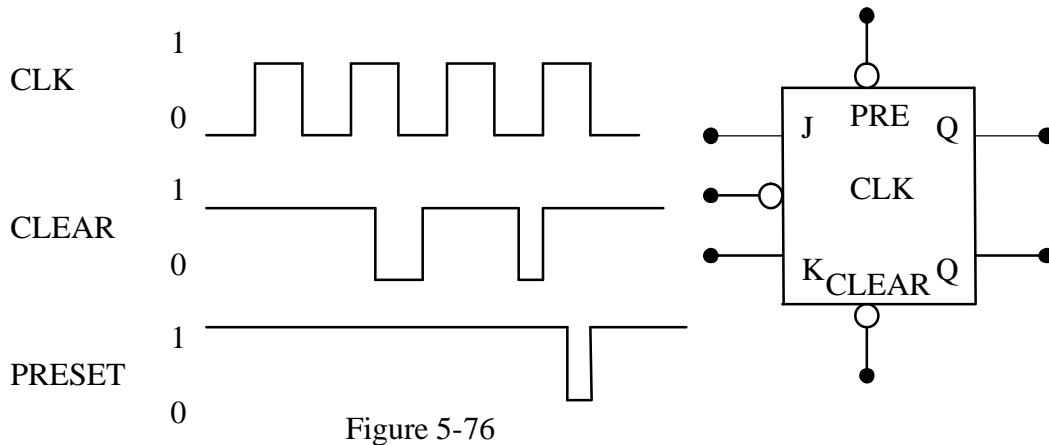


Figure 5-76

Q 33. A 555 oscillator can be combined with a J-K flip-flop to produce a perfect (50 percent duty cycle) square wave. Modify the circuit of Q 23 to include J-K flip-flop. The final output is still to be a 40 kHz square wave.

Q 34. Determine the frequency of the pulses at points w, x, y and z in the circuit of Figure 7.65.

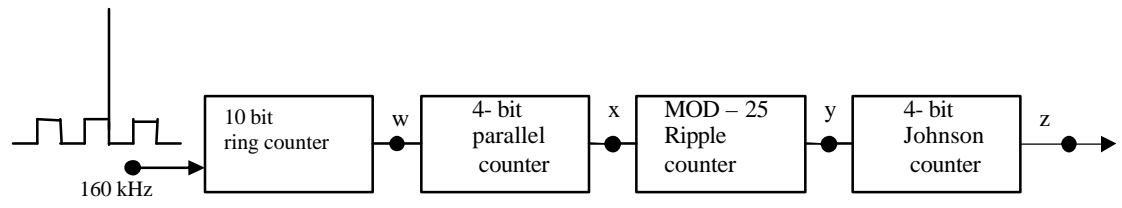


Figure 7-65

## Logic Families

- Q 1. A certain logic family has the following voltage parameters:  
 $V_{IH}(\min) = 3.5$        $V_{IL}(\max) = 1.0$  V  
 $V_{OH}(\min) = 4.9$        $V_{OL}(\max) = 0.1$  V
- (a) What is the largest positive-going noise spike that can be tolerated?  
(b) What is the largest negative-going noise spike that can be tolerated?
- Q 2. A digital gate has an input voltage  $V_{CC}$  equal to 5V. The input current is 2mA for high output and 3.4mA for low output. Find the power dissipated for 50% duty cycle.
- Q 3. A NOT gate has  $V_{IL} = 0.8$ V,  $V_{IH} = 2.5$ V,  $V_{OL} = 0.4$ V,  $V_{OH} = 3.6$ V. If two such gates are cascaded find the low and high noise margins.
- Q 4. A 5V battery has an internal resistance of 100 ohms. It is supplying N identical gates each having an input resistance of 3000ohms. The gates are in parallel. The minimum voltage at each should not fall below 3.5V. Find N.
- Q 5. (a) Does a TTL output act as current sink or current source in Low state?  
(b) IN which TTL input state is the input current largest?
- Q 6. What are the advantages and disadvantages of totem pole output?
- Q 7. What is meant by Unit Load (UL)?
- Q 8. An IC has  $I_{IL} = 0.8$  mA and  $I_{IH} = 10$   $\mu$ A. Express the input currents in UL.
- Q 9. Why is open collector output generally slower than totem pole output?
- Q 10 Name the three output states of tristate IC. In which state is it disabled?
- Q 11. When two or more tristate outputs tied to a common bus are enabled together it is called bus connection.
- Q 12. (a) How is high speed operation possible in ECL Gates?  
(b) Is it true that ECL gates usually have complementary outputs.  
(c) Can ECL be easily used with TTL?  
(d) Which has higher noise margin ECL or TTL?
- Q 13. What is high density IC? What are its advantages? What are disadvantages?
- Q 14. What is the difference between current surcing and current sinking?
- Q 15. What is the function of R/W input?
- Q 16. What is the function of Memory ENABLE input?
- Q 17. List the actions which occur when CPU reads from memory.
- Q 18. List the actions which occur when CPU writes into memory.
- Q 19. Describe the internal structure of ROM for storing 4k bytes and having a square register array.
- Q 20. Briefly describe the function of row select decoder, column select decoder and output buffer in a ROM.
- Q 21. What is the difference between MROM and PROM.
- Q 22. What is the difference between EPROM and EEPROM? What are the advantages for EEPROM over EPROM? What are disadvantages of EEPROM?
- Q 23. Discuss some applications of ROMs.
- Q24. (a) Which RAM uses flip flops?  
(b) Which RAM uses Capacitors?
- Q 25. Disadvantages of DRAM over Static RAM.
- Q 26. The capacity of 2K x 16 PROM is to be expanded to 16k x 16. Find the number of PROM chips required and the number of address lines in the expanded memory.



- Q 27. What is data rate buffer?
- Q 28. Differentiate between ROM and RAM.
- Q 29. What is magnetic core memory?
- Q 30. Name some secondary memory devices

### **Semiconductor Memories**

- Q 1. A certain memory has a capacity of 16K X 32. How many words does it store? What is the number of bits per word? How many memory cells does it contain?
- Q 2. How many different addresses are required by the memory of Problem 1?
- Q 3. What is the capacity of a memory that has 16 address inputs, four data inputs, and four data outputs?
- Q 4. A certain memory stores 8K sixteen-bit words. How many data input and data output lines does it have? How many address lines does it have? What is its capacity in bytes?