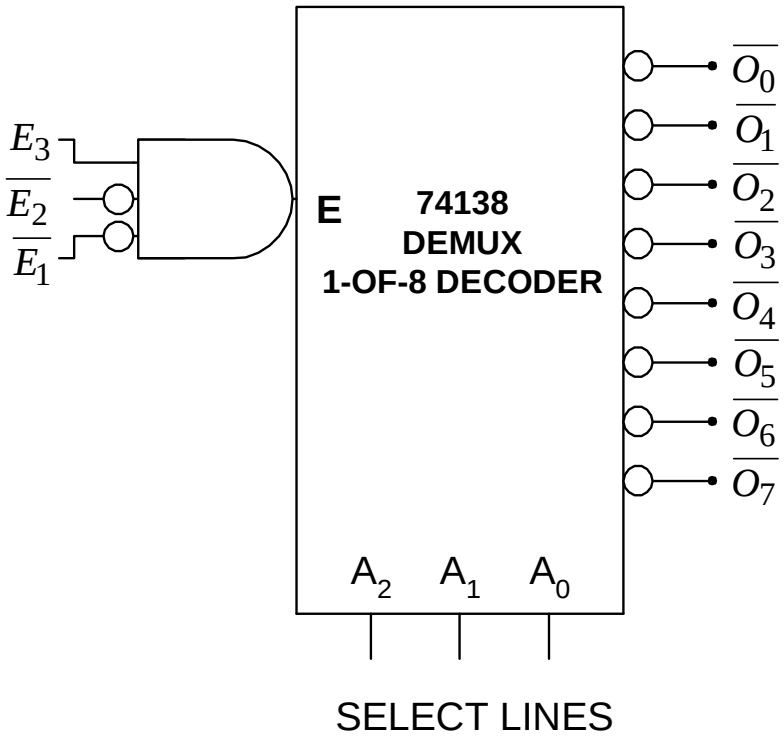
Lecture 17:
DEMULTIPLEXER

DEMULTIPLEXER LOGIC DIAGRAM

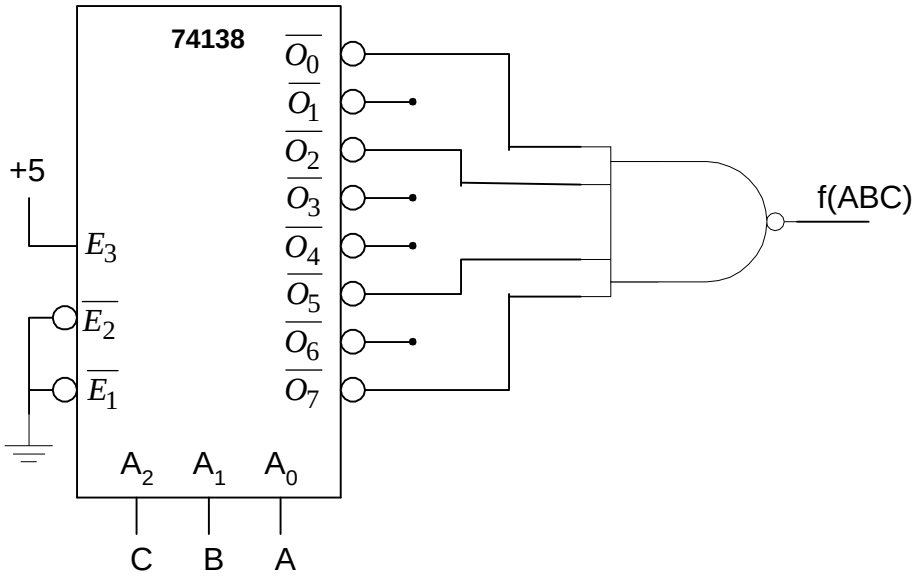
- Logic circuit that depending on the status of its select inputs will funnel its data input to one of several data outputs.

- Separate enable inputs (useful for cascading decoders) into AND gate which must be high to enable the decoder outputs.



$\overline{E_1}$	$\overline{E_2}$	E_3	*OUTPUTS*
0	0	1	RESPOND TO INPUT CODE A2A1A0
1	X	X	DISABLED –ALL HIGH
X	1	X	DISABLED –ALL HIGH
X	X	0	DISABLED –ALL HIGH

LOGIC FUNCTION GENERATION



A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

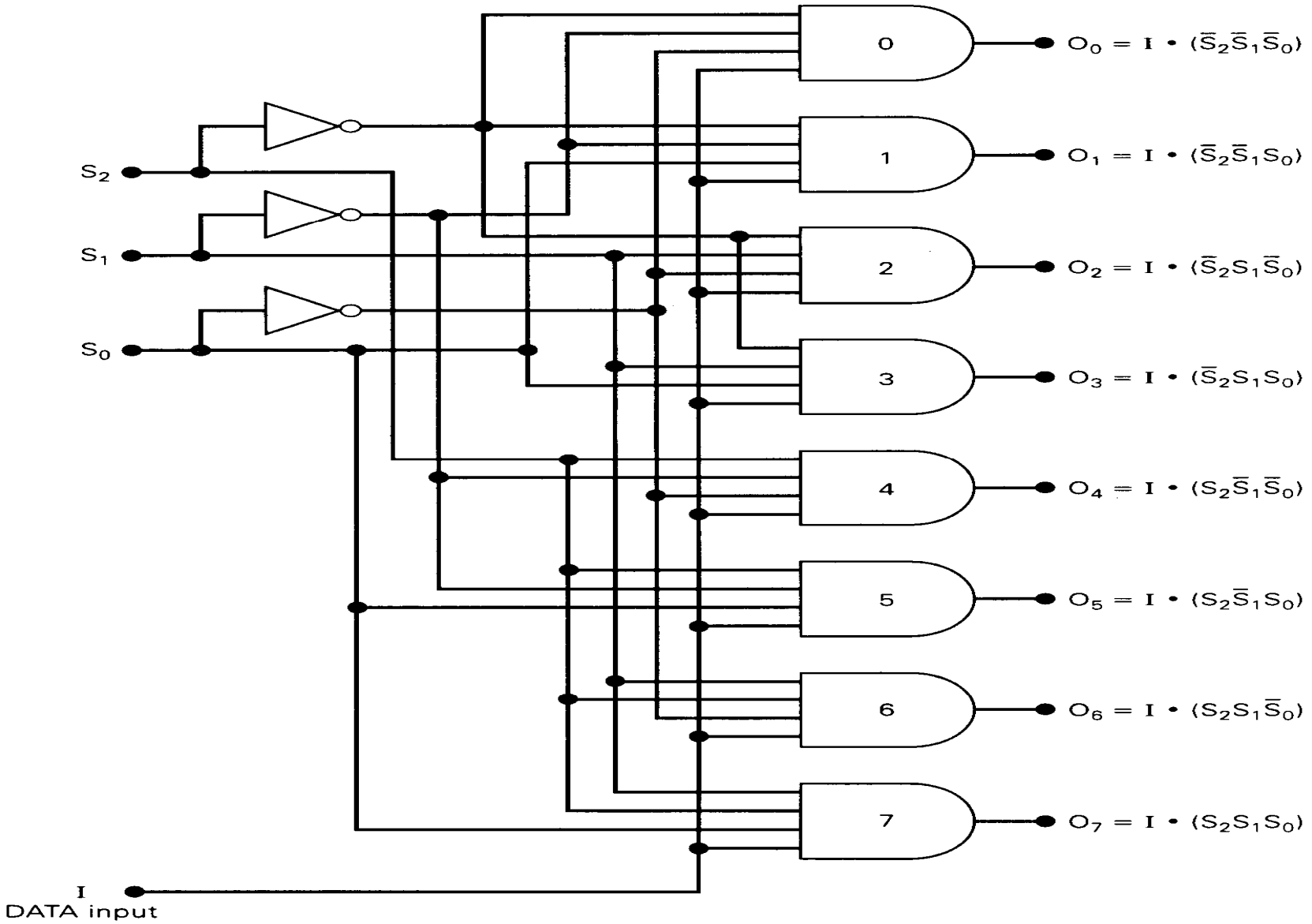
C	B	A	f
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

NAND- any low in gives a high out

DEMULTIPLEXER

SELECT code			OUTPUTS							
S_2	S_1	S_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0	0	I
0	0	1	0	0	0	0	0	0	I	0
0	1	0	0	0	0	0	0	I	0	0
0	1	1	0	0	0	0	I	0	0	0
1	0	0	0	0	0	I	0	0	0	0
1	0	1	0	0	I	0	0	0	0	0
1	1	0	0	I	0	0	0	0	0	0
1	1	1	I	0	0	0	0	0	0	0

DEMULTIPLEXER



PROJECT: A SECURITY MONITORING SYSTEM