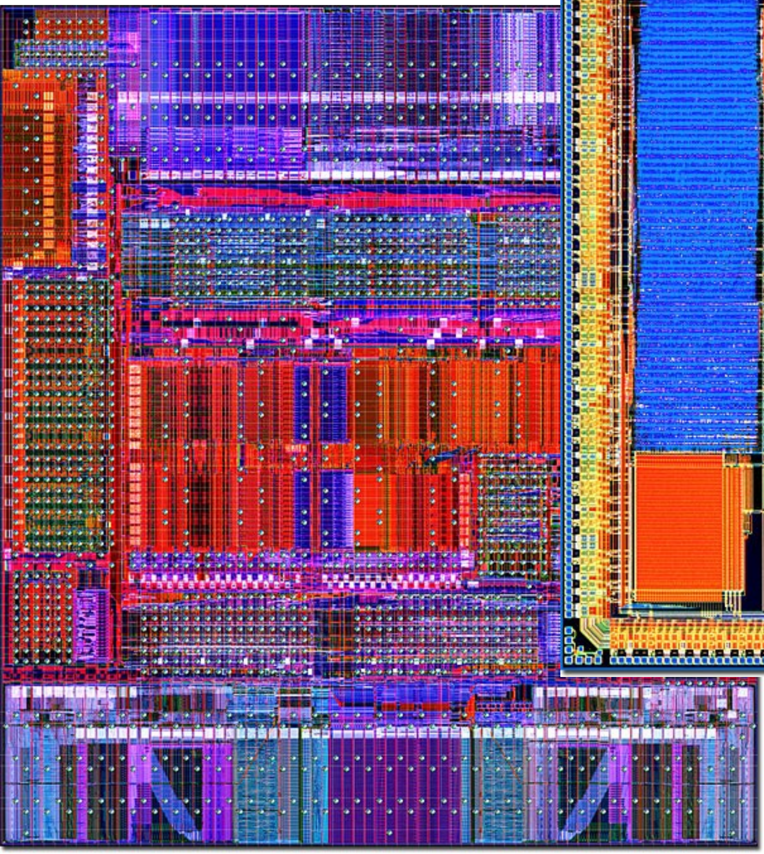
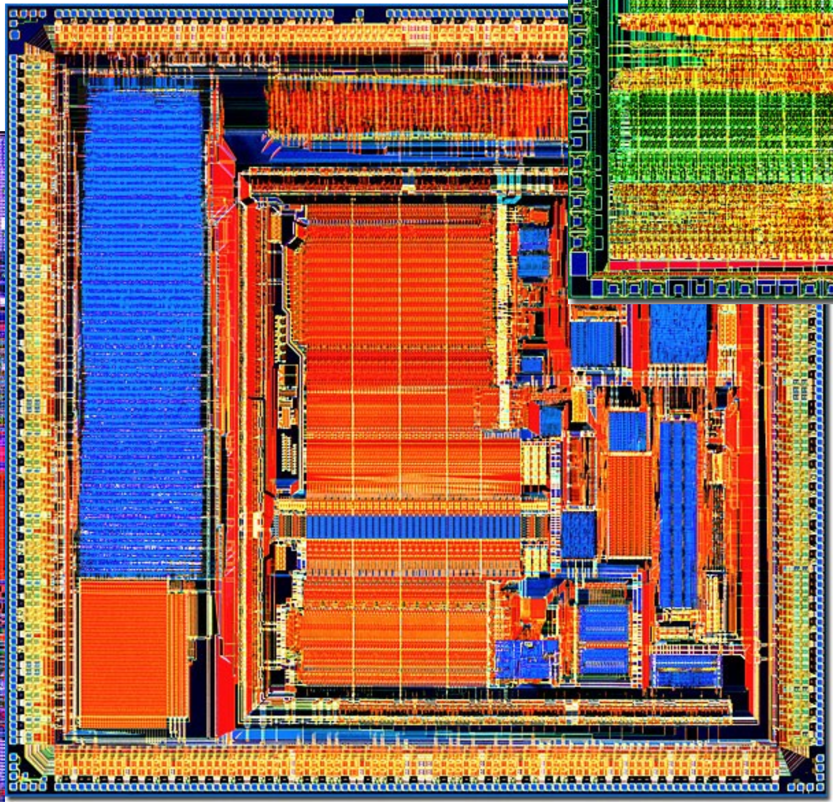
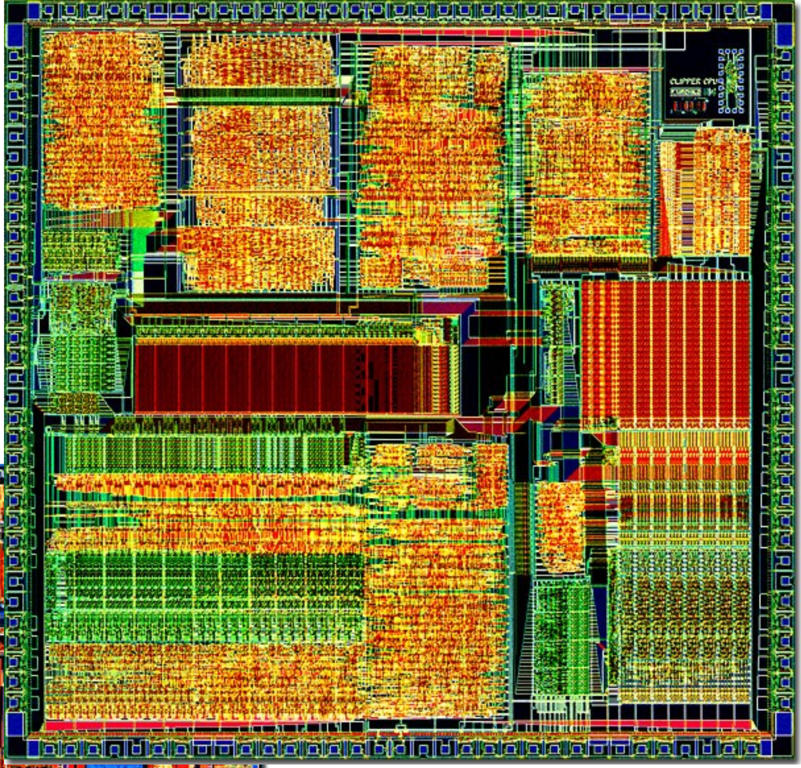
Field Effect Transistors Circuit Analysis

HP PA8000

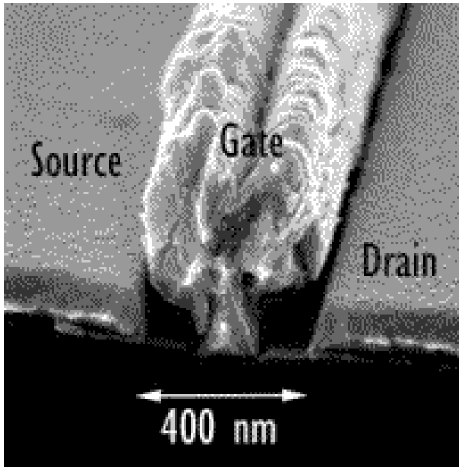




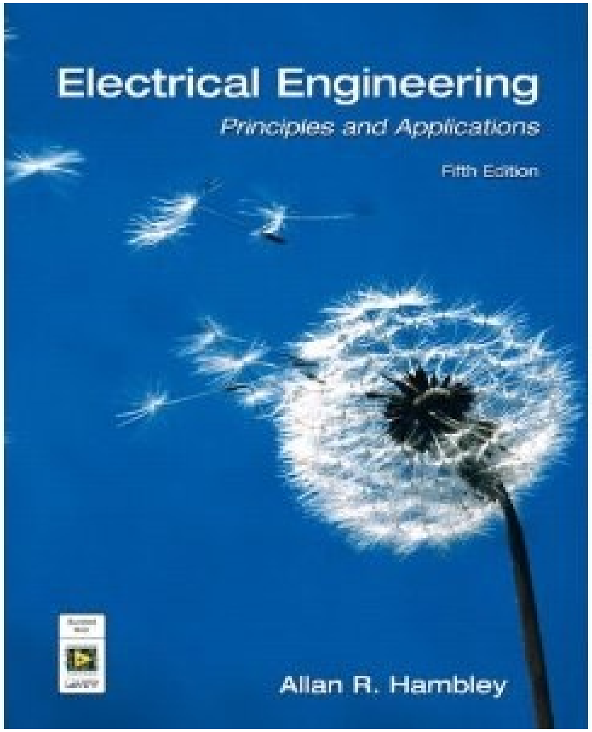
Fujitsu 68903



Fairchild Clipper C100



FET Circuit Analysis



Chapter 12: Field Effect Transistors

1. *MOS Small Signal Equivalent*
2. *Transconductance*
3. *Common-Source Amplifiers*
4. *Source Follower*
5. *Logic gates*

Small-Signal Equivalent Circuit for FETs

Output signal from an amplifier using FET can be effectively modulated by small changes of input signal current. In this way it is possible to make small changes from the Q point.

Symbols:
The total quantities: $i_D(t)$, $v_{GS}(t)$
The dc point values: I_{DQ}, V_{GSQ}
The signal $i_d(t)$, $v_{gs}(t)$

$$v_{GS}(t) = V_{GSQ} + v_{gs}(t)$$

$$i_D(t) = I_{DQ} + i_d(t)$$

Characteristic

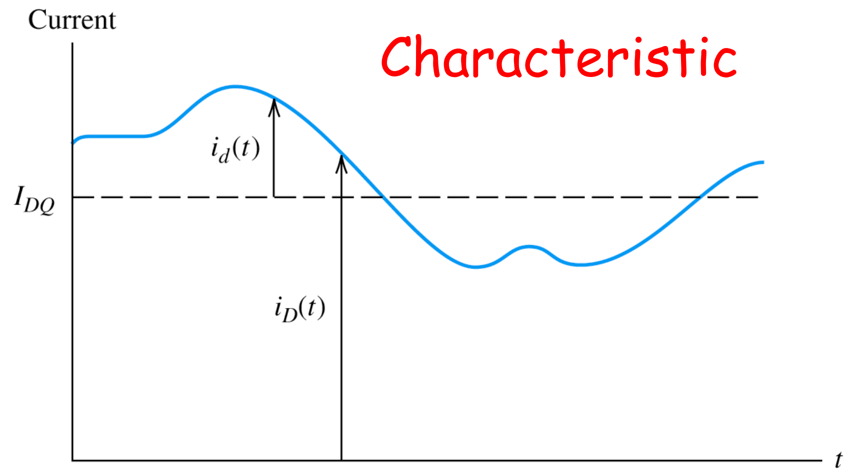


Figure 12.18 Illustration of the terms in Equation 12.15.

Small-Signal Equivalent Circuit -Transconductance

Schematic

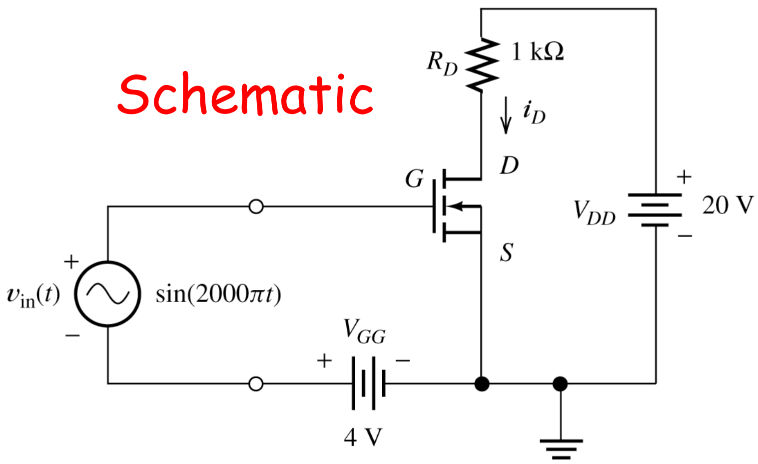


Figure 12.10 Simple NMOS amplifier circuit.

Analysis… (a little bit of math)

$$i_D = K\left(v_{GS} - V_{t0}\right)^2$$

$$I_{DQ} + i_d(t) = K\left[V_{GSQ} + v_{gs}(t) - V_{t0}\right]^2$$

$$I_{DQ} + i_d(t) = K\left(V_{GSQ} - V_{t0}\right)^2 + 2K\left(V_{GSQ} - V_{t0}\right)v_{gs}(t) + Kv_{gs}^2(t)$$

We know that $I_{DQ} = K\left(V_{GSQ} - V_{t0}\right)^2$ *

Also we assume that $\left|v_{gs}(t)\right| << \left|\left(V_{GSQ} - V_{t0}\right)\right|$

Small-Signal Equivalent Circuit -Transconductance

Schematic

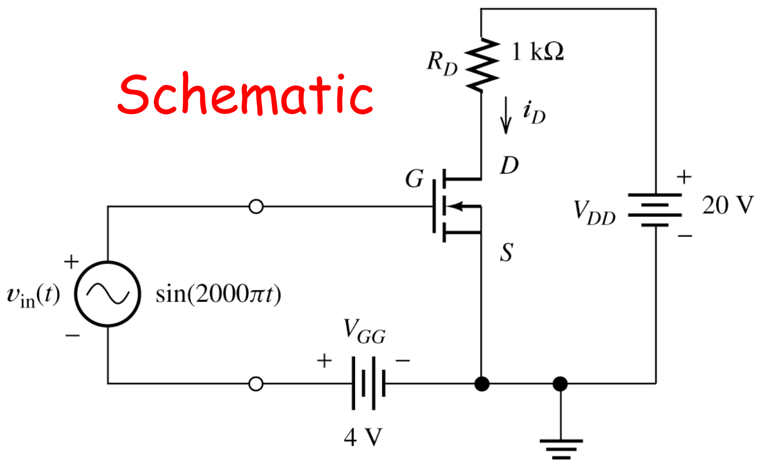


Figure 12.10 Simple NMOS amplifier circuit.

$$I_{DQ} + i_d(t) = K\left(V_{GSQ} - V_{t0}\right)^2 + 2K\left(V_{GSQ} - V_{t0}\right)v_{gs}(t) + Kv_{gs}^2(t)$$

We know that $I_{DQ} = K\left(V_{GSQ} - V_{t0}\right)^2$ *

Also we assume that $\left|v_{gs}(t)\right| << \left|\left(V_{GSQ} - V_{t0}\right)\right|$

Drain current generated by signal

$$i_d(t) = 2K\left(V_{GSQ} - V_{t0}\right)v_{gs}(t)$$

Small-Signal Equivalent Circuit -Transconductance

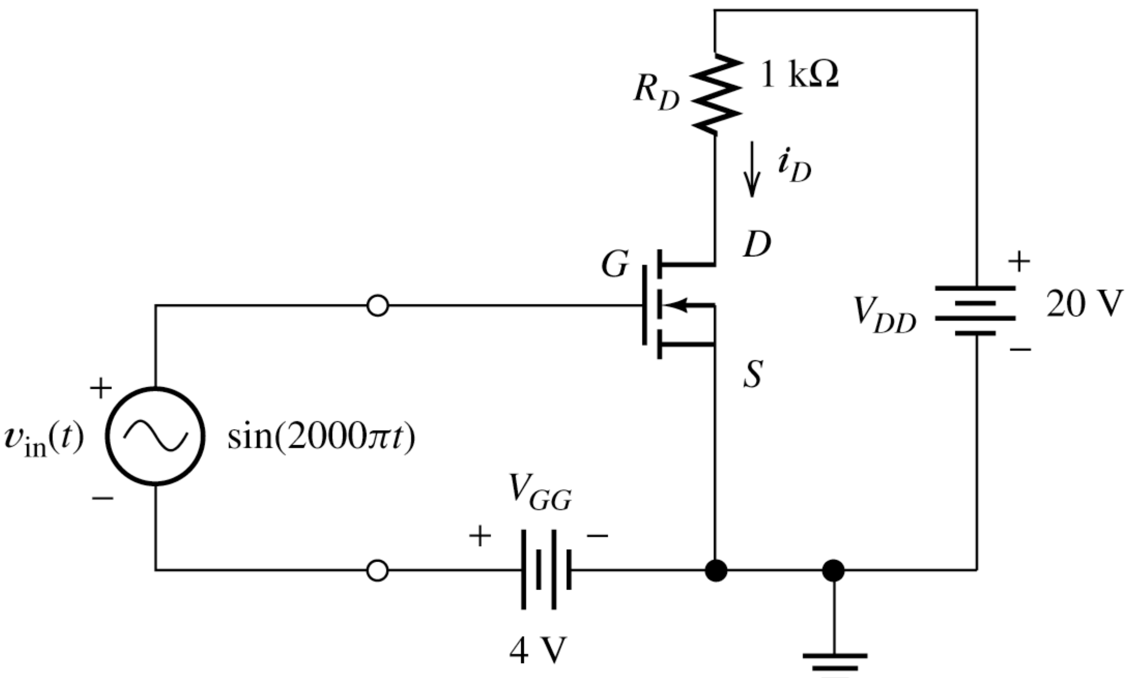


Figure 12.10 Simple NMOS amplifier circuit.

We define the transconductance as

$$g_m = \frac{i_d(t)}{v_{gs}(t)}$$

or

$$i_d(t) = g_m v_{gs}(t)$$

so

$$g_m = 2K\left(V_{GSQ} - V_{t0}\right)$$

Small-Signal Equivalent Circuit -Transconductance

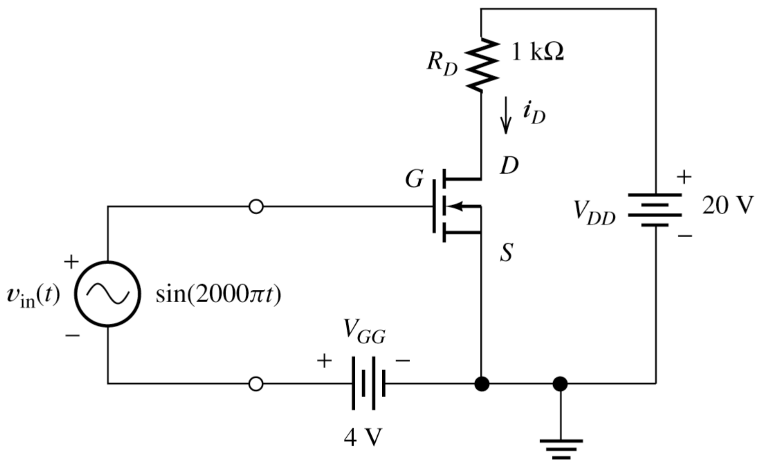


Figure 12.10 Simple NMOS amplifier circuit.

$$i_D = K\left(v_{GS} - V_{t0}\right)^2$$

so

$$\left(v_{GS} - V_{t0}\right) = \sqrt{\frac{I_{DQ}}{K}}$$

Thus the transconductance

$$g_m = 2K\left(V_{GSQ} - V_{t0}\right) = 2\sqrt{KI_{DQ}}$$

Small-Signal Equivalent Circuit -Transconductance

Exercise

The transistor has $KP=50\mu A/V^2$, $V_{to}=2V$, $L=10\mu m$, and $W=400\mu m$

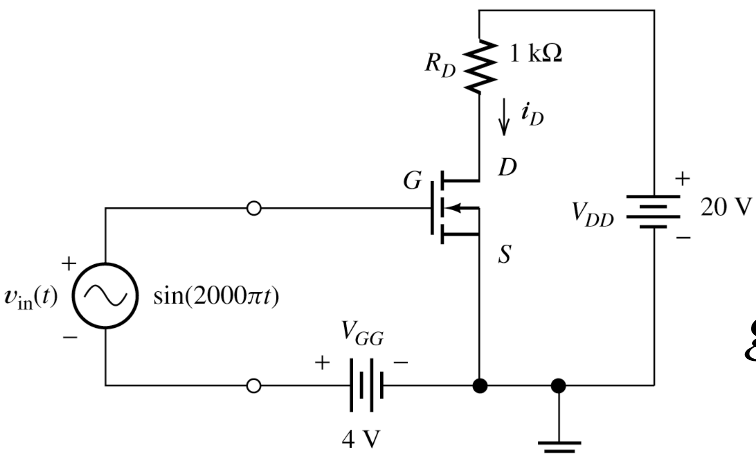


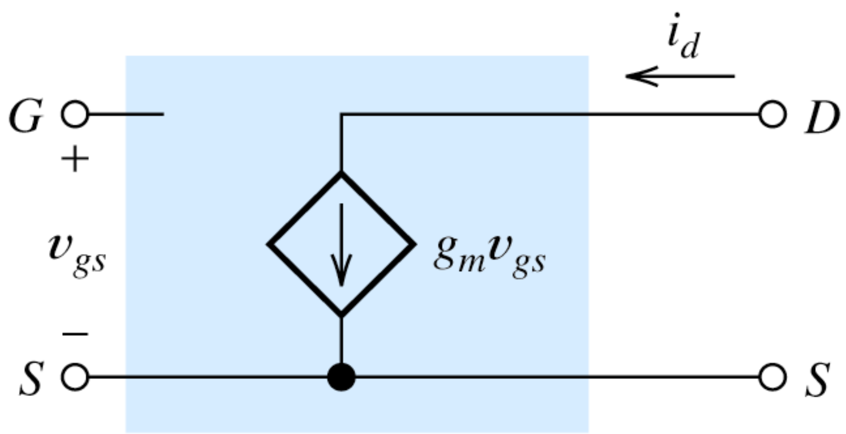
Figure 12.10 Simple NMOS amplifier circuit.

$$K=\left(\frac{W}{L}\right)\frac{KP}{2}=1mA/V2$$

$$g_m=2K\left(V_{GSQ}-V_{t0}\right)=2(4-2)=4mS$$

Small-Signal Equivalent Circuit

Also we assume that $i_g(t) = 0$



$$g_m = 2\sqrt{KI_{DQ}}$$

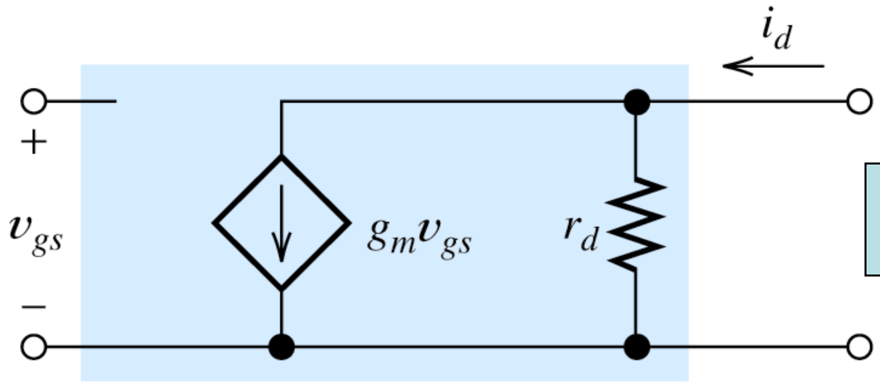
$$K = \left(\frac{W}{L}\right)\frac{KP}{2}$$

Figure 12.19 Small-signal equivalent circuit for FETs.

Better performance is obtained with higher values of g_m. Please notice that g_m is proportional to the square root of the Q point drain current. Simply, we can increase g_m by choosing a higher value of I_{DQ}.

More Complex Equivalent Circuits

For more accurate analyses of FET transistor we have to add more components to an equivalent circuit.
Small capacitance: for high response FET amplifiers
Drain resistor: account for the effect of v_{DS} on the drain current



Correction for i_d

$$i_d(t) = g_m v_{gs}(t) + v_{ds} / r_d$$

Figure 12.20 FET small-signal equivalent circuit that accounts for the dependence of i_D on v_{DS}.

Please read section: Transconductance and … pp.591
Example 12.3

Drain Resistance Calculation

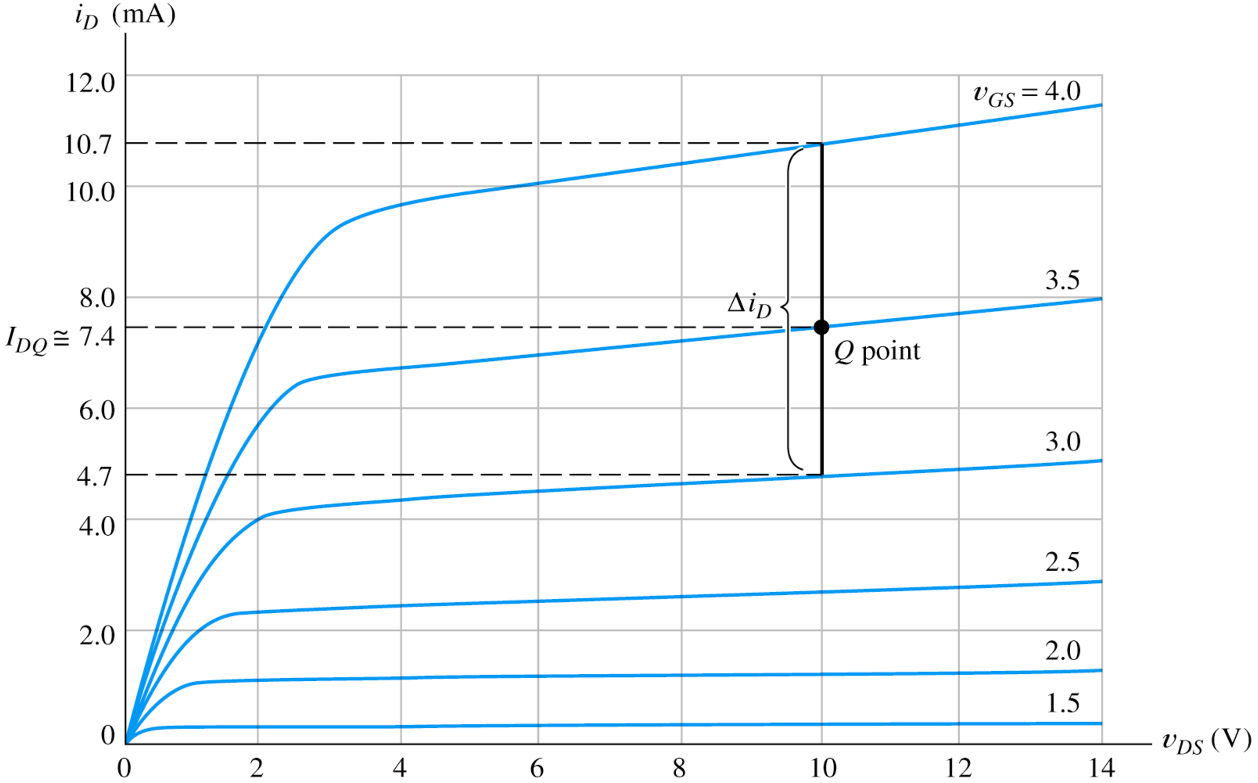


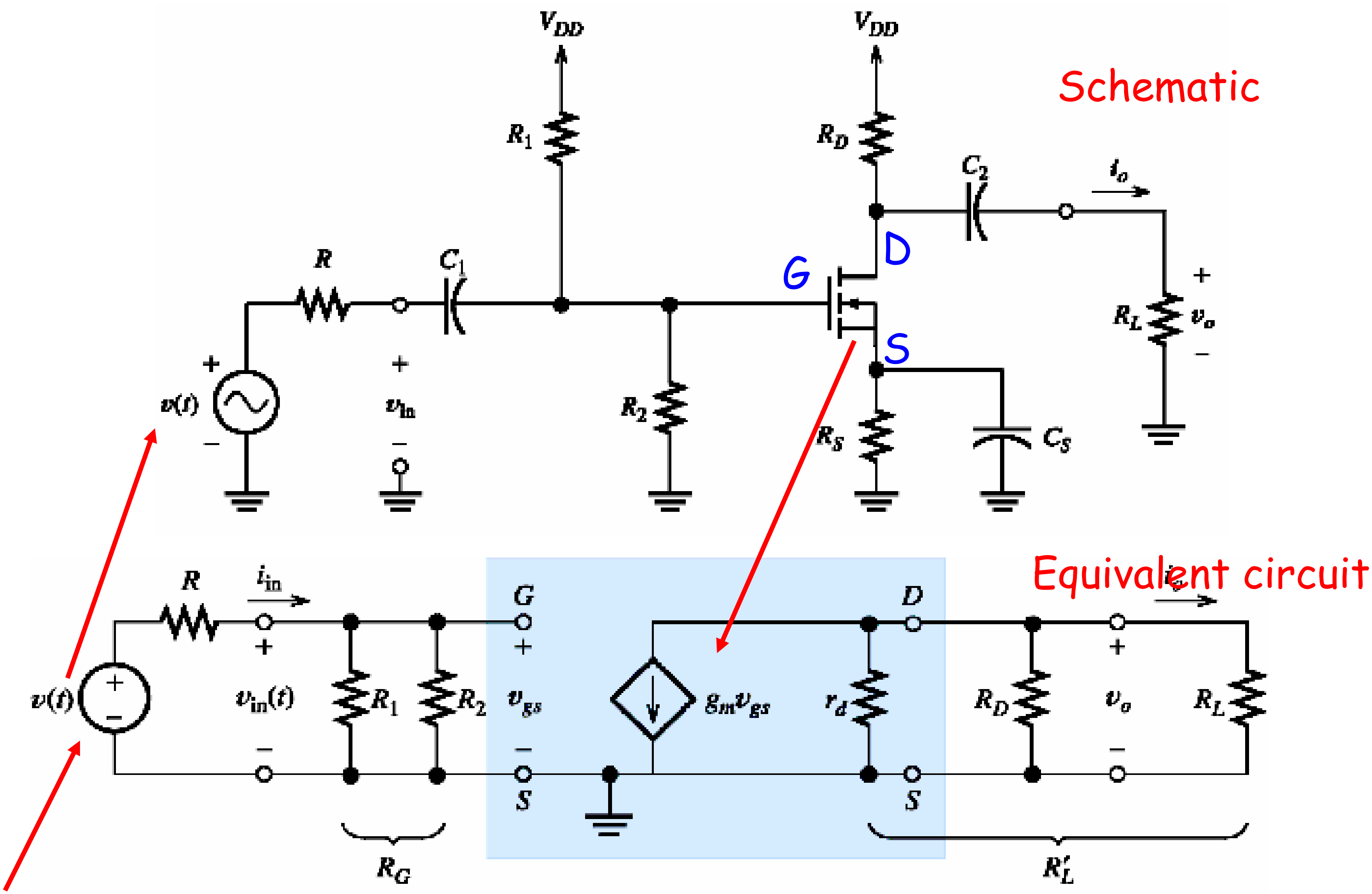
Figure 12.21 Determination of g_m and r_d. See Example 12.3.

$$\frac{1}{r_d} = \frac{\Delta i_D}{\Delta v_{DS}}$$

so at v_{GS}=4V

$$\frac{1}{r_d} = \frac{\Delta i_D}{\Delta v_{DS}} = \frac{(10.7 - 10)mA}{(10 - 6)V} = \frac{0.7}{4} mS = 0.175mS \qquad r_d = 5.7k\Omega$$

Common-Source Amplifier



The dc supply voltage acts as a short circuit for the ac current.

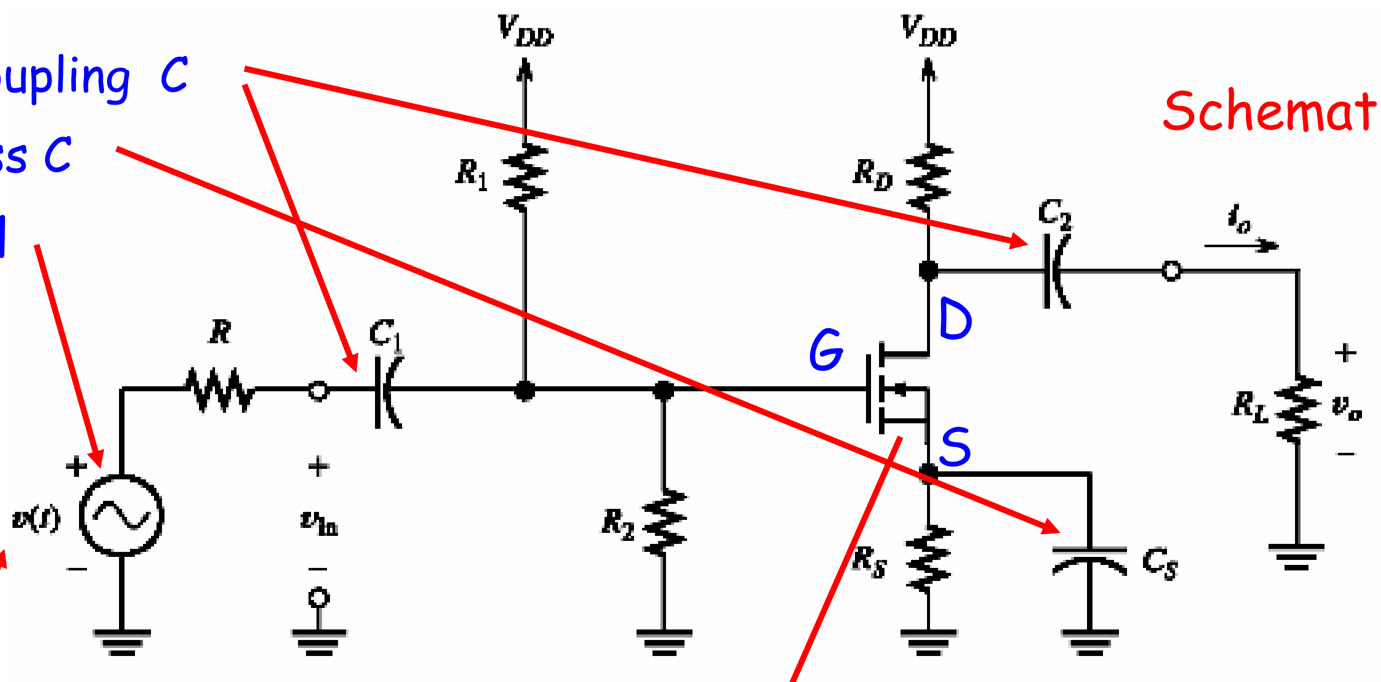
Common-Source Amplifier

C_1, C_2 -coupling C

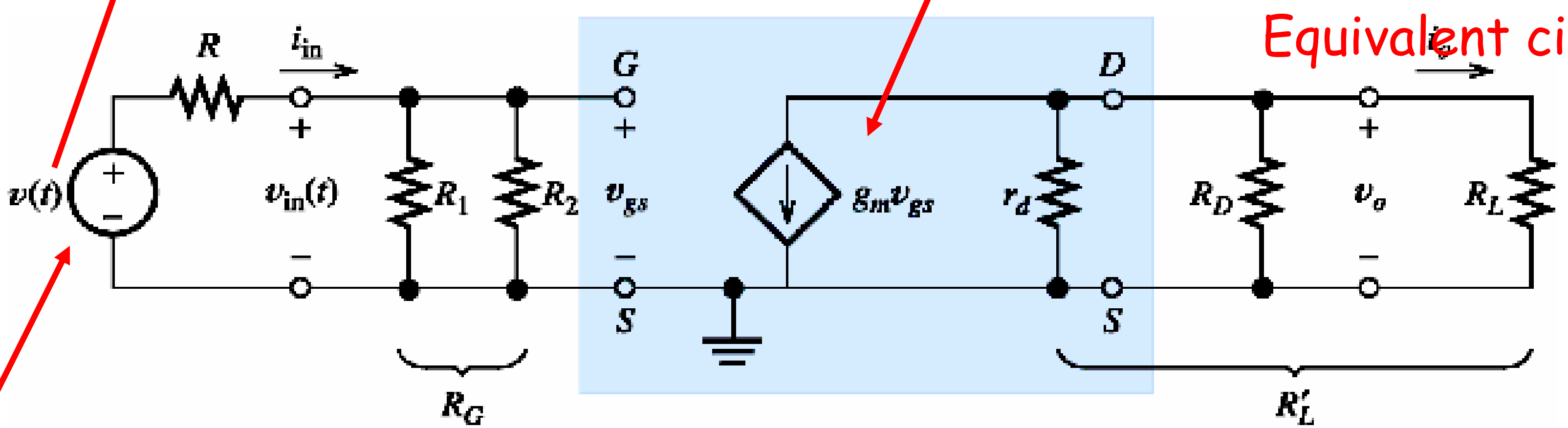
C_s -bypass C

ac signal

Schematic



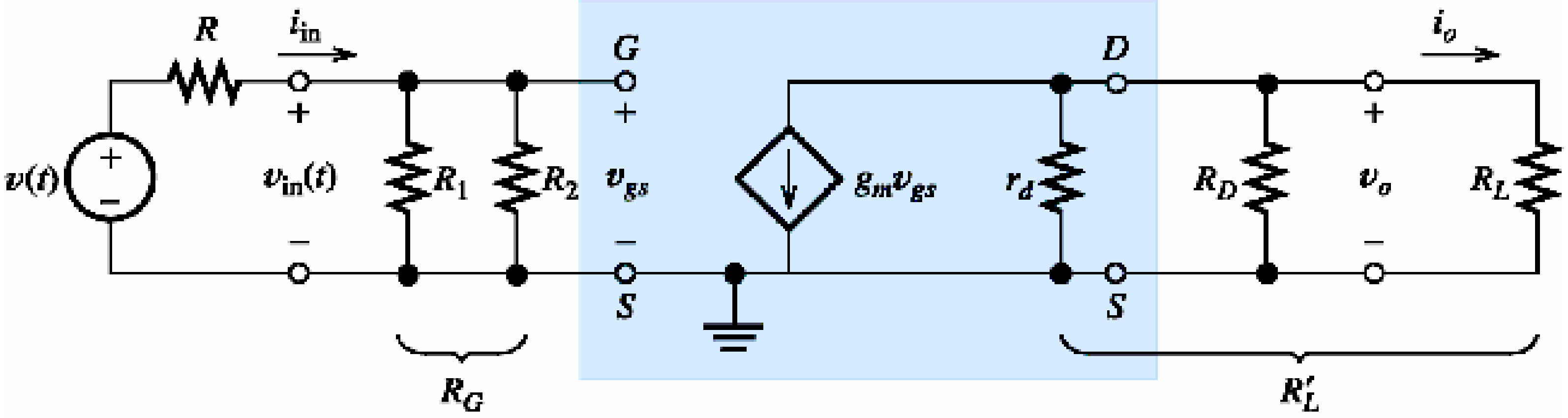
Equivalent circuit



The dc supply voltage acts as a short circuit for the ac current.

Common-Source Amplifier: Gain, R_{in} and R_{out}

Equivalent circuit (once more)



$$R'_L = \frac{1}{1/r_d + 1/R_D + 1/R_L}$$

Voltage gain

$$v_0 = -\left(g_m v_{gs}\right) R'_L \qquad v_{in} = v_{gs}$$

$$A_v = \frac{v_0}{v_{in}} = -g_m R'_L$$

Input resistance

$$R_{in} = \frac{v_{in}}{i_{in}} = R_G = R_1 \| R_2$$

From bias point analysis

Common-Source Amplifier: Gain, R_{in} and R_{out}

To find out the R_{out} we have to: disconnect the load, replace the signal source by short circuit – Thevenin equivalent resistance

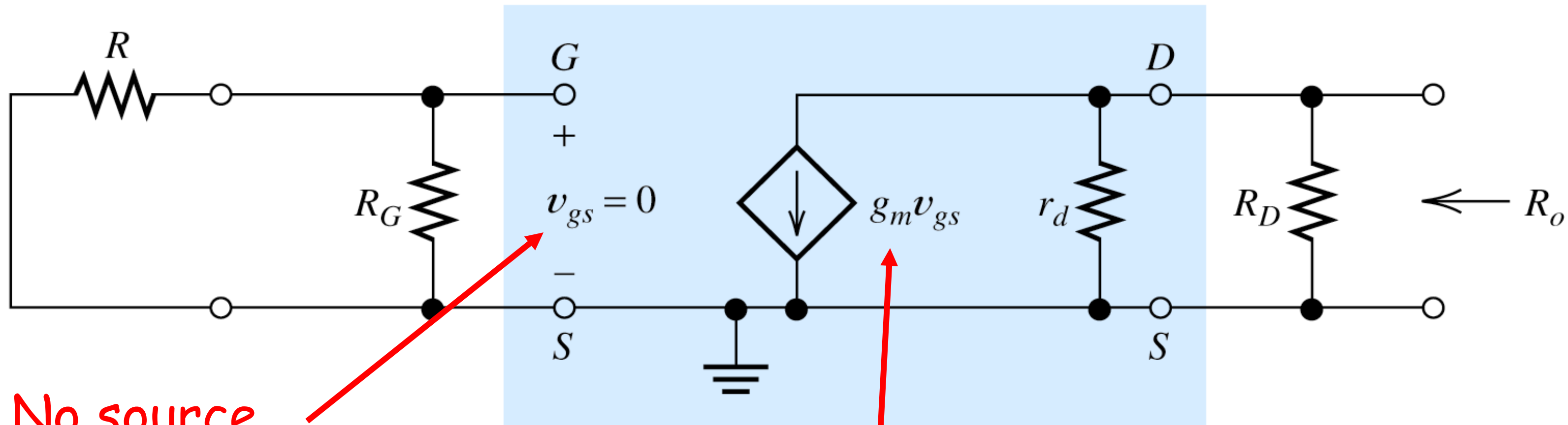


Figure 12.24 Circuit used to find R_o.

No source connected to the input

if $v_{gs}=0$ then $g_m v_{gs}=0$

Output resistance

$$R_{out} = \frac{1}{1/R_D + 1/r_d}$$

Example 12.4

Source Follower

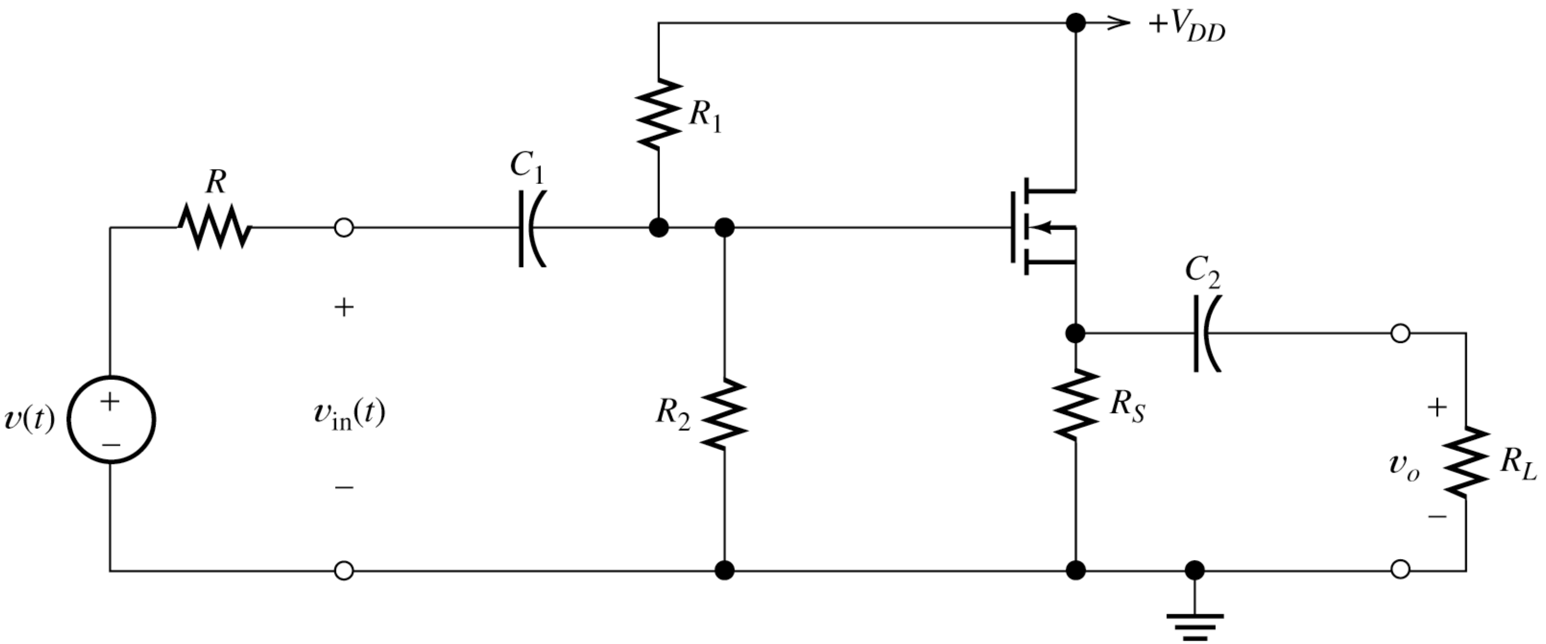


Figure 12.26 Source follower.

Small-Signal Equivalent Circuit –Source Follower

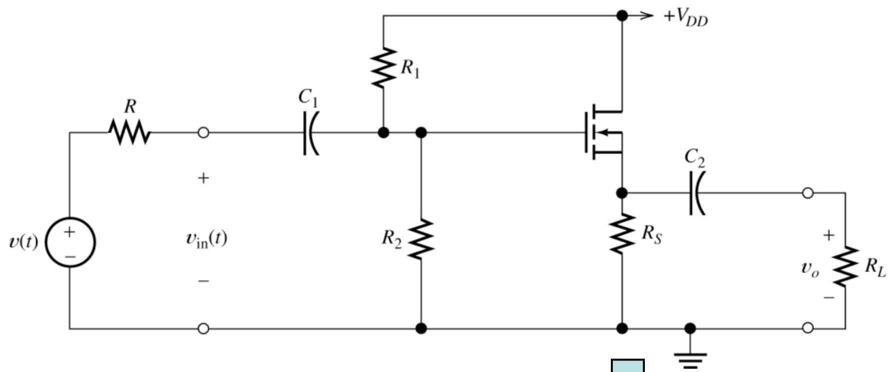


Figure 12.26 Source follower.

Notice that small signal I_{DS} goes up. Why?

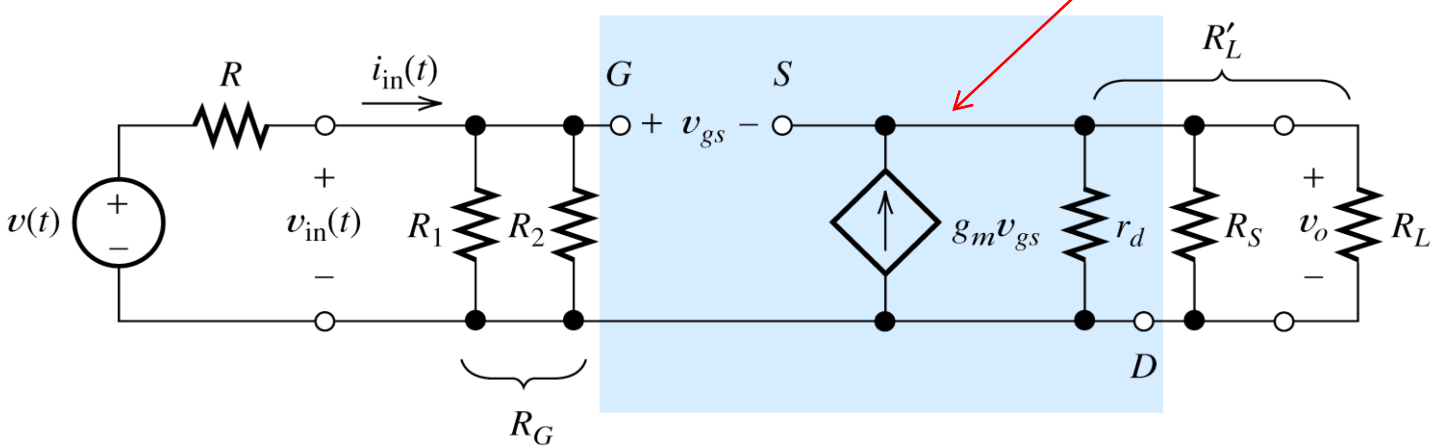


Figure 12.27 Small-signal ac equivalent circuit for the source follower.

Small-Signal Equivalent Circuit –Source Follower

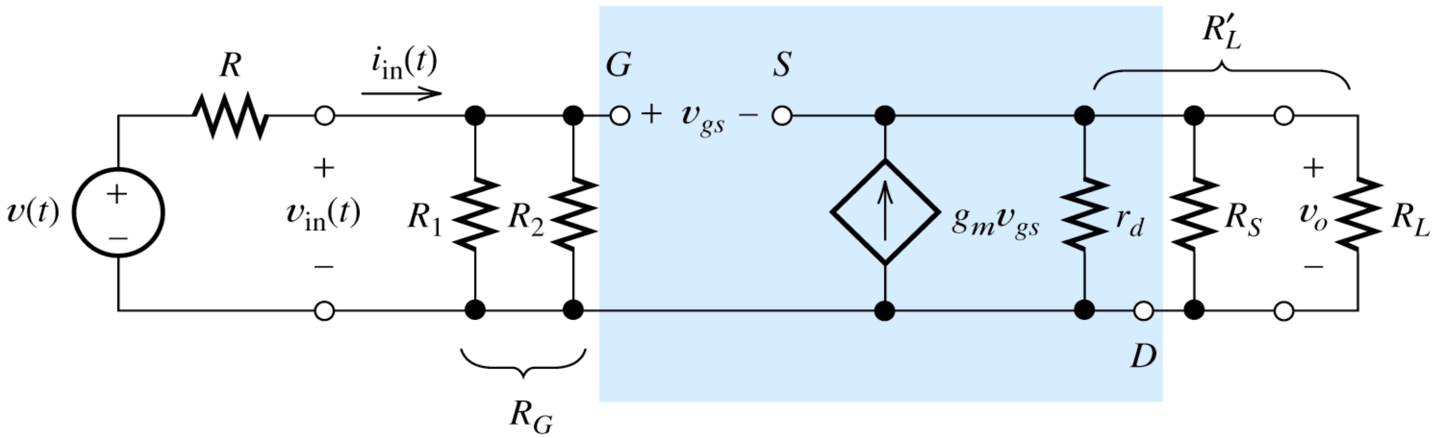


Figure 12.27 Small-signal ac equivalent circuit for the source follower.

$$R'_L = \frac{1}{1/r_d + 1/R_S + 1/R_L}$$

Input resistance

$$R_{in} = \frac{v_{in}}{i_{in}} = R_G = R_1 || R_2$$

Voltage gain

$$v_0 = g_m v_{gs} R'_L \qquad v_{in} = v_{gs} + v_o = v_{gs}\left(1 + g_m R'_L\right)$$

$$A_v = \frac{v_0}{v_{in}} = \frac{g_m R'_L}{1 + g_m R'_L} \leq 1$$

Since the output voltage is almost equal to the input – hence the name source follower

Logic gates - COMS Inverter

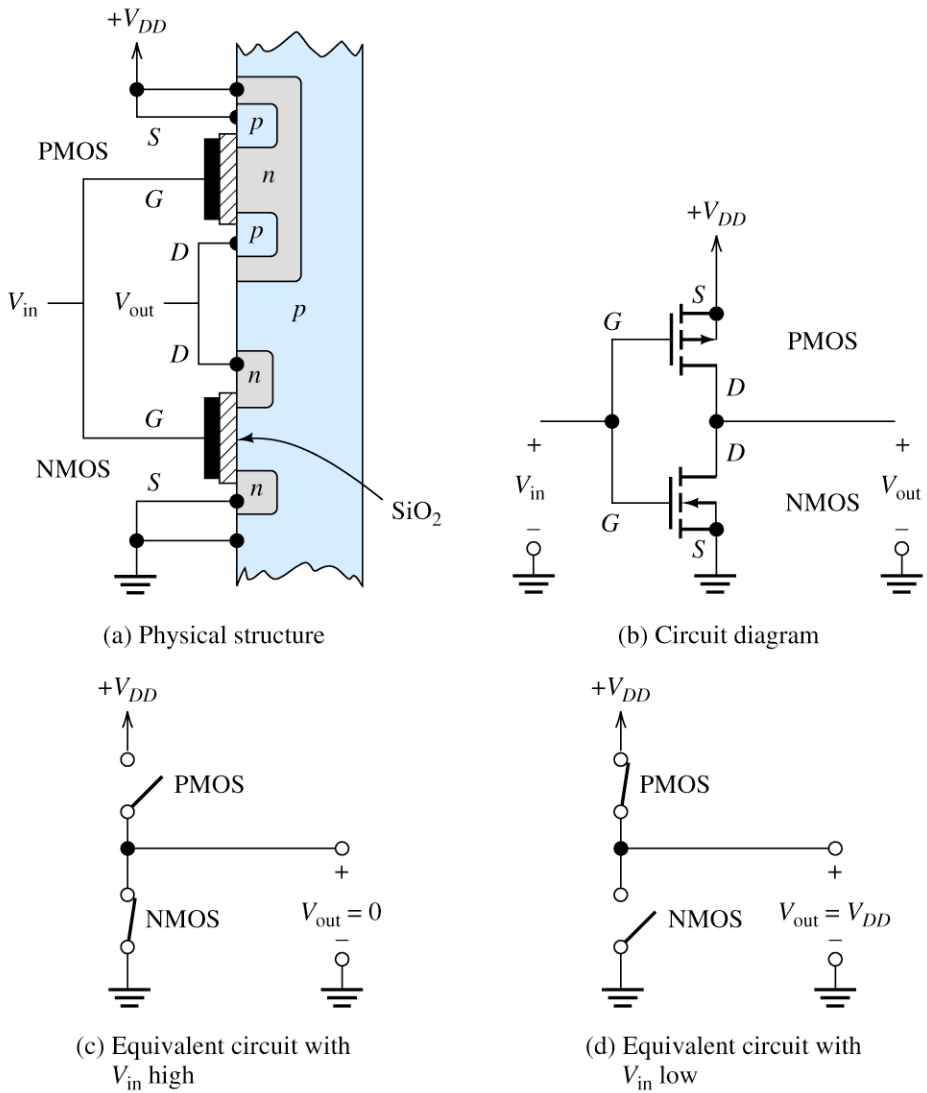


Figure 12.31 CMOS inverter.

Logic truth table

V_{in}	V_{out}
0	1
1	0

Switch level equivalent circuits

Logic gates - COMS NAND gate

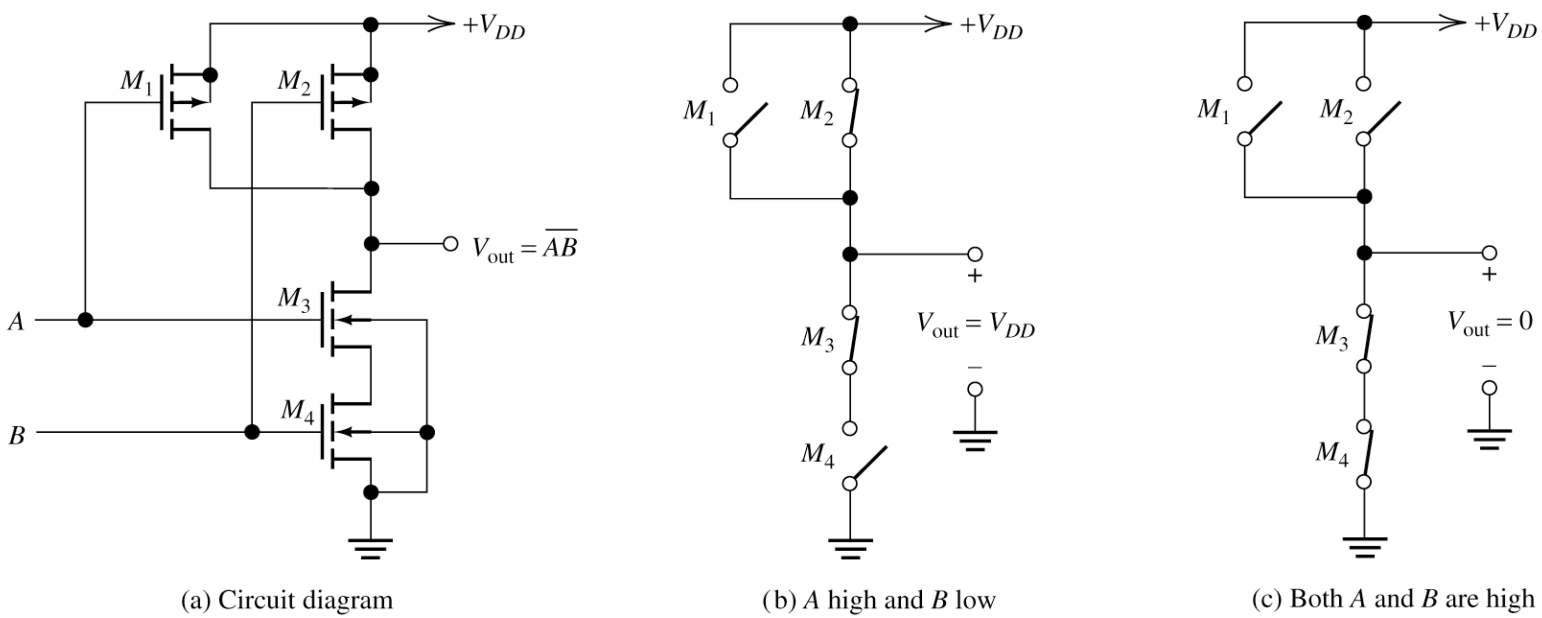


Figure 12.32 Two-input CMOS NAND gate.

Logic truth table

A	B	V out
0	0	1
0	1	1
1	0	1
1	1	0

Logic gates – COMS NOR gate

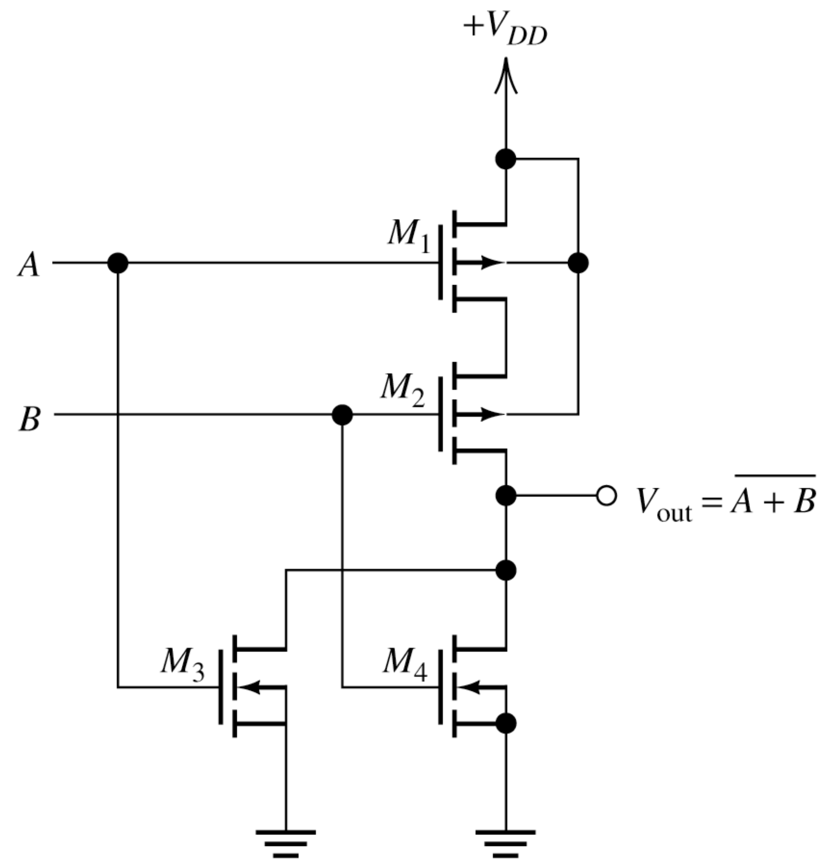
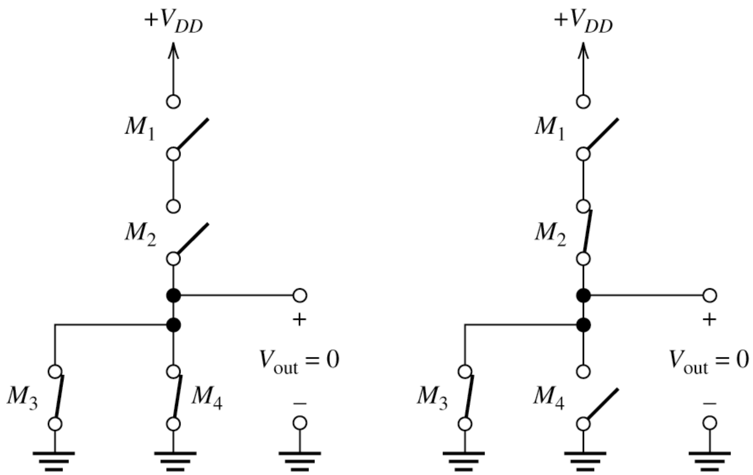


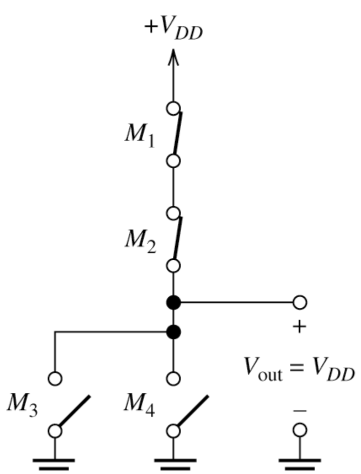
Figure 12.33 Two-input CMOS NOR gate.

Draw switch level circuits for different inputs and derive the truth table for this gate

Logic gates – COMS NOR gate



(a) A and B both high (b) A high and B low



(c) A and B both low

A	B	V_{out}
Low	Low	High
Low	High	Low
High	Low	Low
High	High	Low

(d) Truth table

Figure 12.34 Answers for Exercise 12.14.

Logic truth table

A	B	V out
0	0	1
0	1	0
1	0	0
1	1	0