Doc. No.: DCE/0/15
Revision :00

Lecture Plan -1

Semester:-6th Course Code:-EE-306-F

Section: A

S. No.	Subject: - VLSI DESIGN **Topic :- INTRODUCTION TO MOSFETS & STRUCTURES OF n-Type & p-Type MOSFETS**	**Time Allotted:-**
1.	**Introduction** VLSI DESIGN deals with study, design and fabrication of high component density ICs. The main components of ICs are diodes, resistances, inductances, capacitances and transistors. The knowledge about structure of different types of MOSFETs, the type of conducting channels, substrates and gates used and their modes of operation is very essential.	5 min
2	**Division of the Topic** -Introduction to MOSFETs -Description of MOSFETs -Operation of Enhancement mode & Depletion mode MOSFET -Description & structure of n-MOS & p-MOS -Description & structure of CMOS	35 min
3.	**Conclusion** MOSFET is a voltage controlled current source in contrast to a JFET which is a current controlled device. The structure of a MOSFET consists of layers of semiconductor substrates, insulators oxide, polysilicon and metal with diffused junctions forming drain and source and insulated gates.	5 min
4	**Q1**. Why is Field Effect Transistor (FET) so called? **A1**. The FET is so called because the mechanism of current control is the effect of the "field" produced by the drain-source and gate-source voltages. **Q2**What is the difference between of E-MOSFET and D-MOSFET ? **A2**. In E-MOSFET, a conducting channel is Created and Enhanced between theSource and Drain by application of a gate voltage.On the other hand in Depletion mode MOSFET, a conducting channel already exists between the Drain and Source which can be depleted or enhanced.	5min

Assignment to be given:- NIL

Reference Readings:-

1. Digital Integrated Electronics – Taub & Schilling
2. Integrated Circuits – KR Botkar

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Lecture Plan -2

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: A

S. No.	Topic :- EQUIVLENT CIRCUITOF MOSFETS	Time Allotted:-
1.	**Introduction** For understanding the theory and designing and developing any circuit utilizing any electronic device and for establishing the relations between input voltage/currents and output voltage/currents, it is necessary to represent each type of the device by suitable symbols and equivalent circuits. This topic deals with the symbols and equivalent circuits of MOSFETs.	5 min
2	**Division of the Topic** -Symbols and equivalent circuit of n-MOS & p-MOS. -Threshold voltages for n-MOS and p-MOS -Drain current characteristics of E-type & D-type n-MOSFET -Identification of regions of operation of the MOSFETs -Conductance characteristics of E-type & D-type n-MOSFET - Symbols and equivalent circuit of CMOS	35 min
3.	**Conclusion** The symbols and equivalent circuits of different MOSFETs are specific to each type and can be easily distinguished and are different from those of bipolar transistors. The voltage current characteristics define the ranges and various regions of operation of the MOSFETs.	5 min
4	**Questions / Answers** **Q1**..What are the changes in circuitary between n-MOS and p-MOS ? **A1**. While in n-MOS, the drain and gate are positive with respect to source normally connected to substrate; their polarities are reversed in p-MOS. **Q2**.What are the various regions of operation in an n-MOS? **A2.** There are three regions of operation.(1) Cut off region (2) Ohmic or linear resistive or Triode region (3) Saturated region	5min

Assignment to be given:- Various methods involved in fabrication of VLSI as per Assignment-I enclosed

Reference Readings:-

1.Digital Integrated Electronics – Taub & Schilling
2.Integrated Circuits – KR Botkar

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Lecture Plan -3

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: A

S. No.	TOPIC: MOS DEVICE DESIGN EQATIONS	Time Allotted:-
1.	**Introduction** For utilization of any electronic device in any electronic circuit it is very essential to understand the theory of the device. As MOS transistors are the main components of any IC, knowledge of the theory of MOS transistor is very important. This helps us derive the MOS device design equations and define various parameters of MOS transistors. These equations establish the relation between input currents/ voltages and output currents/ voltages.	5 min
2	**Division of the Topic** -Revision of structure of Enhancement mode n-MOSFET -Polarities of voltages applied to Gate, Drain, Source & Substrate. -Formation of channel in enhancement mode MOSFET -Derivation of mathematical expression for Drain current I_{DS} for n-MOS and p-MOS	35 min
3.	**Conclusion** The current characteristics define the ranges and various regions of operation of the MOSFETs and equations of IDS define the I_{DS} Vs V_{DS} & I_{DS} Vs V_{GS} characteristics.	5 min
4	**Questions / Answers** **Q1.** What do you mean by Threshold voltage for E-type n-MOS? **A1**. It is the minimum positive gate-source voltage required to be applied for establishing current (formation of conducting channel) between drain and source in case of E-type n-MOS. **Q2**.What do you mean by Threshold voltage for D-type n-MOS? For D-type n-MOS it is the minimum negative gate-source voltage required to be applied to completely deplete the cannel or make the channel current zero	5min

Assignment to be given:- NIL

Reference Readings:-

1.Digital Integrated Electronics – Taub & Schilling
2.Integrated Circuits – KR Botkar

Doc. No.: DCE/0/15
Revision :00

Lecture Plan -4

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: A

S. No.	TOPIC: VARIOUS ASPECTS OF MOS DEVICE THRESHOLD VOLTAGE	Time Allotted:-
1.	**Introduction** The gate structure of a MOS transistor consists electrically of charges stored in the dielectric layers and in the surface to surface interfaces as well as in the substrate itself. Threshold voltage is the gate voltage required to neutralize these charges and enabling the underlying silicon to undergo an inversion due to the electric field from the gate so that the MOS transistor is switched from the OFF to ON for E-type and ON to OFF for D-TYPE MOSFET.	5 min
2	**Division of the Topic** -Revision of Diagram of structure of n-MOS & p-MOS & voltage polarities. -Definition of Threshold voltage & substrate bias. -Work function difference between gate and Si -Fermi level potential between inverted surface and bulk Si -Expression for Threshold voltage -Meaning & Expression of Body effect -Effect of temperature change on threshold voltage	35 min
3.	**Conclusion** The threshold voltage decides the switching on/off of MOS transistor. The mathematical expressions helps us in calculation of the threshold voltage fro a MOS device for design and operation in an electronic circuit.	5 min
4	**Questions / Answers** **Q1.** What do you mean by Body effect of Threshold voltage for E-type n-MOS? **A1**. It is the change in the threshold voltage due to variation in source-substrate voltage. Increasing the reverse bias increases the threshold voltage. **Q2**. What is the effect of temperature on Threshold voltage? **A2.** The change in temperature has a negative effect on threshold voltage. The rate of change of threshold voltage with temperature is approximately equal to −2.5 mV/ °C.	5min

Assignment to be given:- NIL

Reference Readings:-

1. Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian
2. Basic VLSI design- D.A. Pucknell & K. Eshraghian

Doc. No.: DCE/0/15
Revision :00

Lecture Plan -5

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: A

S. No.	TOPIC: MOS DEVICE SUB THRESHOLD REGION, CHANNEL LENGTH MODULATION & MOBILITY VARIATION	Time Allotted:-
1.	**Introduction** The cutoff region of the IDS Vs VDS is called as the subthreshold region. The MOS device equations assumed that the carrier mobility is constant and do not take into account the variation in channel length due to changes in drain to source voltage VDS. Hence the necessity to understand the channel length modulation.	5 min
2	**Division of the Topic** -Subthrehold region -Channel length Modulation -Mobility variation -Fowler-Nordheim Tunnelling -Drain Punchthrough -Impact ionization-Hot electrons	35 min
3.	**Conclusion** Knowledge of value of current, although low can be utilized to construct very low power circuits. Channel length modulation is conspicuous for short channel lengths. This increases W/L ratio & increases β with drain voltage. Thus in stead of appearing as a constant current source with infinite impedance in the saturated region, the MOS device has a finite output impedance.. FN tunneling is prominent when gate oxide is very thin. Drain punch through can occur if the drain voltage is very high with respect to the source.	5 min
4	**Questions / Answers** **Q1.** What do you mean by mobility μ of charge carriers? **A1**. It is the ease with which the carriers drift in the substrate and is equal to the ratio of average carrier drift velocity to the applied electric field. **Q2**. How does the mobility μ of charge carriers vary? **A2.** The mobility μ of electrons (negative charge carriers) is approximately 2.5 to 3 times of mobility μ of positive charge carriers. Further the Mobility decreases with increasing doping concentration and increasing temperature	5min

Assignment to be given:- NIL

Reference Readings:-

1.Digital Integrated Electronics – Taub & Schilling

2.Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian

3 Basic VLSI design- D.A. Pucknell & K. Eshraghian

Doc. No.: DCE/0/15
Revision :00

Lecture Plan -6

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: A

S. No.	TOPIC: MOS DEVICE TRANSCONDUCTANCE, OUTPUT CONDUCTANCE AND FIGURE OF MERIT	Time Allotted:-
1.	**Introduction** Knowledge of the basic parameters like trans conductance, output conductance, figure of merit are essential if the MOS device is to be used for ascertaining small signal AC characteristics, Voltage amplification factors(gain) , bandwidth & frequency response characteristics or switching speeds in different electronic switching circuits.	5 min
2	**Division of the Topic** - MOS device transconductance - figure of merit - Small signal equivalent model AC characteristics - Output conductance - Channel resistance	35 min
3.	**Conclusion** Transconductance gm is used to measure the gain of an MOS device. In the linear region gm (linear) is proportional to output drain to source voltage and in the saturation region gm (sat) is proportional to the difference between input gate-source voltage and respective threshold voltage. The output conductance gds (linear) is equal to gm (sat).	5 min
4	**Questions / Answers** Q1 .Differentiate between transconductance gm and output conductance gds? A1. The transconductance gm is the ratio of change in output drain source current for change in input gate-source voltage. The output conductance gds is the ratio of change in output drain source current for change in output drain source voltage. Q2. What is figure of merit?A2**.**It is the ratio of transconductance gm to gate capacitance Cg	5min

Assignment to be given:- Assignment II given as enclosed

Reference:-

1.Digital Integrated Electronics – Taub & Schilling

2.Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian

3 Basic VLSI design- D.A. Pucknell & K. Eshraghian

Doc. No.: DCE/0/15
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Lecture Plan -7

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: A

S. No.	TOPIC: MOS SWITCHING DEVICE	Time Allotted:-
1.	**Introduction** Like transistors and MOSFETS are used as switching device in ICs and these switches can be externally controlled by application of gate voltages above or below threshold voltages. In an IC, if a resistor is to be fabricated, a lot of space is consumed to accommodate high value of load. In the same space a very high value of resistance can be realized using a MOS device instead of a conventional resistor.	5 min
2	**Division of the Topic** -Basic switching device using a mechanical switch and resistor as load -Switching device using a transistor as a switch & resistor as load -Switching device using a MOS transistor as a switch & MOS device as load -Different configurations of MOS switches and MOS loads -Output characteristics for different ratios of (W/L)driver/ (W/L)load	35 min
3.	**Conclusion** The requirement of load value for MOS switching device is very large compared to normal switching device. A miniaturized switch is realized using MOS switch and MOS load. A variety of combinations can be configured by varying the types of MOSFETs and their modes of operation as well as their bias voltages	5 min
4	**Questions / Answers** **Q1** What is typical value of mobility **μ** of charge carriers at room temperature? **A1**. μn = 650 cm2/V μp = 240 cm2/V **Q2**. What are typical value of threshold voltages VTE & VTD for VSB = 0V & 5V? **A2.** For enhancement **n**-MOS with VDD =+ 5V, for VSB = 0V, VTE = +1V & for VSB = **5**V, VTE = +1.5V. The values are similar but negative for pMOS transistors. For depletion nMOS with VDD = +5V, for VSB = 0V, VTD= 3.5V & for VSB = **5**V, VTD= 3.0V	5min

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Assignment to be given:- NIL

Reference Readings:-

1.Digital Integrated Electronics – Taub & Schilling

2.Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian

3 Basic VLSI design- D.A. Pucknell & K. Eshraghian

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Lecture Plan -8

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: A

S. No.	Topic:-LATCH UP IN CMOS CIRCUITS & BICMOS CIRCUIT SUSCEPTIBILITY	Time Allotted:-
1.	**Introduction** Latch –up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between V_{DD} and V_{SS} with disastrous results. The major problem with MOS technology lies in the limited load driving capabilities of MOS transistors. This is due to the limited current sourcing and current sinking abilities associated with both p and n transistors.	5 min
2	**Division of the Topic** 1. Basic Principle 2. Working of Latch –up circuit 3. Latch-up circuit Model 4. V-I characteristics of TTL 5. BiCMOS inverter Circuit 6. An alternative BiCMOS inverter with no static current flow. 7. An improved BiCMOS inverter with better output logic levels. 8. An improved BiCMOS inverter using MOS transistors for base current discharge.	35 min
3.	**Conclusion** Latch up is induced by glitches on the supply rails or by incident radiation. Once latched-up, this condition will be maintained until the latch-up current drops below I1.Bipolar transistors provide higher gain and have generally better noise and high frequency characteristics than MOS transistors. Using BiCMOS gates is an effective way of speeding up VLSI circuits.	5 min
4	**Questions / Answers** **Q1 What is the remedy to latch-up problem?** **Ans** An increase in substrate doping levels with a consequent drop in the value of Rs and reducing Rp by controlling the fabrication parameters and by ensuring a low contact resistance to Vss. **Q2 How BiCMOS suffers less latch-up problems?** **Ans** A reduction of substrate resistance Rs, and a reduction of n-well resistance Rw.	5min

Assignment to be given:- Assignment –IVgiven as enclosed

Reference Readings:-

Principles of CMOS VLSI: Design:……By Neil H. E. Weste.

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Lecture Plan -9

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: B

S. No.	TOPIC: MOS INVRTERS	Time Allotted:-
1.	**Introduction** The basic requirement for producing a complete range of logic circuits is the inverter. This is needed for restoring logic levels, for NAND and NOR gates and for sequential and memory circuits of various forms	5 min
2	**Division of the Topic** -Basic n-MOS inverter with depletion mode pull up transistor as load -Drain current characteristic of driver (Pull down) and load (Pull up) -Derivation of n-MOS inverter transfer characteristic & threshold voltage of inverter. -Effect of variation of (Z pu / Zpd) on the transfer characteristic nition of gain of inverter	35 min
3.	**Conclusion** Various types of inverters can be made with different configurations of MOS devices. The output of the MOS switches (Pull up/ Driver) connected with a load (Pull down) is an invariably an inverted version of input	5 min
4	**Questions / Answers** **Q1** What is the order of load resistors for bipolar transistor switching device and for MOSFET switching device? **A1**..For bipolar transistor switches the load resistor is of order of thousand ohms. For MOSFET switches the load resistor is of order of many thousand ohms, even up to well over 100 kΩ. **Q2**. What is the advantage of MOSFET load over conventional load resistor? **A2.**. A 20 kΩ resistor may occupy an area of 20 square mils while a complete MOSFET switch with load of 100 kΩ may occupy an area of only 2 square mils. The MOSFET load can be fabricated over a small area compared to a diffused resistor	5min

Assignment to be given:- NIL

Reference Readings:-

1.Digital Integrated Electronics – Taub & Schilling
2.Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian
3 Basic VLSI design- D.A. Pucknell & K. Eshraghian

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Lecture Plan -10

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: B

S. No.	TOPIC: CMOS SWITCH &INVERTER	Time Allotted:-
1.	**Introduction** The input output characteristics for a MOSFET switch do not have sharp response as compared to a bipolar transistor switch. Higher is (W/L) DRIVER / (W/L)LOAD, sharper is the response. To achieve a reasonably sharper response the load MOSFET channel should be narrower and longer compared to that of driver MOSFET. This drawback has been reasonably overcome in a CMOS switching device.	5 min
2	**Division of the Topic** -Drawbacks in the input output characteristics of MOS switch -Revision of Basic CMOS structure -Circuit diagram of basic CMOS switch - Description of Input-output characteristic plots for CMOS switch - Effect of variation of (Z pu / Zpd) on the transfer characteristic - Effect of variation of temperature on the transfer characteristic -Variation of drain current during switching along with relevant plots - Power dissipation in CMOS switch.	35 min
3.	**Conclusion** The transition of output voltage between logic level 1 and logic level 0 in a CMOS switch is rather much sharper compared to MOS switch. The input output characteristic is also not sensitive to changes in temperature. The common drain-source current & power consumption is nominally zero when the CMOS switch output is at one or the other limit of its range.	5 min
4	**Questions / Answers** **Q1** What are the changes in Input-output characteristic plots for CMOS switch compared to a MOS switch? **A1**..In CMOS switch we have very sharp transition from level 1 to level 0 compared to slant features in MOS switch.. **Q2**. What are the changes in Input-output characteristic plots for CMOS switch due to change in temperature? **A2.** The input output characteristics are insensitive to changes in temperature.	5min

Assignment to be given:-Nil

Reference Readings:-

1. Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian
2. Basic VLSI design- D.A. Pucknell & K. Eshraghian

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Lecture Plan -11

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: B

S. No.	TOPIC: CMOS INVERTER (CONTINUED)	Time Allotted:-
1.	**Introduction** In Complementary Metal Oxide Semiconductor, no current flows either for logic 0 or for logic 1 input. Full logic 1 and 0 levels are presented at the output. For devices of similar dimensions the p-channel is slower than the n-channel device.	5 min
2	**Division of the Topic** 1. Basic principle of CMOS 2. Working of CMOS 3. DC characteristics of CMOS 4. β_n / β_p ratio 5. Noise Margin 6. CMOS Inverter as an Amplifier	35 min
3.	**Conclusion** The gate – threshold voltage , Vinv , where Vin=Vout is dependent on βn / βp ratio. In order to change this, the channel dimensions i.e., channel-length L and channel-width W need to be changed. Noise Margin is a parameter closely related to the input-output voltage characteristics. It determines the allowable noise voltage on the input of a stage so that the output will not be affected.	5 min
4	**Questions / Answers** **Q1 What is the condition for CMOS acting as a amplifier?** **Ans** Vout = -AVin. **Q2 What is the expression for Noise Margin?** **Ans** $NM_L = [V_{ILMAX} – V_{OLMAX}]$	5min

Assignment to be given:-Nil

Reference Readings:-

Principles of CMOS VLSI: Design:……By Neil H. E. Weste

Doc. No.: DCE/0/15
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Lecture Plan -12

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: B

S. No.	TOPIC: COMPARISONS OF ALTERNATIVE FORMS OF PULLUP	Time Allotted:-
1.	**Introduction** Till now we have assumed that inverter circuit has a depletion mode pull up transistor as its load. Various types of inverters can be made with different configurations of MOS devices.	5 min
2	**Division of the Topic** -Basic configuration of MOS switch with load resistance R_L -Configuration of MOS switch and n-MOS depletion mode transistor pull up -Configuration of MOS switch and n-MOS enhancement mode transistor pull up - Configuration of MOS switch and Complementary transistor (CMOS)pull up -Transfer characteristics different forms of pull up. parison of alternative forms of pull up.	35 min
3.	**Conclusion** Various types of inverters can be made with different configurations of MOS devices. Depending on our requirements and availability of components we have to select the required type of inverter. An inverted version of input.	5 min
4	**Questions / Answers** **Q1** What is a switching device? **A1**.A switching device either allows or does not allow an input to pass through it. **Q2**.Where and how do you use a switching device? **A2.** In digital circuits various logic gates are used. The basic logic gates are made up of series and parallel switches and their combinations. Thus the switches devices can be used to configure various gates in the digital circuitry.	5min

Assignment to be given:- NIL

Reference Readings:-

1.Digital Integrated Electronics – Taub & Schilling

2.Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian

3 Basic VLSI design- D.A. Pucknell & K. Eshraghian

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Lecture Plan -13

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: B

S. No.	MOS AS PASS TRANSISTOR & DETERMINATION OF PULL UP/PULL DOWN RATIO FOR n-MOS INVERTER DRIVEN BY ANIOTHER n-MOS INVERTER /PASS TRANSISTOR	Time Allotted:-
1.	**Introduction** Unlike bipolar transistor, the isolated nature of gate allows MOS transistors to be used as switches in series with lines carrying logic levels in a way similar to relay contacts. This application of MOS device is called the pass transistor. However logic 1 is slightly degraded by an amount equal to the threshold voltage.	5 min
2	**Division of the Topic** -MOS as pass transistor - Determination of pull up / pull down ratio for n-MOS inverter driven by another n-MOS inverter with block circuit diagrams and equivalent circuits -Determination of pull up/pull down ratio for n-MOS inverter driven through one or more pass transistors with block circuit diagrams and equivalent circuits.	35 min
3.	**Conclusion** Pull up/pull down ratio for n-MOS inverter driven by another n-MOS inverter is greater than or equal to 4/1.Pull up/pull down ratio for n-MOS inverter driven through one or more pass transistors greater than or equal to 8/1. It is the driven, not the driver whose ratio is affected	5 min
4	**Questions / Answers** **Q1** What is pass transistor? **A1**..It is an application of MOS device in which it is used as switch in series with lines carrying logic levels in a manner similar to the use of relay contacts. **Q2**.What is the change in Pull up/pull down ratio for n-MOS inverter driven through one or more pass transistors instead of being driven by another n-MOS inverter? **A2.** The Pull up/pull down ratio increases by double. A typical value increases from 4/1 to 8/1.	5min

Assignment to be given:- NIL

Reference Readings:-

1.Digital Integrated Electronics – Taub & Schilling

2.Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian

3 Basic VLSI design- D.A. Pucknell & K. Eshraghian

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Lecture Plan -14

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: B

S. No.	TOPIC: STATIC LOAD MOS INVERTER & DIFFRETIAL INVERTER	Time Allotted:-
1.	**Introduction** When transistors are used as load and driver, the inverter is called as a saturated load inverter, if the load transistor is operated in saturation as a constant current source. If the load transistor is biased for use as a resistor then it is called unsaturated load inverter. An inverter that uses two differential inputs and produces two differential outputs is known as a differential inverter.	5 min
2	**Division of the Topic** -A generic static load inverter -The Pseudo –n MOS inverters -Saturated load inverters using n MOS transistor load -The Cascode inverter -TTL interface inverter -Basic Differential Amplifier Equivalent circuit & I/O characteristic -Differential gain & Common Mode Rejection Ratio -Equivalent circuit & I/O characteristic -CMOS Differential Amplifier - Active load CMOS Differential Amplifier & & I/O characteristic Small signal gain & Effect of Driver gm on gain - lf biased CMOS Differential Amplifier	35 min
3.	**Conclusion** A pseudo –n MOS inverter is a CMOS inverter and is roughly equivalent to the n MOS inverter using a depletion load. It is called as pseudo as this configuration was in use in n MOS technology preceding the introduction of CMOS technology. The differential inverter has two differential inputs and produces two differential outputs.	5 min
4	**Questions / Answers** **Q1 What is Common Mode Rejection Ratio?** **Ans** CMRR = differential Gain/ Common Mode Gain. **Q2**.What is a TTL interface inverter? **A2.** It is a CMOS inverter which is of use in interfacing to TTL logic system.	5min

Assignment to be given:- NIL

Reference Readings:-

1.Digital Integrated Electronics – Taub & Schilling

2.Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian

3 Basic VLSI design- D.A. Pucknell & K. Eshraghian

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Lecture Plan -15

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: B

S. No.	TOPIC: STICK DIAGRAM	Time Allotted:-
1.	**Introduction** Stick diagram is an easy rule method of representing transistor design model by the help of stick bar diagram. Also it helps in understanding the design concept of transistor model and interconnection with the supplies (i/ps, o/ps, Vdd, GND)	5 min
2	**Division of the Topic** -A simple inverter (basic gates) transistor model -The rule for designing pMOS and nMOS transistors -Substitution of stick bar in place of transistors -Supplies interconnection and output drawn with the metal -Inputs connected to the serial and parallel models of transistors.	35 min
3.	**Conclusion** An easier method of design using transistors signifies pull up and pull down network separately with the help of colored bar.	5 min
4	**Questions / Answers** **Q1** What is the significance of Stick Diagram? **Ans** An easier method of design using transistors signifies pull up and pull down network separately with the help of colored bar diagram.	5min

Assignment to be given:- NIL

Reference Readings:-

1.Digital Integrated Electronics – Taub & Schilling
2.Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian
3 Basic VLSI design- D.A. Pucknell & K. Eshraghian

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Lecture Plan -16

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: B

S. No.	TOPIC: LAMBDA BASED RULES	Time Allotted:-
1.	**Introduction** It is standard defined rule for construction of layout design for any transistor model. The rule signifies common rules setup for design rule check (DRC). It depends on technological parameter i.e the size length, which is common factor for low area devices. The following rules describe the min. gap required for different construction material such as poly silicon, diffusion and metal.	5 min
2	**Division of the Topic** -An inverter layout -The distance gap within different construction material used for transistor model. -Design Rule Check -Channel length parameter -Latest technology trends	35 min
3.	**Conclusion** Standard rules defined for construction of layout and complied with the DRC whether generated layout have some error or not.	5 min
4	**Questions / Answers** **Q1 Simplify significance of scaling in terms of channel length?** **Ans** Channel length becomes general parameter of scaling the overall architecture of transistor model.	5min

Assignment to be given:- NIL

Reference Readings:-

1.Digital Integrated Electronics – Taub & Schilling
2.Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian
3 Basic VLSI design- D.A. Pucknell & K. Eshraghian

Doc. No.: DCE/0/15
Revision :00

Lecture Plan -17

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: B

S. No.	TOPIC: SUPER BUFFERS	Time Allotted:-
1.	**Introduction** When the inverter is used to drive very large capacitive load, delays occur. To avoid these delays, inverting or non-inverting gates are used to source and sink large amount of charge in short times, these buffers are called super buffers. It is the interface between small signal gates and large pad drivers.	5 min
2	**Division of the Topic** -Super Buffers classified into two type 1. Inverting Type 2. Non-Inverting Type	35 min
3.	**Conclusion** Super buffers are used to produce typically symmetric propagation delays within the logic circuit.	5 min
4	**Questions / Answers** **Q1 What is Super buffer?** **Q2.Discuss classification of Super Buffers in detail?** .	5min

Assignment to be given:- NIL

Reference Readings:-

1.Digital Integrated Electronics – Taub & Schilling

2.Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian

3 Basic VLSI design- D.A. Pucknell & K. Eshraghian

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Lecture Plan -18

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: B

S. No.	TOPIC: BICMOS AND STEERING LOGIC	Time Allotted:-
1.	**Introduction** BiCMOS is the third IC technology which is the combination of bipolar and CMOS features. It has advantage of higher bandwidth and low power dissipation. Steering Logic are the circuits that route data inputs to outputs based on the setting of control signals.	5 min
2	**Division of the Topic** -BiCMOS Features - Gates design BiCMOS -Steering Logic through multiplexer -Few examples implementation by Steering logic	35 min
3.	**Conclusion** BiCMOS Logic is one of the latest IC technology that have advantage of both bipolar and CMOS devices. Steering Logic is an easier representation of logic functions using mux combinations.	5 min
4	**Questions / Answers** **Q1 Describe the features of BiCMOS?** **Q2**.Design Half Adder using Steering Logic?	5min

Assignment to be given:- NIL

Reference Readings:-

1.Digital Integrated Electronics – Taub & Schilling
2.Principles of CMOS VLSI Design – Neil H.E. Weste & K. Eshraghian
3 Basic VLSI design- D.A. Pucknell & K. Eshraghian

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Lecture Plan -19

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: C

S. No.	Topic :- STRUCTURED DESIGN OF COMBINATIONAL CIRCUITS	Time Allotted:-
1.	**Introduction** Design of combinational circuits can be easily discussed with the help of any Boolean expression. The simplified Boolean expression easily implemented in terms of PMOS (Pull Up) and NMOS (Pull Down) network. Both the network combined together for CMOS implementation.	5 min
2	**Division of the Topic** - Combinational circuit Boolean expression minimization - Expression realization with the pMOS - Expression realization with the nMOS - Realization of digital circuits using cMOS	35 min
3.	**Conclusion** Any combinational circuit can be designed with the help of Boolean expression using CMOS implementation.	5 min
4	**Questions / Answers** **Q1 What is combinational circuits?** **A 1 It** is the simple circuit in which output dependent on present inputs. **Q2 Relate Pull up network to Pull down network.**	5min

Assignment to be given:-
Define various parameters used in the MOS and latch up susceptibility?
Reference Readings:-
Principles of CMOS VLSI: Design:……By Neil H. E. Weste.

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Lecture Plan -20

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: C

S. No.	Topic :- THE TRANSMISSION GATE & TRI STATE INVERTER	Time Allotted:-
1.	**Introduction** A transmission gate is a very important element of a semiconductor memory and register. It is a gate formed by paralleling of a n MOS and p MOS with a common input to common drain/source and its transmission is controlled by complementary clock signal at the gates. Transmission gates can be formed with only MOS devices or with CMOS devices.	5 min
2	**Division of the Topic** - Basic circuit for CMOS transmission gate - n MOS pass transistor - p MOS pass transistor - Transmission gate characteristics - Tristate inverter	35 min
3.	**Conclusion** The transmission gate is a fundamental and ubiquitous component in MOS logic. It finds use as a multiplexing element, a logic structure, a latch element, and an analog switch. It also acts as a voltage controlled resistor connecting the input and output. By cascading a transmission gate with an inverter we get a tristate inverter whose output is in a tristate condition.	
4	**Questions / Answers** **Q1 What is the function of Transmission gate?** **A 1 It** transmits the input logic to pass through under conditions controlled by another input such as a clocking signal. **Q2 State some applications of transmission gate.** **A2** Memory cell/register, multiplexing element, a logic structure, a latch element, analog switch etc.	5 min 5min

Assignment to be given:-
Define various parameters used in the MOS and latch up susceptibility?
Reference Readings:-
Principles of CMOS VLSI: Design:……By Neil H. E. Weste.

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Lecture Plan -21

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: C

S. No.	Topic :- MOS CIRCUITS AND LOGIC DESIGN	Time Allotted:-
1.	**Introduction** we will discuss CMOS logic configurations to the fully Complimentary CMOS logic gate. The objective is to find the range of options that may be useful in a design situation. We will also discuss the physical layout of CMOS gates to examine the impact of the physical structure on the behavior of the circuit. We also discuss CMOS logic structures and clocking strategies. The objective is to find the range of options that may be useful in a design situation.	5 min
2	**Division of the Topic** 1. Design Considerations 2. Basic Physical Design of Simple Logic Gates 3. V-I CMOS Logic Structures 4. Clocking Strategies	35 min
3.	**Conclusion** Hence every useful VLSI system must store some state as storage element. Outputs are fed back to the inputs via storage devices that are clocked by a system clock. The storage devices used are defined in terms of a set of clock waveforms used to store and access the state of each storage element. The selection of a particular clocking strategy influences how many transistors are used per storage element and how many clock signals need to be routed throughout the chip. The storage devices used are defined in terms of a set of clock waveforms used to store and access the state of each storage element. The selection of a particular clocking strategy influences how many transistors are used per storage element and how many clock signals need to be routed throughout the chip.	5 min
4	**Questions / Answers** **Q1 What are the CMOS logic gate design considerations?** **Ans** Fan-in , Fan-out, CMOS NAND and NOR Delays **Q2 What are the various types of clocking strategies?** Ans Phase Locked Loop Clock Techniques, Two Phase Clocking, Two Phase Memory Structures. Four Phase Clocking.	5min

Assignment to be given:- What are the various logic designs in MOS circuits?

Reference Readings:-

Principles of CMOS VLSI: Design:……By Neil H. E. Weste.

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Lecture Plan -22

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section: C

S. No.	Topic :- CIRCUIT CHARACTERIZATION & PERFORMANCE ESTIMATION	Time Allotted:-
1.	**Introduction** An MOS structure is created by superimposing a number of layers of conducting, insulating and transistor forming materials. In this lecture we will discuss the understanding of system behavior that will provide the basis whereby systems performance in terms of signal delays and power dissipation can be estimated.	5 min
2	**Division of the Topic** Estimation of R 1. Resistance of Nonrectangular Regions 2. Contact and Via Resistance Estimation of C	35 min
3.	**Conclusion** Hence the resistance of a conductor on a layer is obtained by multiplying the sheet resistance Rs by the ratio of the length to width of the conductor.	5 min
4	**Questions / Answers** Q What is the resistance of non-rectangular regions? Ans Break the shape of total resistance into simple regions and then calculate the resistance.	5min

Assignment to be given:-Nil

Reference Readings:-

Principles of CMOS VLSI: Design:……By Neil H. E. Weste.

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Lecture Plan -23

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section:C

S. No.	Topic:- LEFT/RIGHT SHIFT SERIAL/PARALLEL REGISTER	Time Allotted:-
1.	**Introduction** Left/right Shift serial/parallel register is a register circuit which is a bi-directional type i.e. it can shift the bits to the left as well as to the right. The input may be given serially or parallely and the output may be obtained in serial form at either end of the register	5 min
2	**Division of the Topic** 1) Refresh loop 2) Parallel load mode 3) Shift right mode 4) Shift left mode 5) Parallel out put 6) Isolation of inverters	35 min
3.	**Conclusion** The system is restricted to shift of one bit only in either direction and hence any shift of more bits will take proportionality more time. The register uses two phase non-overlapping clock of which φ_1 allows loading shifting and refreshing to occur while φ_2 isolates the two inverters so that the cells may be loaded.	5 min
4	**Questions / Answers** **Q What is a shift register?** Ans This is a register circuit that can store the bits by shifting the bits.	5min

Assignment to be given:-Nil
Reference Readings:-
Basic VLSI Design ……By Pucknell

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Lecture Plan -24

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section:D

S. No.	Topic:- SWITCHING CHARACTERISTICS & POWER DISSIPITION	Time Allotted:-
1.	**Introduction** we will discuss analytical and empirical models that describe the switching characteristics of a CMOS inverter. These models are used to understand the parameters that affect CMOS delays. The components that establish the amount of power dissipated in a MOS circuit are Static dissipation which is due to leakage current or other current drawn continuously from the power supply and Dynamic dissipation which is due to switching transient current and charging and discharging of load capacitance.	5 min
2	**Division of the Topic** Analytic Delay Models of -Rise Time, t_r, -Fall Time, t_f, -Delay Time, t_d Empirical Delay Models Gate delays -Static Dissipation -Dynamic Dissipation -Short Circuit Dissipation -Total Power Dissipation	35 min
3.	**Conclusion** The switching speed of a CMOS gate is limited by the time taken to charge and discharge the load capacitance CL. An input transition results in an output transition that either charges CL toward VDD or discharges CL toward VSS. The total power dissipation can be obtained from the sum of three dissipation components, so that Ptotal = Ps + Pd + Psc	5 min
4	**Questions / Answers** **Q1 What is the range rise time, fall time and delay time?** **Ans** Rise time- 10% to 90% Fall time- 90% to 10% Delay time- 50% **Q2 What is the expression of power dissipation?** **Ans** $P_d = C_L V_{dd}^2 f_p$	5min

Assignment to be given:-Nil

Reference Readings:-

Principles of CMOS VLSI: Design:……By Neil H. E. Weste.

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Lecture Plan-25

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section:D

S. No.	Topic :-USE OF CAD TOOLS AND INTRODUCTION TO VHDL	Time Allotted:-
1.	**Introduction:-** VHDL is an acronym for VHSIC Hardware Description Language .It is a hardware description language that can be used to model a digital system at many levels of abstraction, ranging from the algorithmic level to the gate level. The language can be used as an exchange medium between chip vendors and CAD tool users. It can also be used as a communication medium between different CAD and CAE tools.	10 min
2	**Division of the Topic** □ Introduction to CAD tools □ Use of CAD tools □ Introduction to VHDL	30 min
3.	**Conclusion:** VHDL is used to describe a model for a digital H/W device. This model specifies the external view of the device and one or more internal views. The internal view of the device specifies the functionality or structure, while the external view specifies the interface of the device through which it communicates with other models in its environment.	5 min
4	**Question / Answer** Q1 What is HDL and VHDL? Ans HDL is Hardware Description Language where as VHDL is Very High Speed Integrated Circuit Hardware description Language. Q2 What are the capabilities of the language? Ans It supports Hierarchy, flexible design methodologies, not-technology specific, supports synchronous and asynchronous timing models.	5 min

Assignment to be given:- Applications of CAD tools.
Reference Readings:- A VHDL Primer ……By J. Bhaskar.

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Lecture Plan -26

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section:D

S. No.	Topic:- VHDL BASIC LANGUAGE ELEMENTS	Time Allotted:-
1.	**Introduction:** A Hardware abstraction of this digital system is called an entity. An entity X, when used in another entity Y , becomes a component for the entity Y. Therefore a component is also an entity, depending on the level at which it is modeled. It provides five different design units: Entity Declaration, Architecture body, Configuration Declaration, Package Declaration and Package Body.	10 min
2	**Division of the Topic** VHDL Basic Language Elements – Entity Declaration, Architecture body, Configuration Declaration, Package Declaration and Package Body. Architecture body specifying the internal details can be modeled as:- - Structural Modeling - Data Flow Modeling - Behavioral Modeling	30 min
3.	**Conclusion:** This lecture provided a brief overview of the major aspects of the language. Some of the other important features like types, overloading, and resolution functions, were not discussed which will be covered later.	5 min
4.	**Question / Answer** Q1 Draw the entity model of half adder circuit. Q2. Draw a 2-to- 4 Decoder circuit.	5 min

Assignment to be given:-
1. Do the data flow modeling of 2*4 decoder
2. Do the Behavioral modeling of multiplexer.

Reference Readings:- A VHDL Primer ……By J. Bhaskar.

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Lecture Plan -27

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section:D

S. No.	Topic:- DATA OBJECTS,CLASSES,DATA TYPES, OPERATORS	Time Allotted:-
1.	**Introduction:** This lecture describes the basic elements of the language. These include data objects that store values of a given type, literals that represent constant values and operators that operate on data values. Every data object belongs to a specific type. The various categories of types and the syntax for specifying user defined types will also be discussed.	5 min
2	**Division of the Topic** Data Objects- Data Objects holds a value of a specified type. Every data object belongs to one of the following four classes: • Constant • Variable • Signal • File All possible types that can exist in the language can be categorized into the following four major categories: • Scalar Type • Component Types • Access Types • File Types	35 min
3.	**Conclusion**: It is important to understand the notion of data objects as VHDL is a strongly typed language. It does not allow objects and literals of different types to be mixed freely in expressions.	5 min
4	**Question / Answer** Q1 How are data objects of VHDL different from data objects of C language. Q2 Write the syntax for file data objects.	5min

Assignment to be given:-NIL

Reference Readings:- A VHDL Primer ……By J. Bhaskar.

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Lecture Plan -28

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section:D

S. No.	Topic:- INTRODUCTION TO BEHAVIORAL ,STRUCTURAL AND DATAFLOW MODELING	Time Allotted:-
1.	**Introduction**:-In this lecture we will study the three styles of modeling. Dataflow style specifies how data will be transferred from signal to signal and input to output.In structural style entity is described as a set of interconnected components.In Behavioural style, entity is described as a set of Sequential statements.	5 min
2	**Division of the Topic** Introduction to Three Modelling styles - Dataflow Modelling - Structural Modelling - Behavioural Modelling	35 min
3.	**Conclusion:** An entity declaration describes the external interface of the entity, ie, it gives the black- box view. An architecture body describes the internal view of an entity. It describes the functionality or the structure of the entity.	5 min
4	**Question / Answer** Q1 Give the Structural Modelling of a half adder circuit. Q2 Write architecture body of 2:4 decoder using Dataflow Modelling	5min

Assignment to be given:-NIL

Reference Readings:- A VHDL Primer ……By J. Bhaskar.

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Lecture Plan -29

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section:D

S. No.	Topic:- LIBRARIES AND PACKAGES	Time Allotted:-
1.	**Introduction**: In this lecture we will discuss about packages and how compiled design units are stored in design libraries. It explains how the contents of design units stored in different libraries may be shared by several design units.	5 min
2	**Division of the Topic** • Libraries and Packages • Overloading	35 min
3.	**Conclusion**: Hence a package provides a convenient mechanism to store and share declarations that are common across many design units. A compiled design unit is stored in a design library. A design library is an area of storage in the file system of the host environment.	5 min
4	**Question / Answer** Q1 Write the syntax for package declaration. Q2 Which is a library that is predefined in the language? Ans STD	5min

Assignment to be given:-Nil
Reference Readings:-
Moris mano, R P Jain, J. Bhaskar

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Lecture Plan -30

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section:D

S. No.	Topic:- PROGRAMMABLE LOGIC DEVICES	Time Allotted:-
1.	**Introduction** The semiconductor memories can be programmed to provide logic functions in the sum of logic function.	5 min
2	**Division of the Topic** □ Programmable Logic Devices. □ Programmable Array Logic □ Programmable Logic Array □ FPGA □ ROM □	35 min
3.	**Conclusion** PLDs consists of AND-OR logic with inverters and it can be programmed to give logic function at the o/p as per required.	5 min
4	**Question / Answer** Q1- how many different locations can be selected by using 16 address lines? A1-65536	5min

Assignment to be given:-Nil
Reference Readings:-
Basic VLSI Design ……By R.P.JAIN

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Lecture Plan -31

Semester:-6th Course Code:-EE-306-F

Subject:-VLSI DESIGN Section:D

S. No.	Topic:- ROM,PLA, PAL, FPGA & CPLD's	Time Allotted:-
1.	**Introduction** These are programmable logic devices. A programmable logic device is an IC that is user configurable and is capable of implementing logic functions. It is an LSI chip that contains a regular structure and allows the designer to customize it for any specific application i.e. it is programmed by the user to perform a function required for his application.	5 min
2	**Division of the Topic** -ROM(Read Only Memory) as PLD -PLA(Programmable Logic Array) and PAL(Programmable Array Logic) -FPGA(Field Programmable Gate Array) -CPLD's(Complex Programmable Logic Devices)	35 min
3.	**Conclusion** These types of devices help in designing of very complex circuits. These reduce the board space requirement and reduced power requirement.	5 min
4	**Question / Answer** Q1 Discuss various programmable devices Q2 What is PLA A2 Programmable Logic Array Q3 What are the advantages of FPGA over PLA A3 Complex circuit can be designed easily	5min

Assignment to be given:-Nil

Reference Readings:-

Basic VLSI Design ……By R.P.JAIN