Differential Amplifier

Differential amplifiers

Classification of closed loop differential amplifier with negative feedback according to the no. of op-amp used. That is,
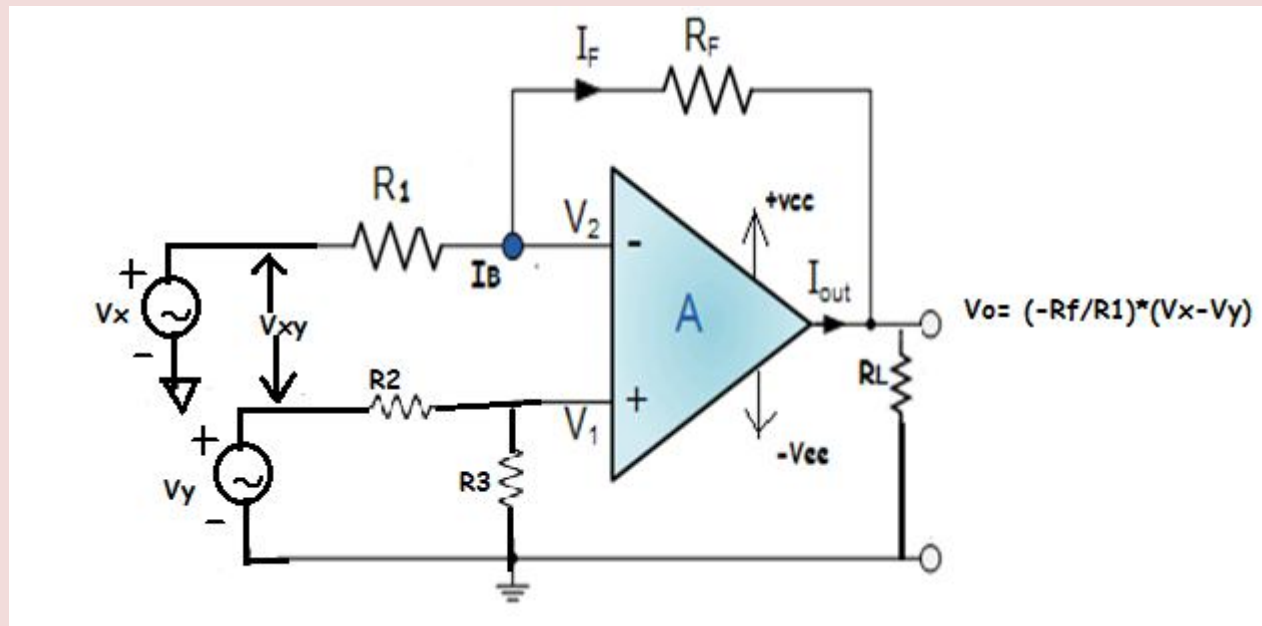
1.Differential amplifier with one op-amp

2.Differential amplifier with two op-amp

Differential amplifiers are used in instrumentation and industrial applications to amplify differences between two input signals.

Differential amplifier are preferred over single ended because they are better able to reject common mode (noise) voltages than single input circuits such as inverting and non-inverting amplifiers.

Diff amp. Enables us to bias the amplifier and to couple amplifier stages together without the need of bypass and coupling capacitors.

Differential amplifier with one op-amp

Voltage gain $A_D = V_o/V_{xy} = -R_f/R_1$

Input Resistance Rif is determined looking into either one of the two terminals with other grounded.
$R_{iFx} = R_1$ with $V_y = 0V$
$R_{iFy} = (R_{2+} R_3)$ with $V_x = 0V$

- ## Differential amplifier operated in 3 different modes:

1) **Single ended mode**: when input signal is applied to only one of the two input terminals i.e. either of the two input is zero, then differential amp will be in single ended mode. In this mode,diff amp will act either as an inverting or non inverting amplifier depending on whether the signal is applied to the inverting or non inverting.

2) **Differential mode**: In this mode of operation ,magnitude of two input signals may be same or different but their polarity is opposite at every instant of time.

$V_x = -V_y$, $V_{in} = V_x - V_{y=} 2 V_x$ Hence $V_o = -(R_f/R_{1)} (V_x - V_y) = -2 (R_f/R_1) V_x$

3) **Common mode**: In this mode the two input signals are same in magnitude as well as in phase at every instant of time. So $V_x - V_y = 0$ and $V_o = 0$

Emitter coupled logic

- Differential amplifier is basic block of analog circuit.

- It is the input stage of virtually every opamp, and basis of high speed digital logic circuit family, called emitter coupled logic.

- Differential amplifier, amplifies the difference between two input signals.

Emitter-coupled differential pair

The emitter-coupled differential pair is a very important circuit that is used in many bipolar analog integrated circuits.

The circuit is shown in the figure and the two transistors are assumed identical. The current source I_{EE} is typically implemented as a current source circuit.
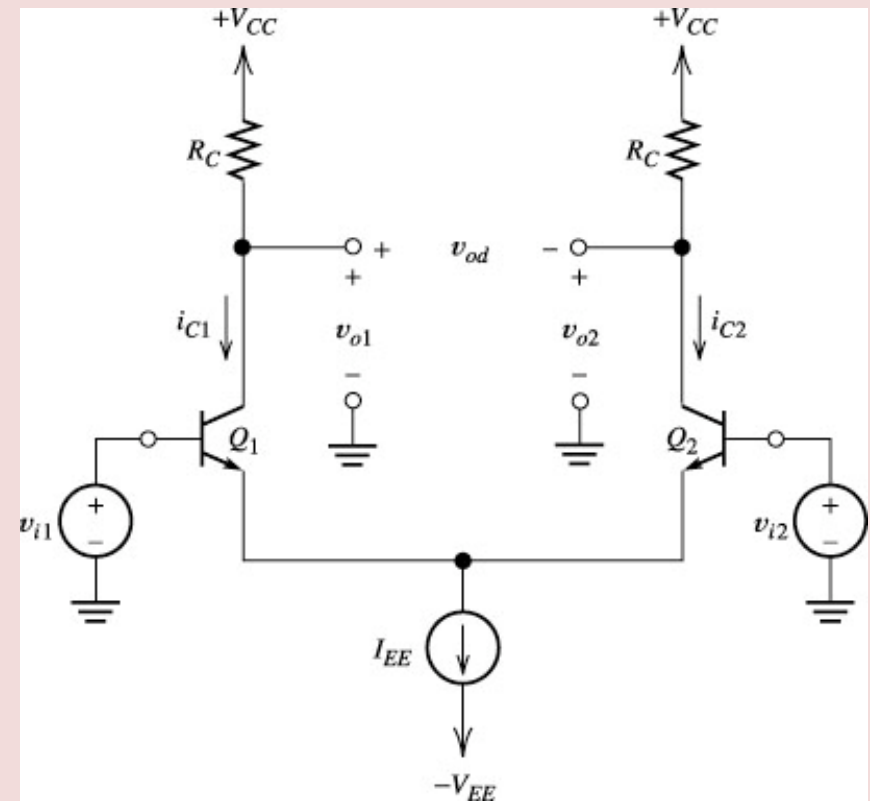
The input voltages vi1 and vi2 can be considered to be composed of a differential signal v_{id} and a common mode signal v_{icm} defined below:

Q1 and Q2 in remain in forward bias.

$$v_{id} = v_{i1} - v_{i2}$$
$$v_{icm} = 1/2(v_{i1} + v_{i2})$$

Differential output voltage is defined as

$$v_{od} = v_{o1} - v_{o2},$$
$$\text{since} \quad v_{o1} = V_{CC} - R_C i_{C1}, v_{o2} = V_{CC} - R_C i_{C2}$$
$$\text{so} \quad v_{od} = R_C(i_{C2} - i_{C1})$$

Figure: Basic BJT differential amplifier.

Emitter-coupled differential pair II

First, consider the two input signal vi1 and vi2 are equal. Then the differential input voltage vid is 0 and we have a pure common-mode input signal.

In this case, the current IEE splits equally between the Q1 and Q2, therefore vod=0.

In other words, the circuit does not respond to the common-mode component of the input.

(a) Common-mode input signal ($v_{i1} = v_{i2}$)
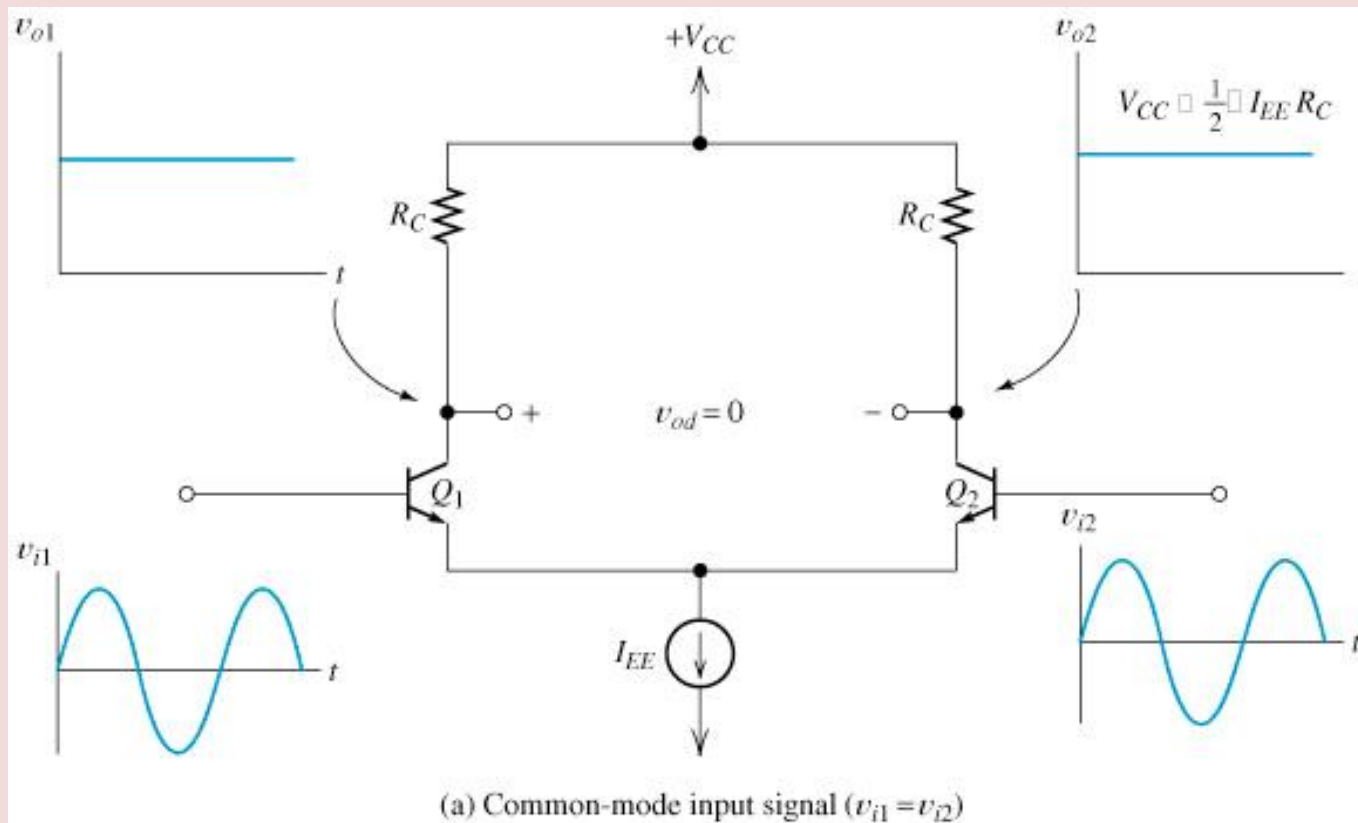
Figure : Basic BJT differential amplifier with waveforms.

Emitter-coupled differential pair III

For a pure differential input (when v_{icm}=0), it can be shown that a non-zero differential output voltage v_{od} is resulted, as a differential input signal steers I_{EE} toward one side or the other.

In summary, the circuits rejects common-mode input and responds to the differential input. In amplifiers, a small differential input signal is amplified to a differential output signal.
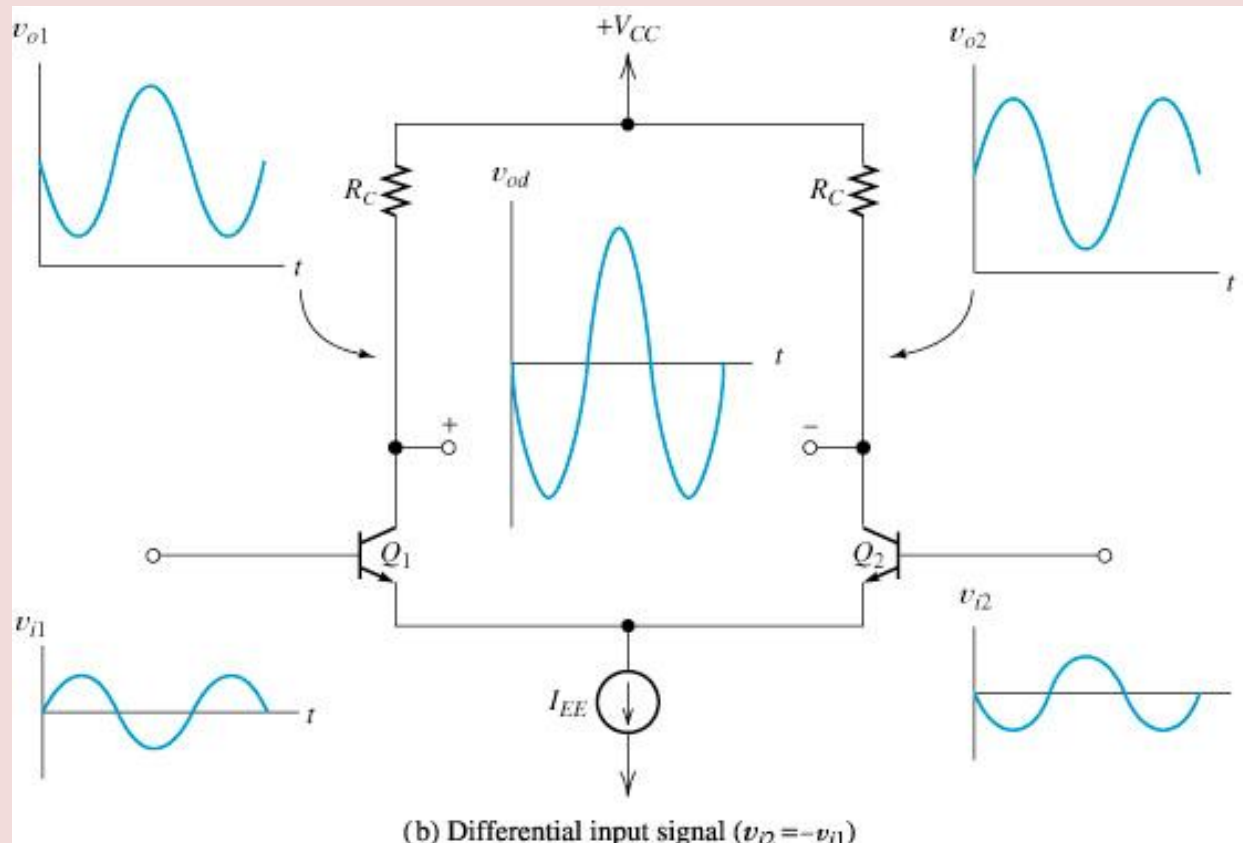
Figure : Basic BJT differential amplifier with waveforms.
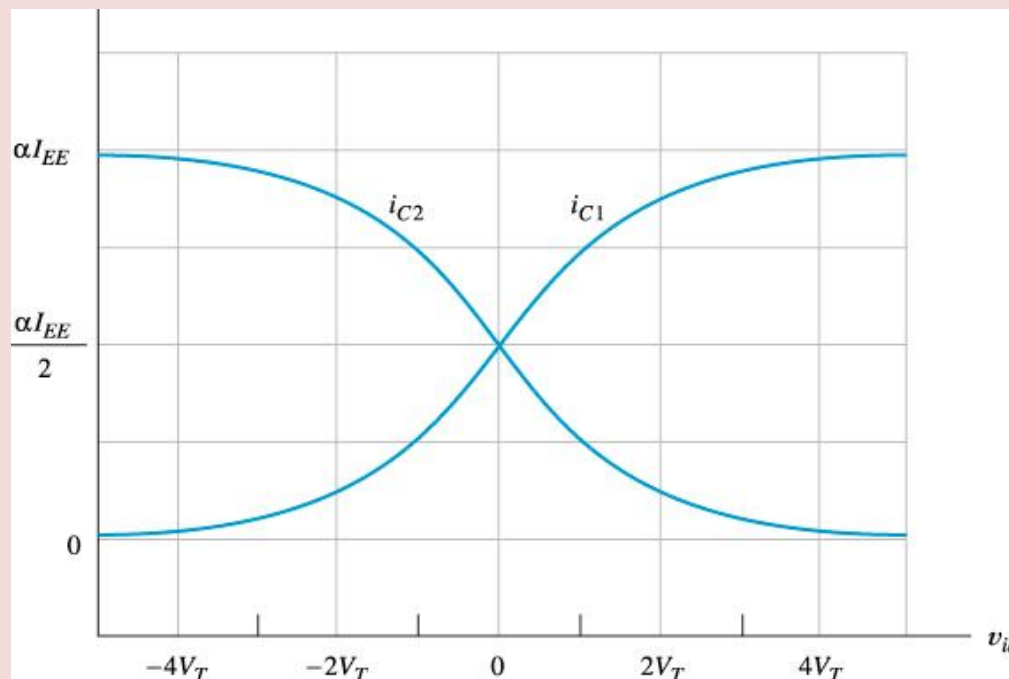
Transfer characteristics of Differential amp.

The following collector current versus differential input voltage can be obtained.

$$i_{C1} = \frac{I_{EE}}{1 + \exp(v_{id}/V_T)} , i_{C2} = \frac{I_{EE}}{1 + \exp(+v_{id}/V_T)}$$

Note that in the plot, when vid=0, ic1=ic2.

Figure : Collector currents versus differential input voltage.

Important definitions

- **Input Common-mode range (ICMR)**

  ICMR is the range of common-mode voltages over which the differential amplifier continues to sense and amplify the difference signal with the same gain.

  Typically , ICMR is defined as common-mode voltage range over which all MOSFETs remain in the saturation region.

- Offsets:

  Output offset voltage (V_{OS}(out)) : It is defined as the voltage which appears at the output of the Diff Amp when the inputs terminal are shorted or grounded.

 **Input offset voltage (V_{OS}(in)) :** It is equal to the output offset voltage divided by the differential voltage gain - $V_{OS} = (V_{OS}(out) / A_{VD})$
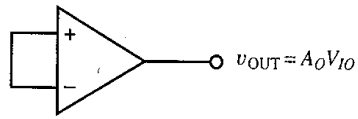
Input-Offset Voltage
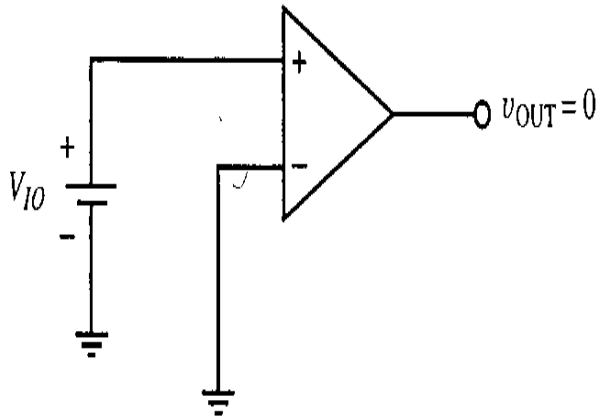
➤ Input offset voltage Vio is the differential input voltage that exists between two input terminals of an op-amp without any external inputs applied.

➤ Or in other words, **it is the amount of input voltage that should be applied between two input terminals in order to force the output voltage to zero.**

➤ The input-offset voltage (labeled Vio in the figure at the left) can be positive or negative and is usually small (anywhere from 1 uV to 10 mV)

➤ Typical value of input offset voltage +- 2mv for 741.
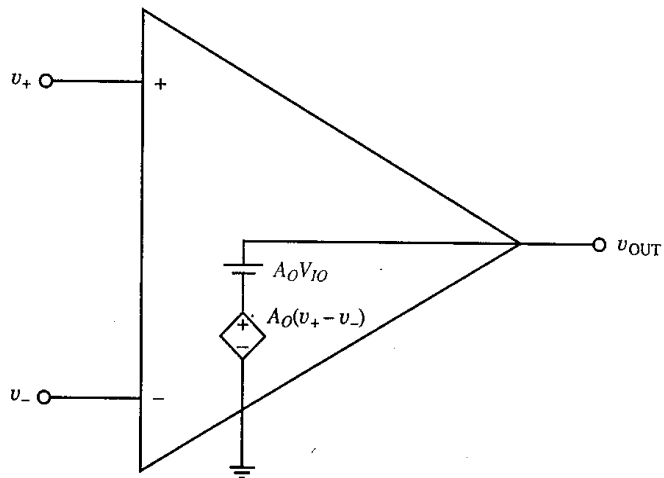
Input-Offset Voltage Effect on Output Voltage
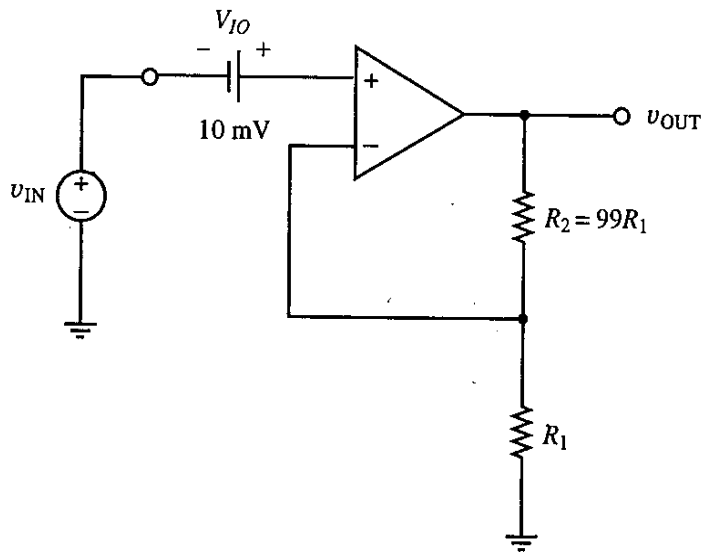
- To examine the effect input-offset voltage has on the output voltage, consider the non-inverting op-amp
  - The gain of the op-amp is (R1 + R2)/R1 = 100
  - Assume the input voltage is modelled adequately by a source V_{IO} = +/- 10 mV
  - Then, we can write that the output voltage is given by

    $v_{OUT} = (v_{IN} + V_{IO})(R1 + R2)/R1$
    $= 100\ v_{IN}\ +/-\ 1\ \text{volt}$
  - Thus, a 10 mV input-offset causes a 1V offset in v_{OUT}

# Output-Offset Voltage and Nulling Out Offset

(a)

(b)

- A parameter called the **output-offset voltage** may be used to represent the internal imbalance of an op-amp, rather than the input-offset voltage
  - **The output-offset voltage is defined as the measured output voltage when the input terminals are shorted together,** as shown at the left-top fig.

  - The output-offset voltage may be modelled by placing a voltage source A_oV_{IO} in series with the output voltage source $A_o(v_+ - v_-)$
    - Consequently, the output-offset voltage is essentially the input-offset voltage multiplied by the open loop gain.

13

Non-zero Input Bias Currents
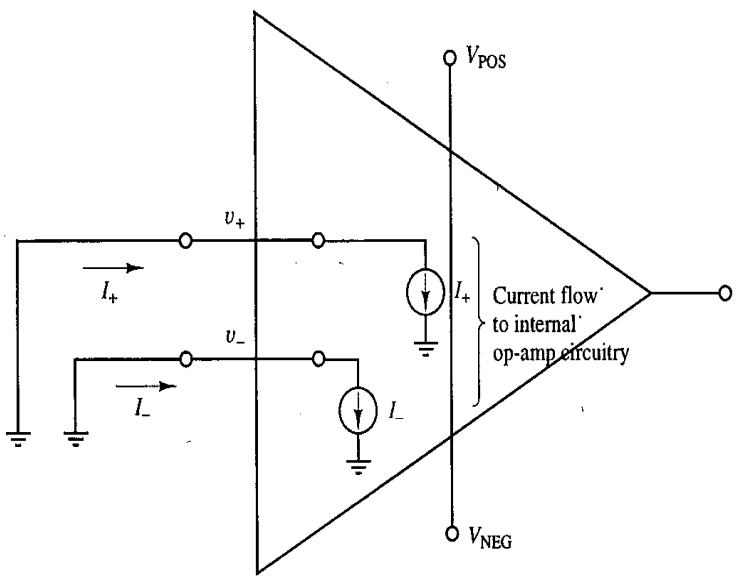
- In practice op-amps do not actually have zero input currents, but rather have very small input currents labeled I_+ and I_- in the figure at the left
  - Modeled as internal current sources inside op-amp
  - I_+ and I_- are both the same polarity

  - In order to allow for slightly different values of I_+ and I_-, we define the term I_{BIAS} as the average of I_+ and I_-

$$I_{BIAS} = ½ (I_+ + I_-)$$

- An input bias current is defined as average of the two input bias currents, I_+ and I_- .
- I_+ =dc bias current flowing into the non inverting input
- I_- = dc bias current flowing into the inverting input

- Value of bias current is very small ,in the range of few hundred nano Amps.Its a dc current
- Typical value of I_{bias} is 500nA max. At Supply voltages +-15v dc for 741.

Input Offset Current Definition

- Non-zero input bias currents I+ and I- may not always be equal (some opamps)

- We define a parameter "input offset current" used as an indicator of the degree of mismatching between these two currents.
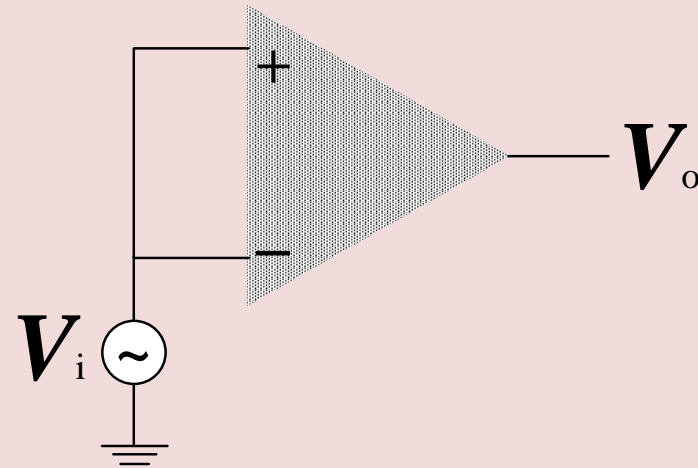
  $$I_{IO} = I_+ - I_-$$

  - Typical values of I_{IO} are 5-10% (of I-) although it can be as high as 50%
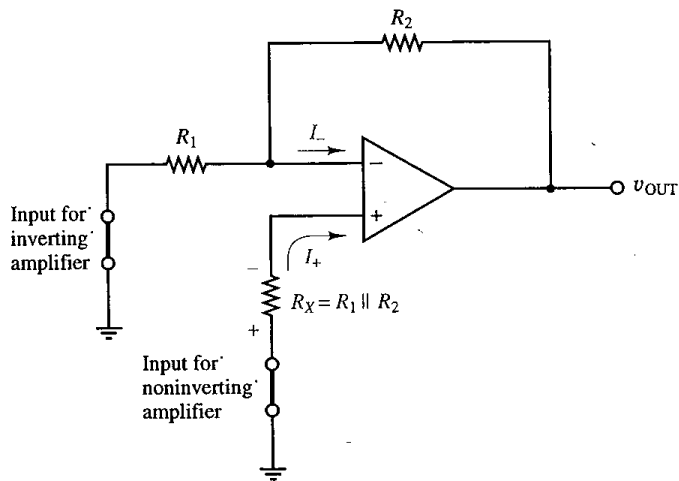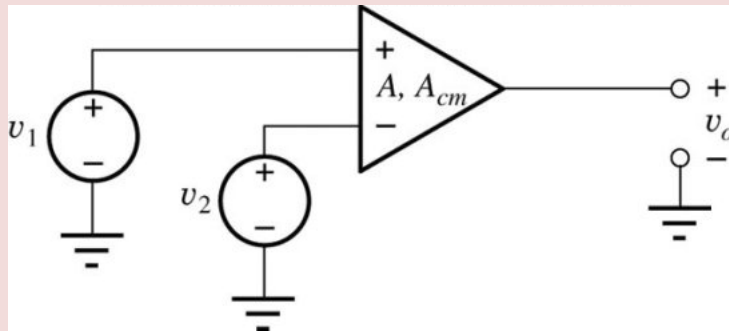
Common-Mode Operation

- Same voltage source is applied at both terminals

- Ideally, two input are equally amplified

- Output voltage is ideally zero due to differential voltage is zero

- Practically, a small output signal can still be measured

Note for differential circuits:
Opposite inputs : highly amplified
Common inputs : slightly amplified

$\Rightarrow$ Common-Mode Rejection

Finite Common-Mode Rejection Ratio (CMRR)

A(or A_{dm}) = differential-mode gain

A_{cm} = common-mode gain

v_{id} = differential-mode input voltage

v_{ic} = common-mode input voltage

$$v_1 = v_{ic} + \frac{v_{id}}{2} \qquad v_2 = v_{ic} - \frac{v_{id}}{2}$$

A real amplifier responds to signal common to both inputs, called the common-mode input voltage (v_{ic}). In general,

$$v_o = A_{dm}(v_1 - v_2) + A_{cm}\left(\frac{v_1 + v_2}{2}\right)$$

$$v_o = A_{dm}(v_{id}) + A_{cm}(v_{ic})$$

An ideal amplifier has $A_{cm} = 0$, but for a real amplifier,

$$v_o = A_{dm}\left(v_{id} + \frac{A_{cm}v_{ic}}{A_{dm}}\right) = A_{dm}\left(v_{id} + \frac{v_{ic}}{\text{CMRR}}\right)$$

$$\text{CMRR} = \left|\frac{A_{dm}}{A_{cm}}\right|$$

and $\text{CMRR(dB)} = 20\log_{10}(\text{CMRR})$

Finite Common-Mode Rejection Ratio: Example

- **Problem**: Find output voltage error introduced by finite CMRR.
- **Given Data**: A_{dm}= 2500, CMRR = 80 dB, v_1 = 5.001 V, v_2 = 4.999 V
- **Assumptions**: Op amp is ideal, except for CMRR. Here, a CMRR in dB of 80 dB corresponds to a CMRR of 10^4.
- **Analysis**:

$$v_{id} = 5.001\text{V} - 4.999\text{V}$$

$$v_{ic} = \frac{5.001\text{V} + 4.999\text{V}}{2} = 5.000\text{V}$$

$$v_o = A_{dm}\left(v_{id} + \frac{v_{ic}}{\text{CMRR}}\right) = 2500\left(0.002 + \frac{5.000}{10^4}\right)\text{V} = 6.25\text{V}$$
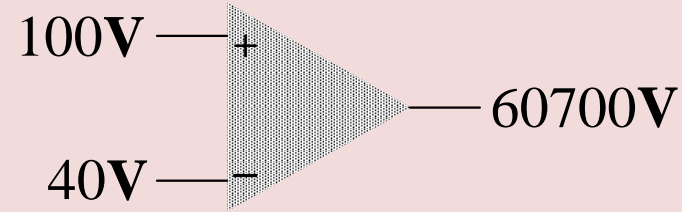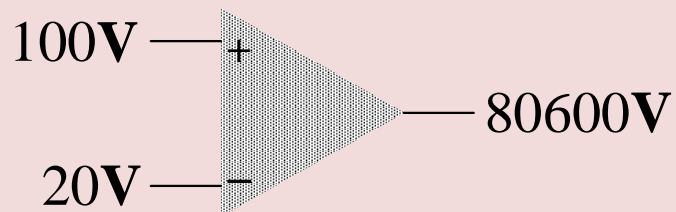
In the "ideal" case, $v_o = A_{dm} v_{id} = 5.00$ V

$$\% \text{ output error} = \frac{6.25 - 5.00}{5.00} \times 100\% = 25\%$$

The output error introduced by finite CMRR is 25% of the expected ideal output.

CMRR Example

What is the CMRR?

$$100\mathbf{V} \longrightarrow + $$
$$\longrightarrow 80600\mathbf{V}$$
$$20\mathbf{V} \longrightarrow -$$

$$100\mathbf{V} \longrightarrow +$$
$$\longrightarrow 60700\mathbf{V}$$
$$40\mathbf{V} \longrightarrow -$$

Solution :

$$\left. \begin{array}{l} V_{d1} = 100 - 20 = 80\mathbf{V} \\ V_{c1} = \dfrac{100 + 20}{2} = 60\mathbf{V} \end{array} \right\} (1)$$

$$\left. \begin{array}{l} V_{d2} = 100 - 40 = 60\mathbf{V} \\ V_{c2} = \dfrac{100 + 40}{2} = 70\mathbf{V} \end{array} \right\} (2)$$

From (1) $\quad V_o = 80G_d + 60G_c = 80600\mathbf{V}$

From (2) $\quad V_o = 60G_d + 70G_c = 60700\mathbf{V}$

$G_d = 1000$ **and** $\quad G_c = 10 \quad \Rightarrow \mathbf{CMRR} = 20\log(1000/10) = 40\mathbf{dB}$