8237 DMA Controller

Introduction

Direct memory access (DMA) is a process in which an external device takes over the control of system bus from the CPU.

DMA used for **high-speed data transfer** from/to mass storage peripherals, e.g.

Hard disk drive,
Magnetic tape,
CD-ROM, and sometimes video controllers.

Example

A hard disk transfer rate of 5 M bytes per second, i.e. 1 byte transmission every 200 ns. To make such data transfer via the CPU is both undesirable and unnecessary.

The basic idea of DMA is to transfer blocks of data directly between memory and peripherals. The data don't go through the microprocessor but the data bus is occupied.

Cont..

“Normal” transfer of one data byte takes up to 29 clock cycles.

The DMA transfer requires only 5 clock cycles.

Nowadays, DMA can transfer data as fast as 60 M byte per second. The transfer
rate is limited by the speed of memory and peripheral devices.

Features of 8237

1. It provides various modes of DMA.ing.
2. It provide on chip 4 independent channel. the no of channel can be increase by cascading.
3. Each channel can be use auto initialize mode.
4. It can transfer data between memory to memory.
5. In memory to memory transfer single word can be written in all location of memory block.
6. Address of memory is either increment or decrement.
7. Clock frequency 3Mhz.
8. Data transfer rate 1.6 Mbps/sec.

Continue..

9. Directly expendable to any no of channel by cascading.
10. It provide EOP line that is used for terminate DMA operation. This signal can be generated by external h/w.
11. DMA can be requested by setting an appropriate bit of request register.
12. Independent control for DREQ and DACK. These signal can be initialize by active high or low.
13. It provide compressed timing to improve throughput.it can compress the transfer time to two (2s)

Basic process of DMA

For 8088 in maximum mode:

The RQ/GT1 and RQ/GT0 pins are used to issue DMA request and receive acknowledge signals.

Sequence of events of a typical DMA process

1) Peripheral asserts one of the request pins, e.g. RQ/GT1 or RQ/GT0 (RQ/GT0 has higher priority)
2) 8088 completes its current bus cycle and enters into a HOLD state
3) 8088 grants the right of bus control by asserting a grant signal via the same pin as the request signal.
4) DMA operation starts
5) Upon completion of the DMA operation, the peripheral asserts the request/grant pin again to relinquish bus control.

Minimum mode

For 8088 in minimum mode:

The HOLD and HLDA pins are used instead to receive and acknowledge the hold request respectively.

Normally the CPU has full control of the system bus.

In a DMA operation, the peripheral takes over bus control temporarily.

DMA controller

A DMA controller interfaces with several peripherals that may request DMA.

The controller decides the priority of simultaneous DMA requests

communicates with the peripheral and the CPU, and provides memory

addresses for data transfer.

Conti..

DMA controller commonly used with 8088 is the 8237 programmable device.

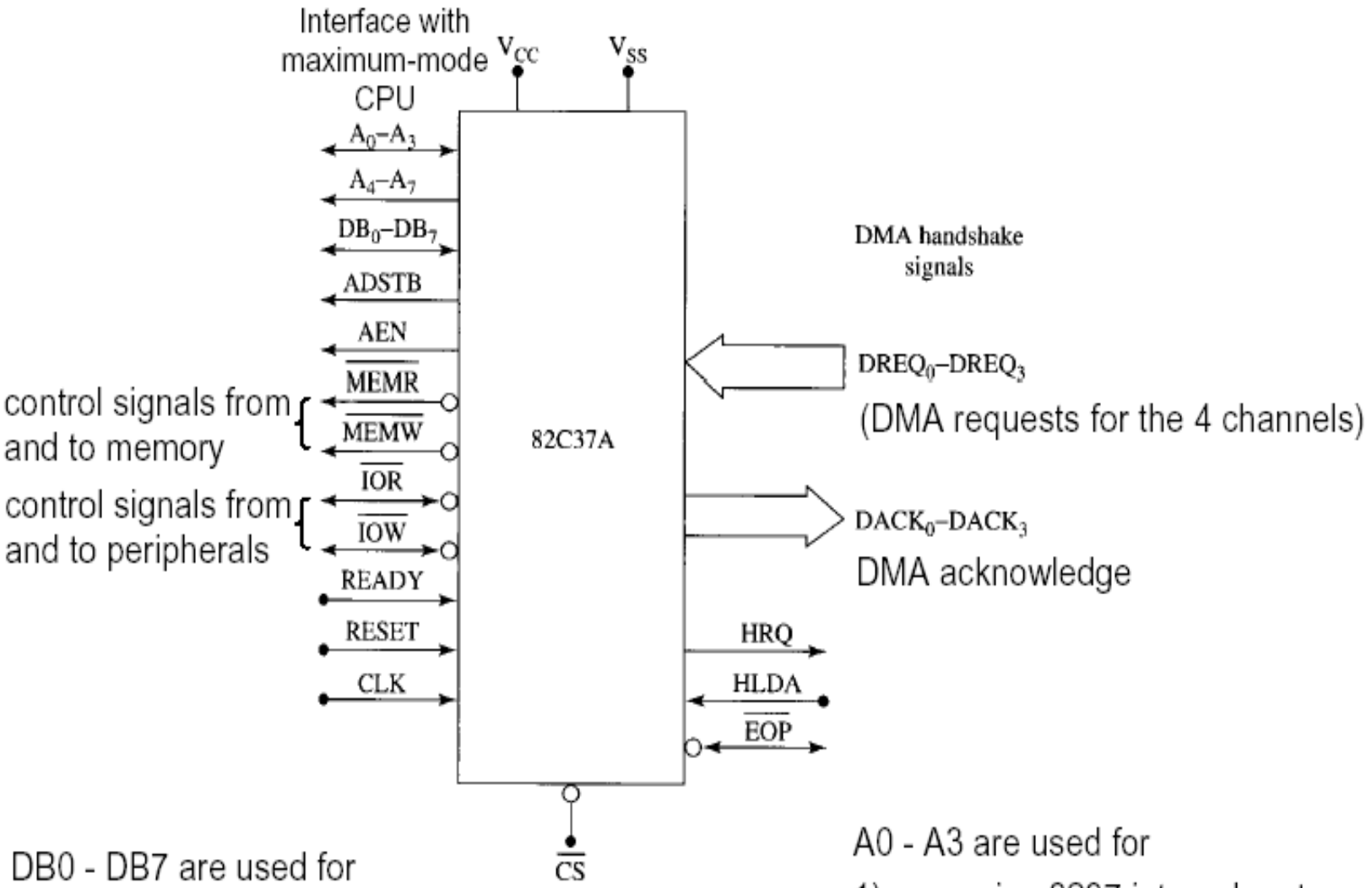
The 8237 is in fact a special-purpose microprocessor.

Normally it appears as part of the system controller chip-sets.

The 8237 is a 4-channel device.

Each channel is dedicated to a specific peripheral device and capable of addressing 64 K bytes section of memory.

8237 DMA controller

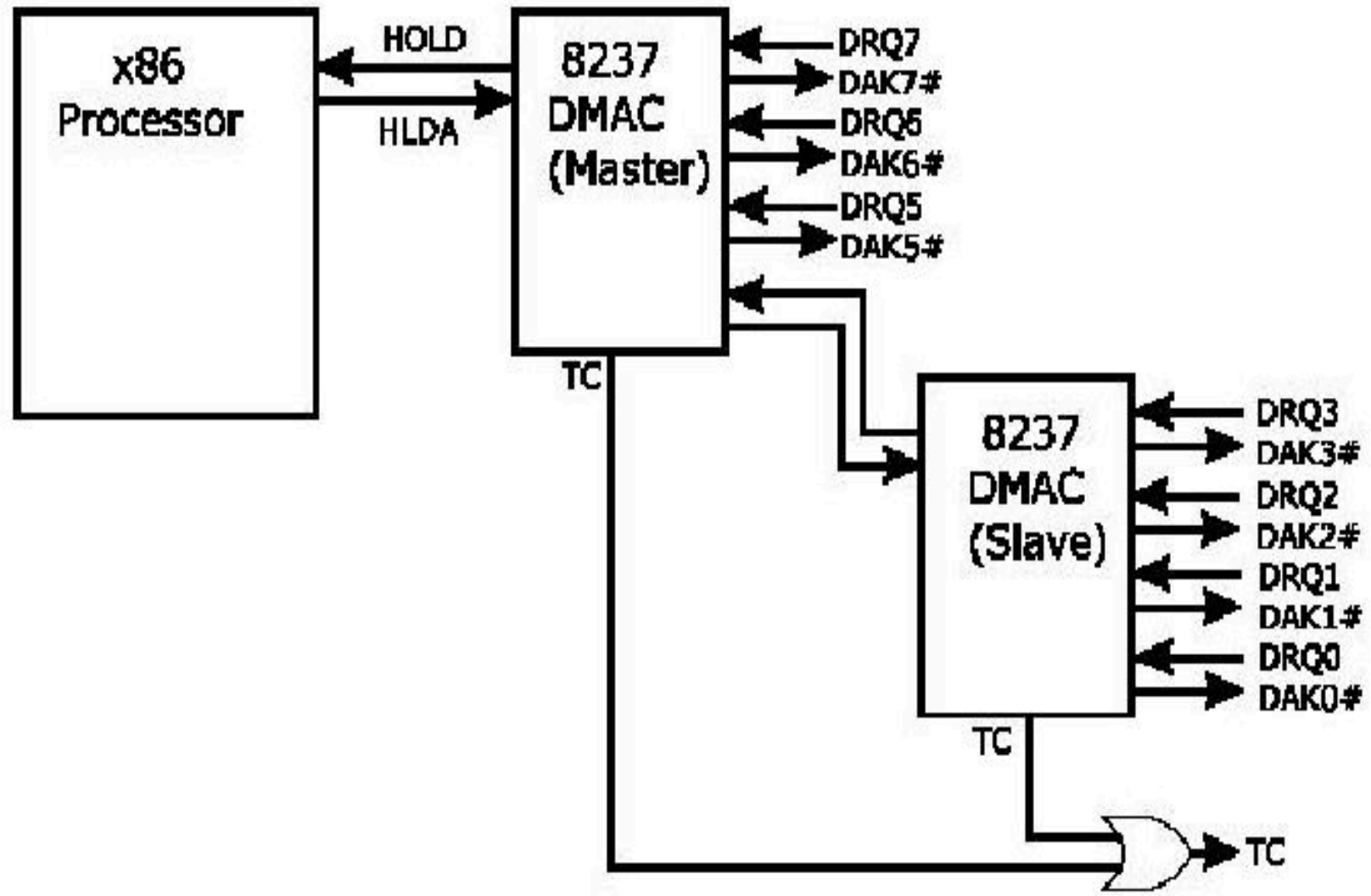


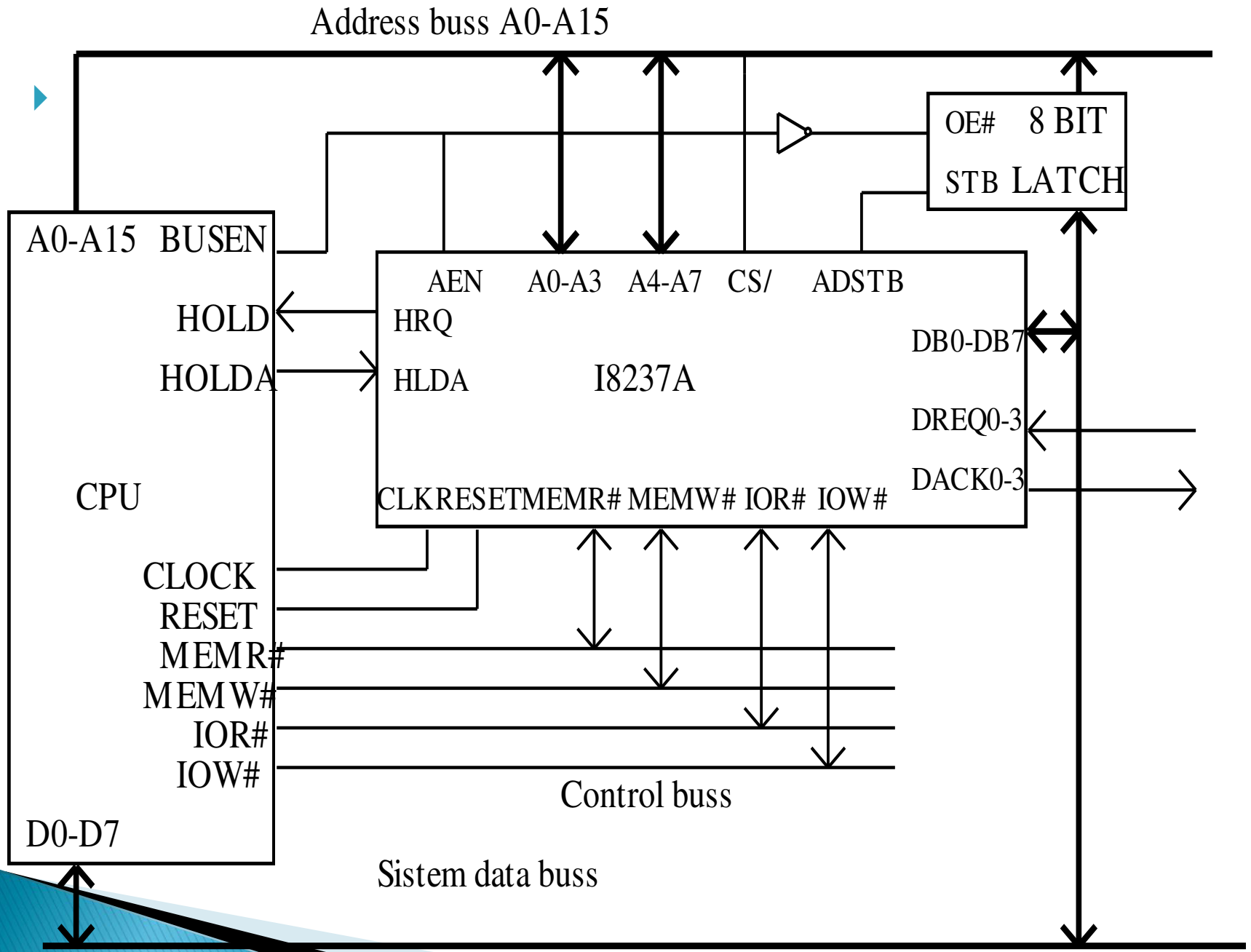
DB0 - DB7 are used for

1) transfer of data
2) 8237 programming

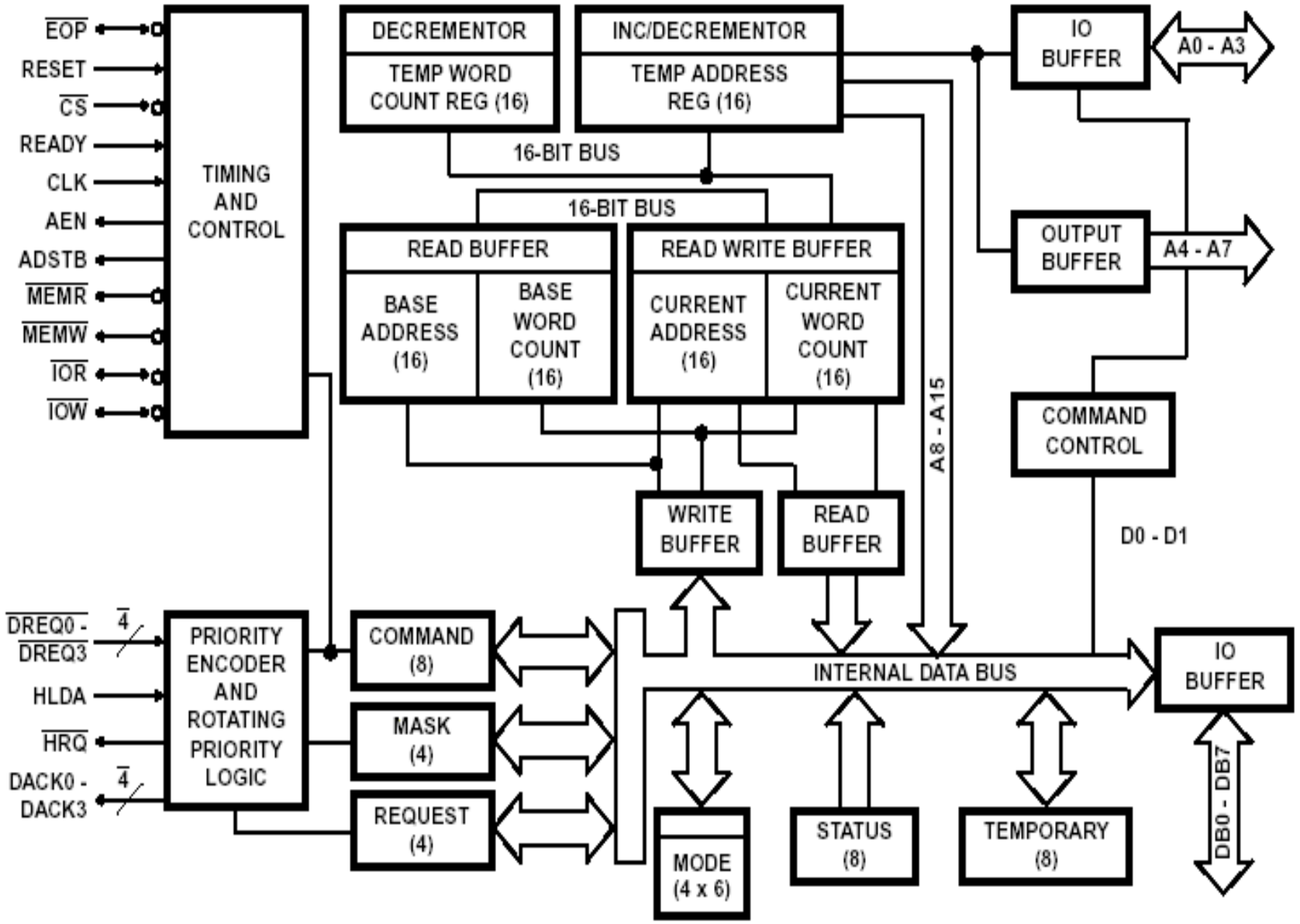
A0 - A3 are used for

1) accessing 8237 internal ports
2) carrying memory address in DMA read and write operations


x86
Processor
HOLD
HLDA
8237
DMAC
(Master)
DRQ7
DAK7#
DRQ6
DAK6#
DRQ5
DAK5#
TC
8237
DMAC
(Slave)
DRQ3
DAK3#
DRQ2
DAK2#
DRQ1
DAK1#
DRQ0
DAK0#
TC
TC


Address buss A0-A15
OE#
8 BIT
STB
LATCH
A0-A15
BUSEN
AEN
A0-A3
A4-A7
CS/
ADSTB
HOLD
HRQ
DB0-DB7
HOLDA
HLDA
I8237A
DREQ0-3
DACK0-3
CPU
CLK
RESET
MEMR#
MEMW#
IOR#
IOW#
CLOCK
RESET
MEMR#
MEMW#
IOR#
IOW#
Control buss
D0-D7
Sistem data buss

Block Diagram



8237 DMA

- Figure shows internal block diagram of 8237A it consists block of

- Control register and
- Internal register.

Control Logic

- 8237A contain three basic block of control logic.
- **i. Timing and control Block**. It generate internal timing and external control signal to the 8237A.
- **ii. Program command control Block**. It decodes various command given to the 8237 by the microprocessor before servicing a DMA request.it also decodes the mode control word,which is used to select the type of DMA during the servicing.
- **iii. Internal registers**. 8237 contain 344 bits of internal memory in the form of register which is shown in next slide

Name size and no of register of 8237

Name	Size	Number
Base Address Registers	16-bits	4
Base Word Count Registers	16-bits	4
Current Address Registers	16-bits	4
Current Word Count Registers	16-bits	4
Temporary Address Registers	16-bits	1
Temporary Word Count Registers	16-bits	1
Status Registers	8-bits	1
Command Registers	8-bits	1
Temporary Registers	8-bits	1
Mode Registers	6-bits	4
Mask Registers	4-bits	1
Request Registers	4-bits	1

1.Base address register

Each channel has 16 bit base address register

- It is a write only register
- It hold original value of address during all DMA transfer i.e. the content of this register not updated during DMA transfer
- When EOP' is activated the 8237 transfer content of base register into current address register in auto initialize mode.
- This register is written along with current address register during initialization format is same as current address register.

2.Base word count register

- 16 bit,write only,
- it hold original count value during all DMA cycle means content of this register are not updated during DMA transfer.
- When EOP' is activated the 8237 transfer content of this register into current word register in autoinitialization mode.
- This register is written along with current address register during initialization format is same as current word register.

3.Current address Register

- Each channel has 16 bit current address register,this register hold the address of memory location to be accessed during current DMA cycle.
- The address stored in this register is auto incremented or decremented after each transfer
- It is read and write register
- Divided into 2 parts lower byte & higher byte.
- In autoinitialization mode it initialized automatically with original address after EOP' signal

Current address register

4.Current word count register

- Each channel has 16 bit current word count register.
- The original value store in this register indicate the no of bytes to be transferred.
- The word count is decremented after each transfer the current count indicate the no of pending transfer.
- When the count value goes to zero a TC will be generated.
- it is a read and write register
- Divided into 2 parts lower byte & higher byte.
- In auto initialization mode it initialized automatically with original count value after EOP' signal the current word register format is

- w15 w14 . .. .. w0

5.Temporary address register

- This register is used to hold data during memory to memory transfer.
- It is 8 bit read only register
- The microprocessor can read least byte of memory to memory transfer.
- It is cleared by reset signal

Status register

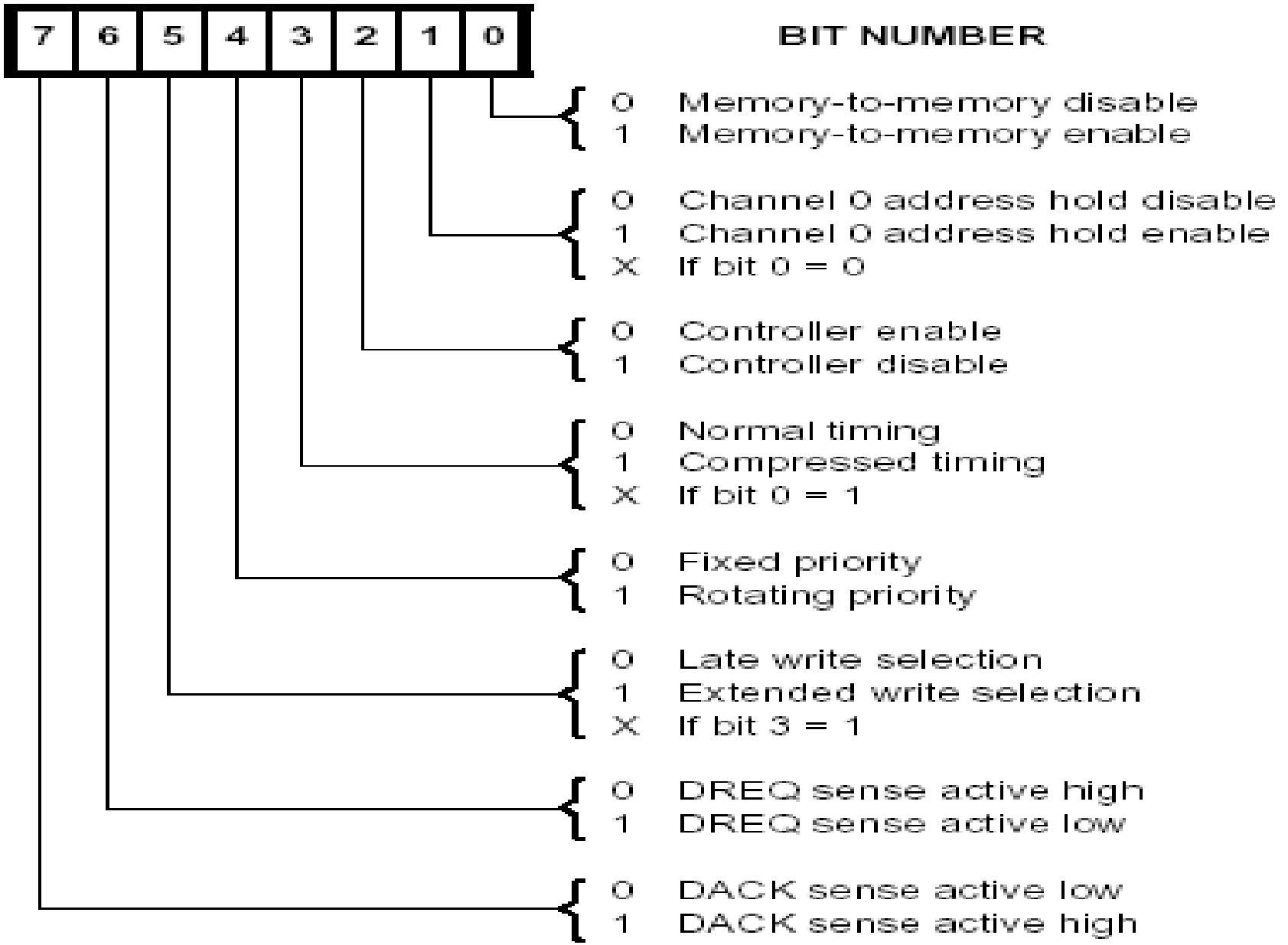
- 8bit read only
- It indicate which channels have reached a terminal count and which channel has pending DMA.
- Bits 0-3 are every time a TC is reached by that channel or external EOP signal is applied.
- These bits are clear automatically on reading the status register and upon reset signal.
- Bits 4-7 are set whenever their corresponding channel is requesting service.
- D7 d6 d1 d0
- Do if 0 channel reached TC if 1 not reach TC
- D1 if 1 channel reached TC if 1 not reach TC and so on

Command register

- It is 8 bit write only register
- This register is cleared by reset signal
- It is used to initialize operational modes of 8237

- The format is shown in next slide

Command Register



Mode register

- It is 8bit write only register
- It is used to set operative modes
- Each channel has 6bit mode register.
- All register are clear by reset signal.
- Format is shown in next slide

Mode Register

BIT NUMBER

00	Channel 0 select
01	Channel 1 select
10	Channel 2 select
11	Channel 3 select
XX	Readback
00	Verify transfer
01	Write transfer
10	Read transfer
11	Illegal
XX	If bits 6 and 7 = 11
0	Autoinitialization disable
1	Autoinitialization enable
0	Address increment select
1	Address decrement select
00	Demand mode select
01	Single mode select
10	Block mode select
11	Cascade mode select

Mask Register

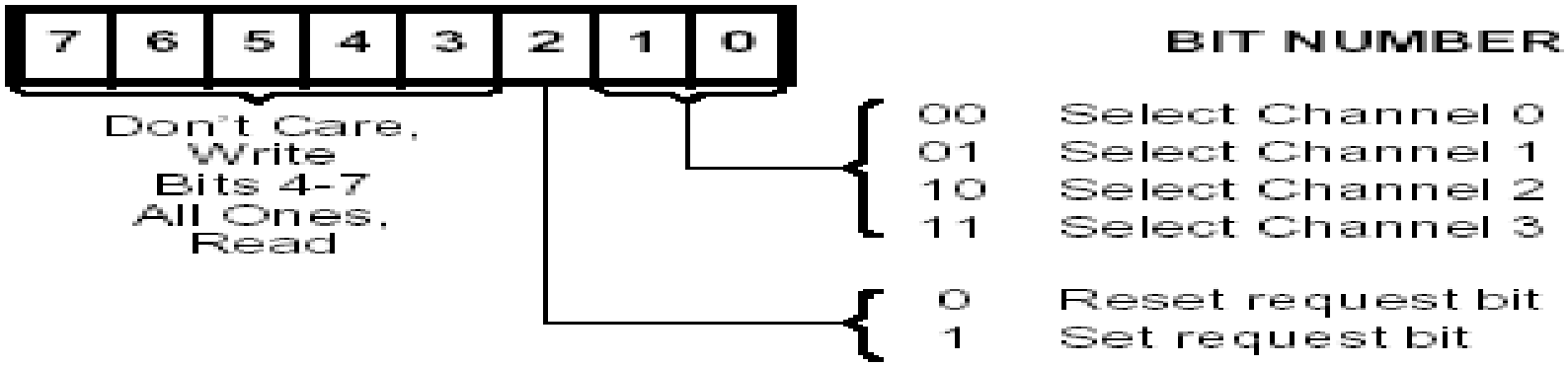
- It as a 8bit write only register

- In normal mode mask bit set automatically after TC.
- It is not affected in autoinitialize mode

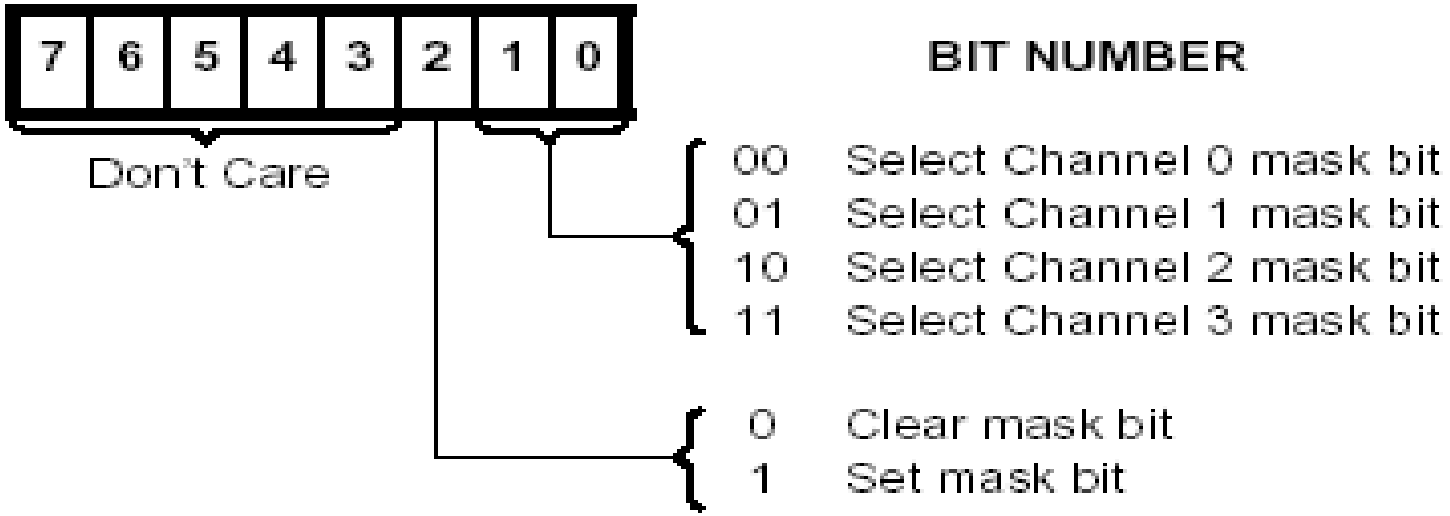
Request register

- 8bit write only
- It is used to request DMA through s/w. each channel has a request bit associated with in the request register.
- Each register is set or reset separately.
- Clear by reset
- Format shown in next slide

Request Register



Mask Register



Block transfer mode

- In this mode device can make no of transfer as programmed in word count register.
- After each transfer count word is decremented by one and the address is decremented or incremented by one.
- The DMA transfer is untill the word count “roll over” from zero to FFFFh, a terminal count(TC) and external End of Process (EOP) is encountered. Block transfer mode is used when the DMACneeds to transfer a block of data.

Scope of Research

- DMA controller is widely used chip it transfer the data by passing the microprocessor. We can enhance the capability of DMA controller.