

**ECE Department**  
**Virtual Lab Experiments**

LINK: [www.vlab.co.in](http://www.vlab.co.in)

**Sem :IV ECE**

**Lab:Digital Electronics**

**Lab under Virtual Portal: Digital Electronics, IIIT H**

S.No	Experiment	Link
1	Write VHDL programs for the following circuits, check the wave forms and the hardware generated a. Multiplexer      b. Demultiplexer	<a href="http://iiith.vlab.co.in/?sub=21&amp;brch=66&amp;sim=531&amp;cnt=862">http://iiith.vlab.co.in/?sub=21&amp;brch=66&amp;sim=531&amp;cnt=862</a>
2	Implement Full Adder using FPGA & CPLD.	<a href="http://iitb.vlab.co.in/?sub=43&amp;brch=227&amp;sim=1000&amp;cnt=1821">http://iitb.vlab.co.in/?sub=43&amp;brch=227&amp;sim=1000&amp;cnt=1821</a>
3	Implement BCD to 7 segments Decoder using FPGA& CPLD.	<a href="http://iitb.vlab.co.in/?sub=43&amp;brch=227&amp;sim=1000&amp;cnt=1821">http://iitb.vlab.co.in/?sub=43&amp;brch=227&amp;sim=1000&amp;cnt=1821</a>
4	Implement an Up Counter using FPGA & CPLD.	<a href="http://iitb.vlab.co.in/?sub=43&amp;brch=227&amp;sim=1000&amp;cnt=1821">http://iitb.vlab.co.in/?sub=43&amp;brch=227&amp;sim=1000&amp;cnt=1821</a>