Programmable Logic Devices

INTRODUCTION

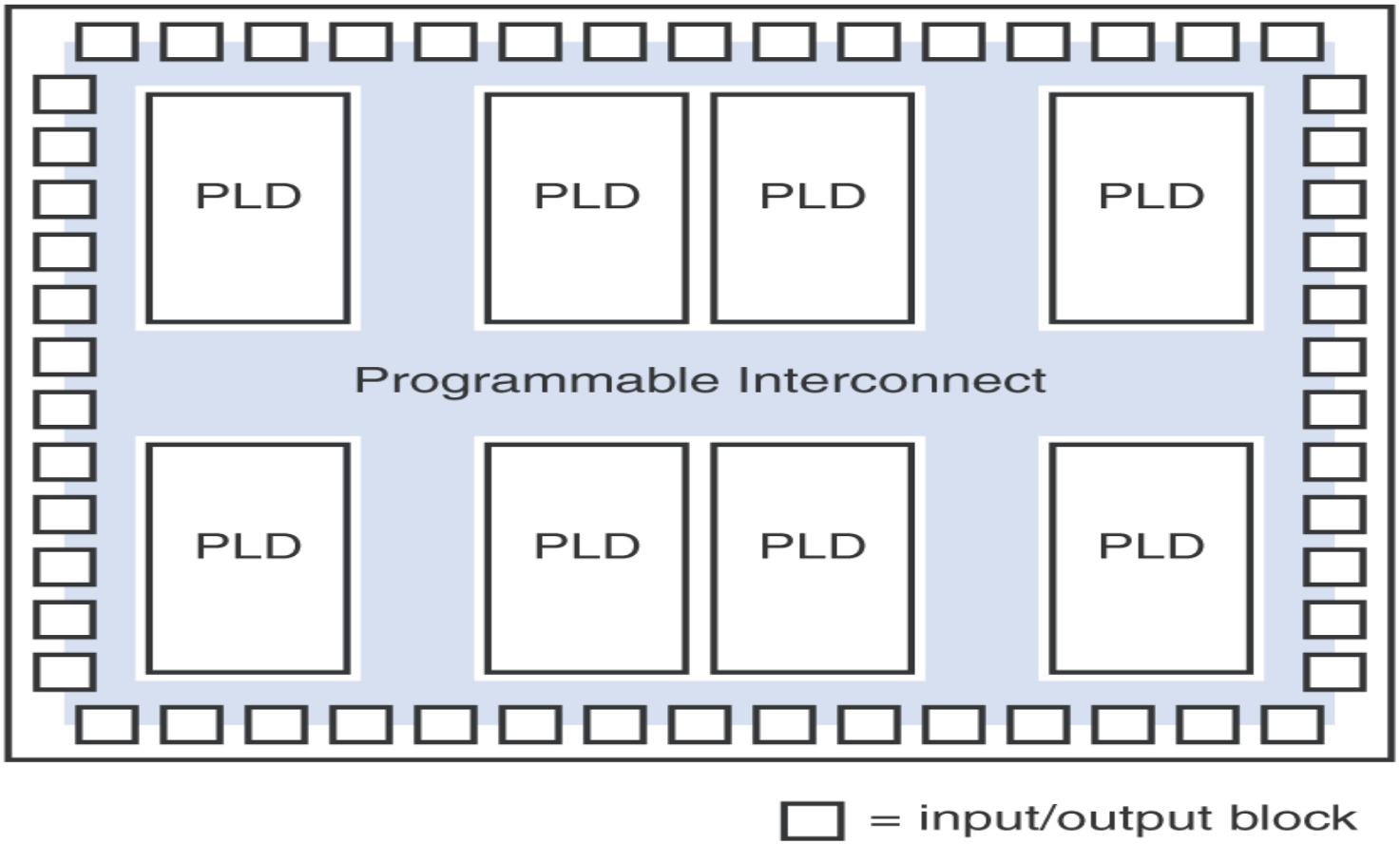
- A programmable logic device or PLD is an electronic component used to build reconfigurable digital circuits. Unlike a logic gate, which has a fixed function, a PLD has an undefined function at the time of manufacture. Before the PLD can be used in a circuit it must be programmed, that is, reconfigured.

CPLD

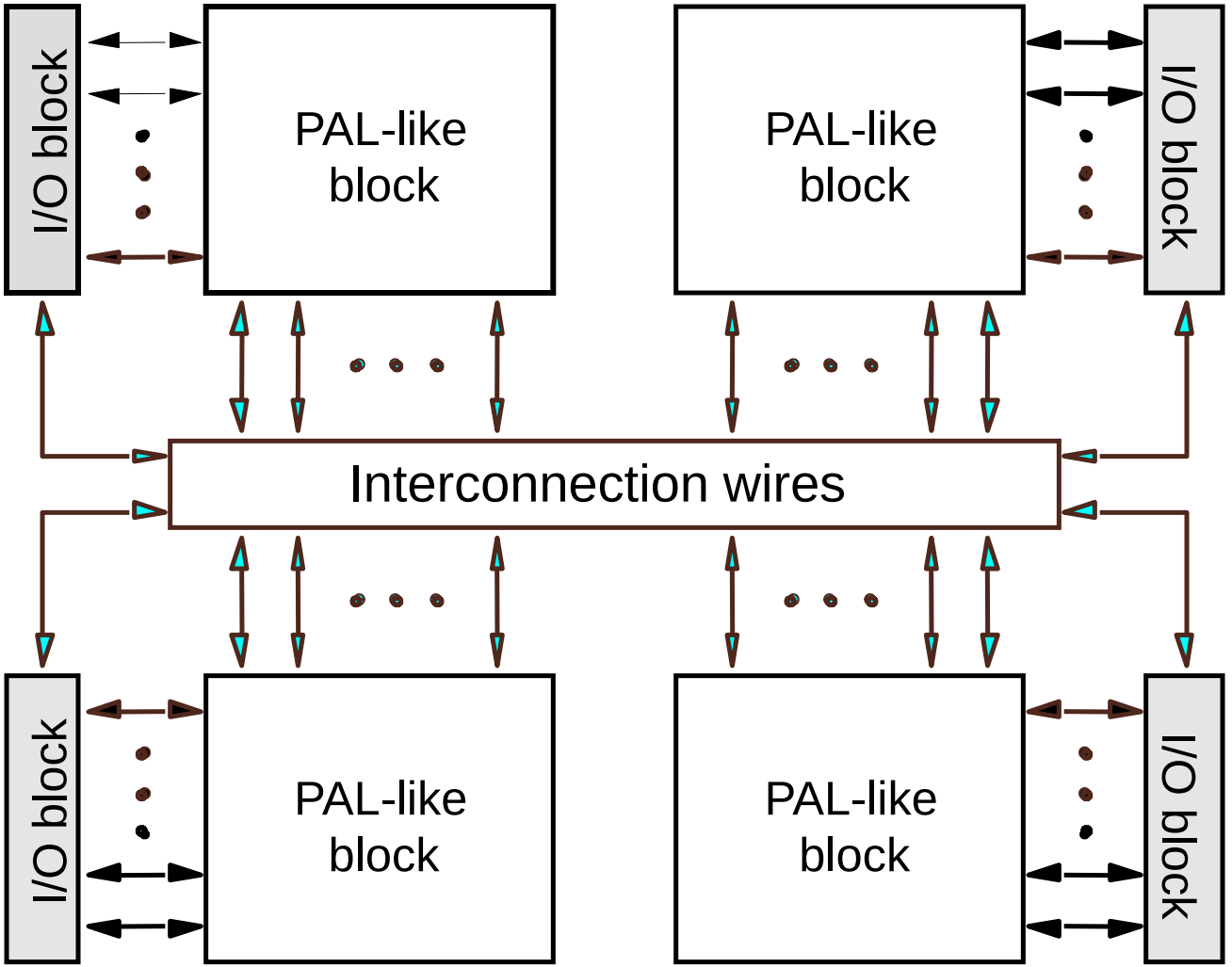
- Complex Programmable Logic Devices (CPLD)
- SPLDs (PLA, PAL) are limited in size due to the small number of input and output pins and the limited number of product terms
- CPLDs contain multiple circuit blocks on a single chip
  - Each block is like a PAL: PAL-like block
  - Connections are provided between PAL-like blocks via an interconnection network that is programmable
  - Each block is connected to an I/O block as well

CPLD

- A CPLD is just a collection of individual PLDs on a single chip, accompanied by a programmable interconnection structure.
- This structure allow the PLDs to be interconnected in the same way as can be done off-chip.



Structure of a CPLD: A Closer Look



CPLD Logic Block

- Inputs
- Product-term array
- Macro-cells (registers)

- Logic blocks executes sum-of-product expressions and stores the results in micro-cell registers
- CPLDs have many pins – large ones have > 200
  - Removal of CPLD from a PCB is difficult without breaking the pins
  - Use ISP (in system programming) to program the CPLD
  - JTAG (Joint Test Action Group) port used to connect the CPLD to a computer

Why CPLDs?

- For larger applications, we could simply increase the number of inputs and outputs in a conventional SPLD …
- Problems:
  - too costly
  - logic gets slower as number of inputs to AND array increases
- Solution:
  - multiple PLDs with a relatively small (fast) programmable interconnect
  - less general than a single large PLD, but we can use software to partition our design into smaller PLD blocks

- To create a CPLD device:
  - put a lot of Simple PLDs on the same chip
  - add “wires” between them whose connections can be programmed (interconnect)
  - use EEPROM technology for the connections

CPLD featured in common FPGA:-

i. Large number of gates available.
ii. Can include complicated feedback path.

CPLD application:-

i. Address coding
ii. High performance control logic
iii. Complex finite state machines

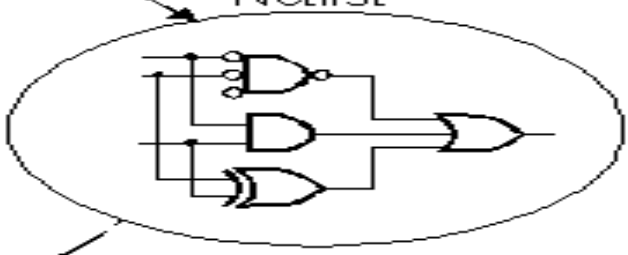
VHDL Source Code

```
entity leddcd is
   port(
      d: in std_logic_vector(3 downto 0);
      s: out std_logic_vector(6 downto 0);
   );
end;

architecture leddcd_arch of leddcd is
begin
   s <= "1110111" when d="0000" else
        "0010010" when d="0001" else
        "1101101";
end leddcd_arch;
```

Synthesize

Netlist



routing resources

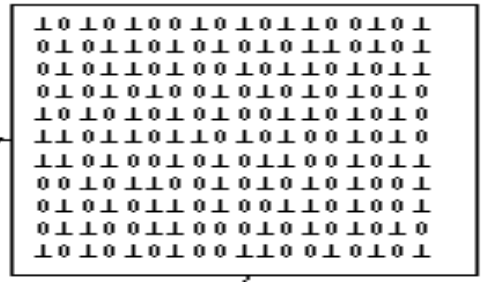
FPGA

look-up table

configurable logic block

Map, Place & Route

Bitstream



Generate Bitstream

Download and Test

XSA Board