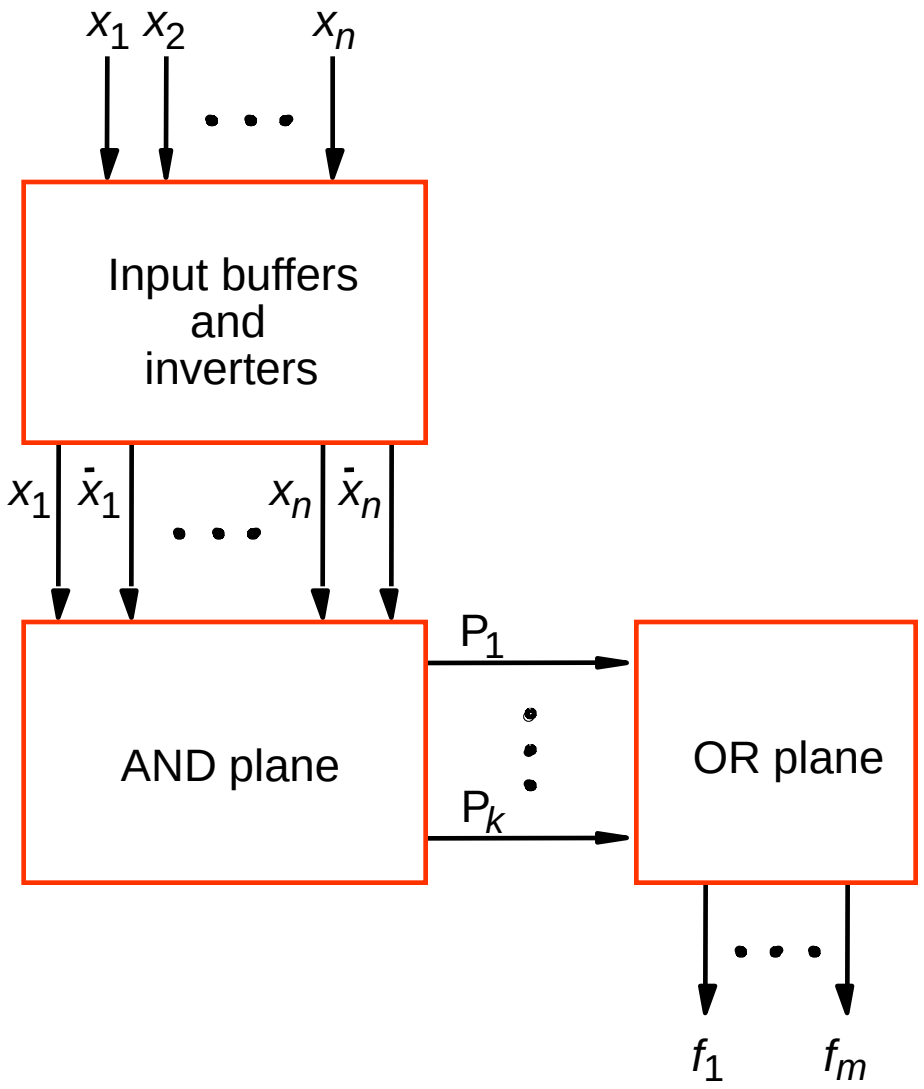
Programmable Array Logic (PAL)

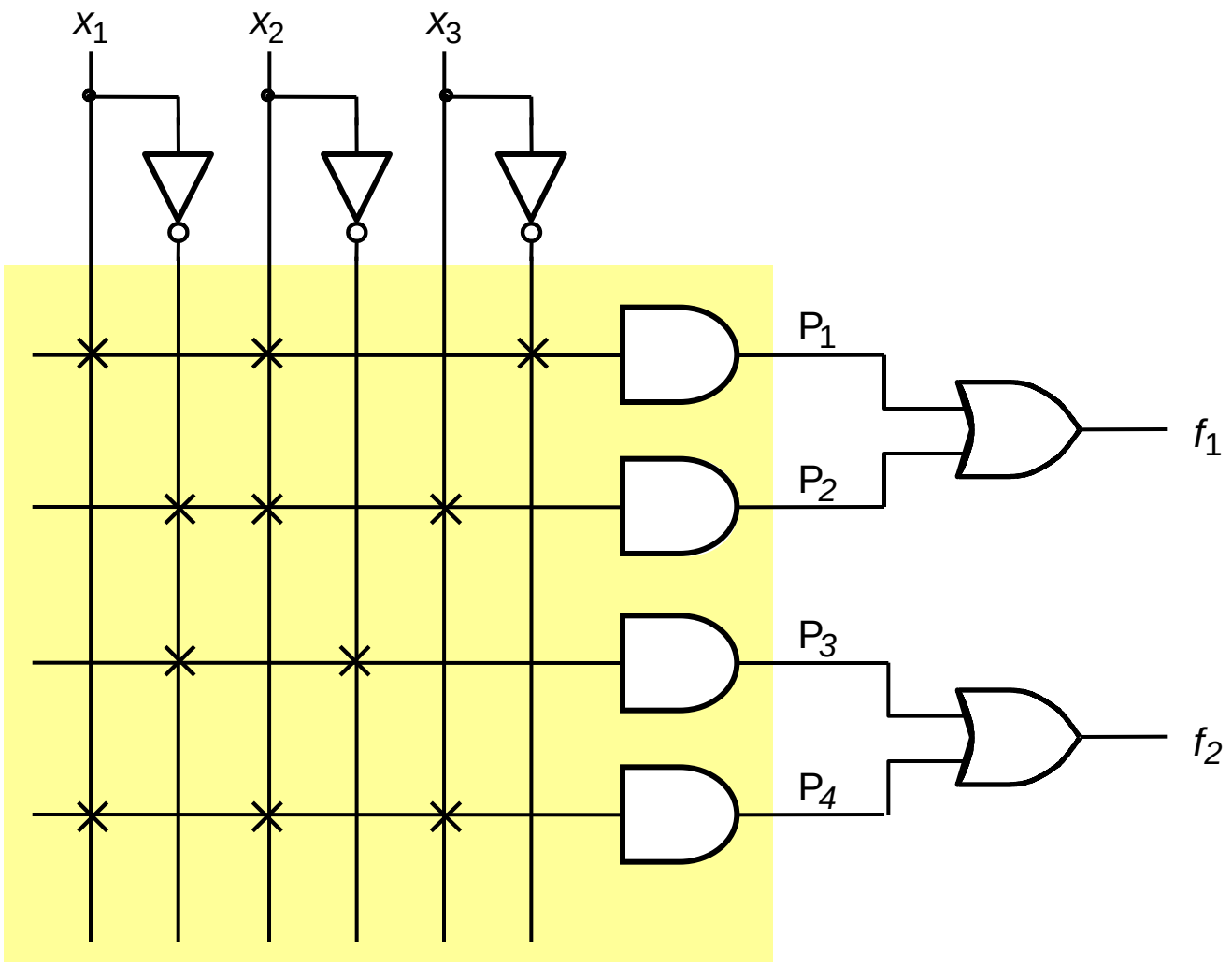
- Also used to implement circuits in SOP form
- The connections in the AND plane are programmable
- The connections in the OR plane are NOT programmable



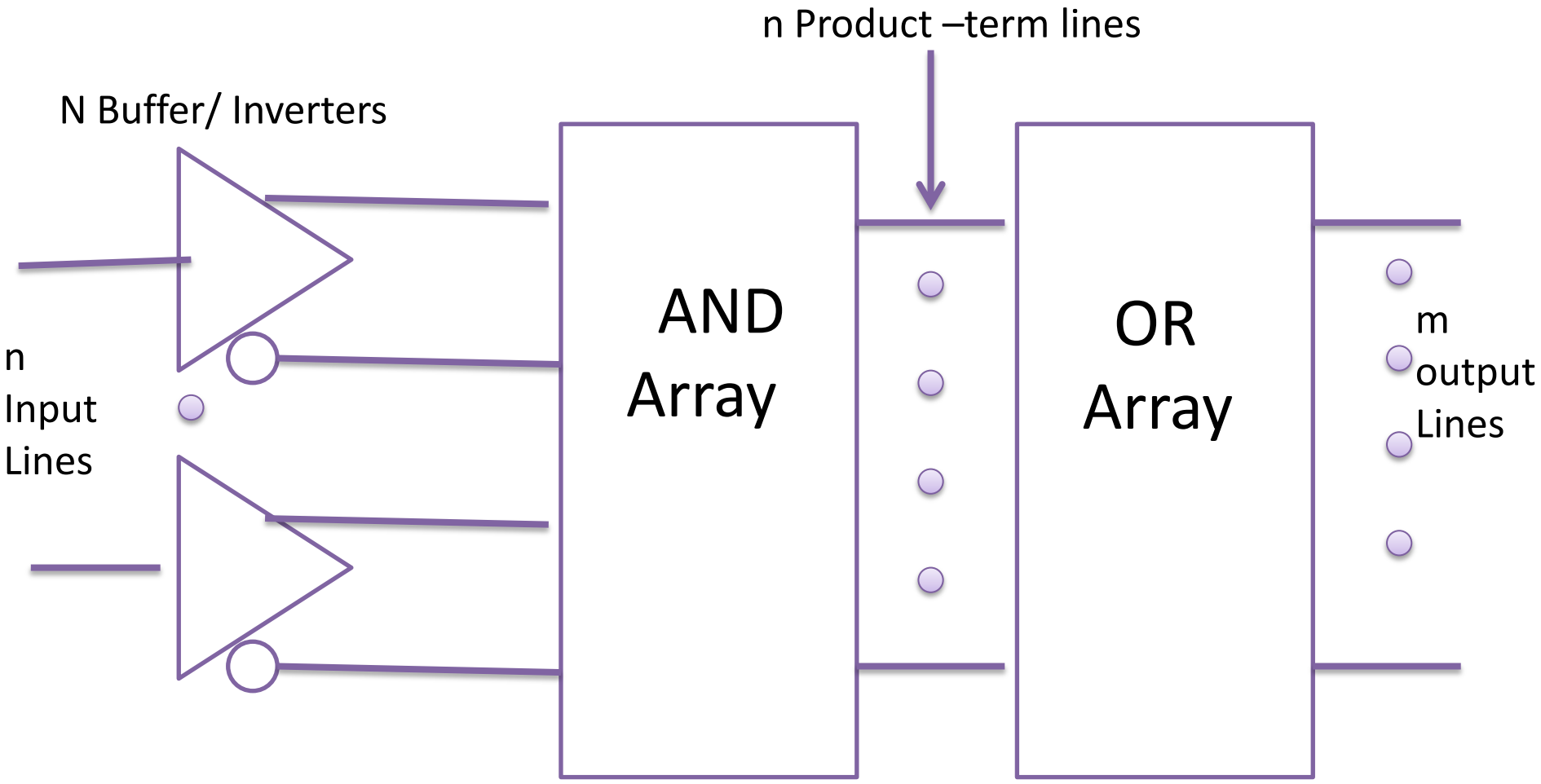
Example Schematic of a PAL

$f_1 = x_1x_2x_3' + x_1'x_2x_3$

$f_2 = x_1'x_2' + x_1x_2x_3$



PLDs


n Product –term lines
N Buffer/ Inverters
n
Input
Lines
AND
Array
OR
Array
m
output
Lines

Types of PLD

- PROM (Programmable read only memory)
- PLA (programmable logic array)
- PAL (Programmable array logic)
- GAL (Generic array logic)
- PEEL (Programmable Electrically Erasable Logic)
- CPLDs (Complex programmable logic device)
- FPGA (Field programmable gate array)

Programmable Array

Device	AND Array	OR Array
ROM	Fixed	Programmable
PLA	Programmable	Programmable
PAL	Programmable	Fixed
GAL	Programmable	Fixed

ROM as PLD

- Consider a ROM with m outputs (the address lines) and *n* inputs (the data lines).
- When used as a memory, the ROM contains words of *n* bits each

TYPES

- PROMs (programmable ROMs),
- EPROMs (ultraviolet-erasable PROMs)
- EEPROMs (electrically erasable PROMs)