PLD (Programmable Logic Device)

- Can be programmed by the users as per their requirement
- Large circuit is designed on a single chip
- Possible to implement a combinational or sequential circuit using the PLD
- Consist of array of NOT, AND and OR gates
- Any Boolean function can be represented by sum of the product form.

Programmable ROM (PROM)

- Address: m bits; data: n bits
- ROM contains 2^N word of M bit each
- The input bits decide the particular word that becomes available on output lines

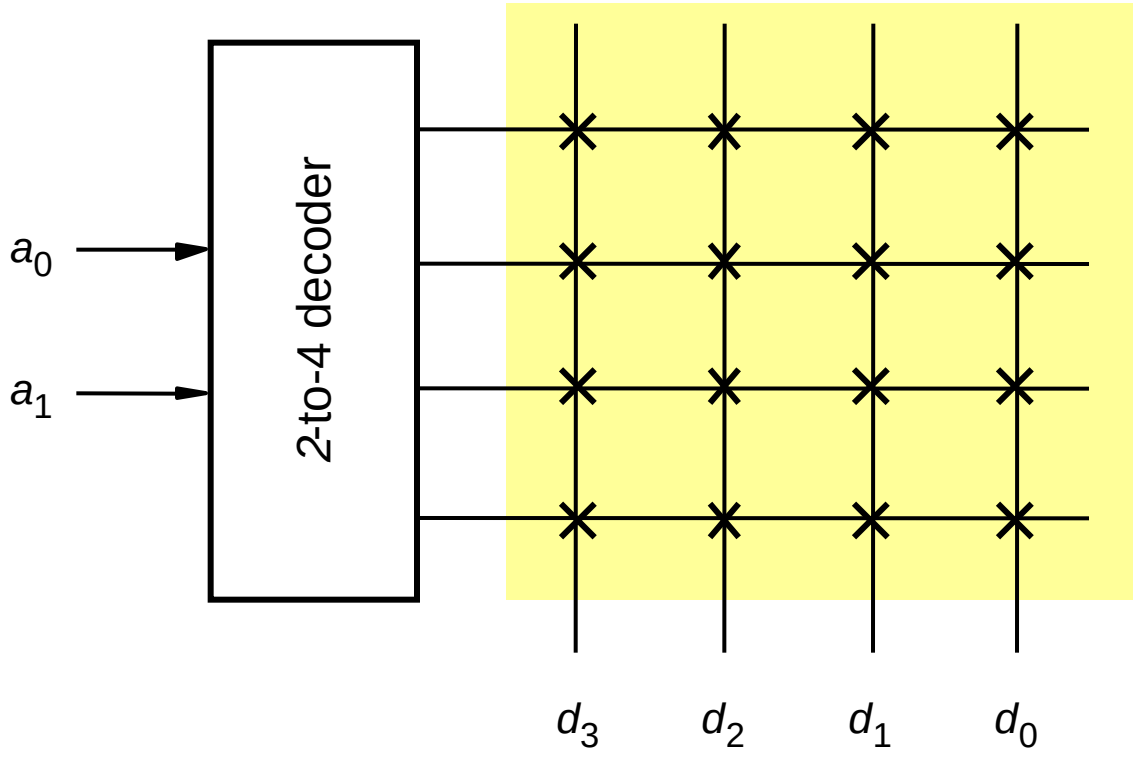
- A ROM (Read Only Memory) has a fixed AND plane and a programmable OR plane

- Size of AND plane is 2^n where n = number of input pins
  - Has an AND gate for every possible minterm so that all input combinations access a different AND gate

- OR plane dictates function mapped by the ROM

4x4 ROM

- 2^2x4 bit ROM has 4 addresses that are decoded

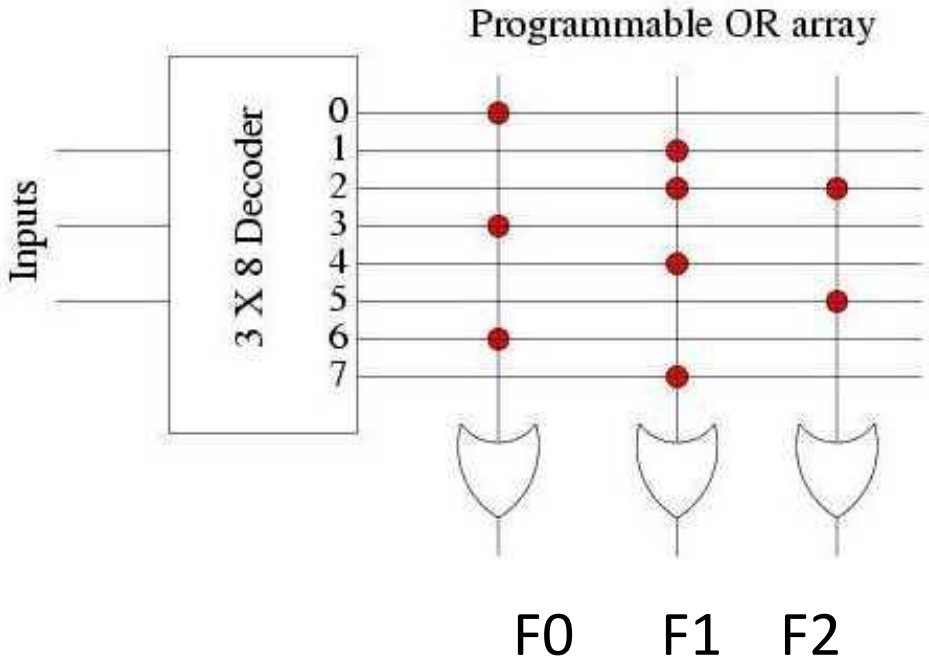


ROM Types

- Programmable PROM
  - Break links through current pulses
  - Write once, Read multiple times
- Erasable PROM (EPROM)
  - Program with ultraviolet light
  - Write multiple times, Read multiple times
- Electrically Erasable PROM (EEPROM)/ Flash Memory
  - Program with electrical signal
  - Write multiple times, Read multiple times

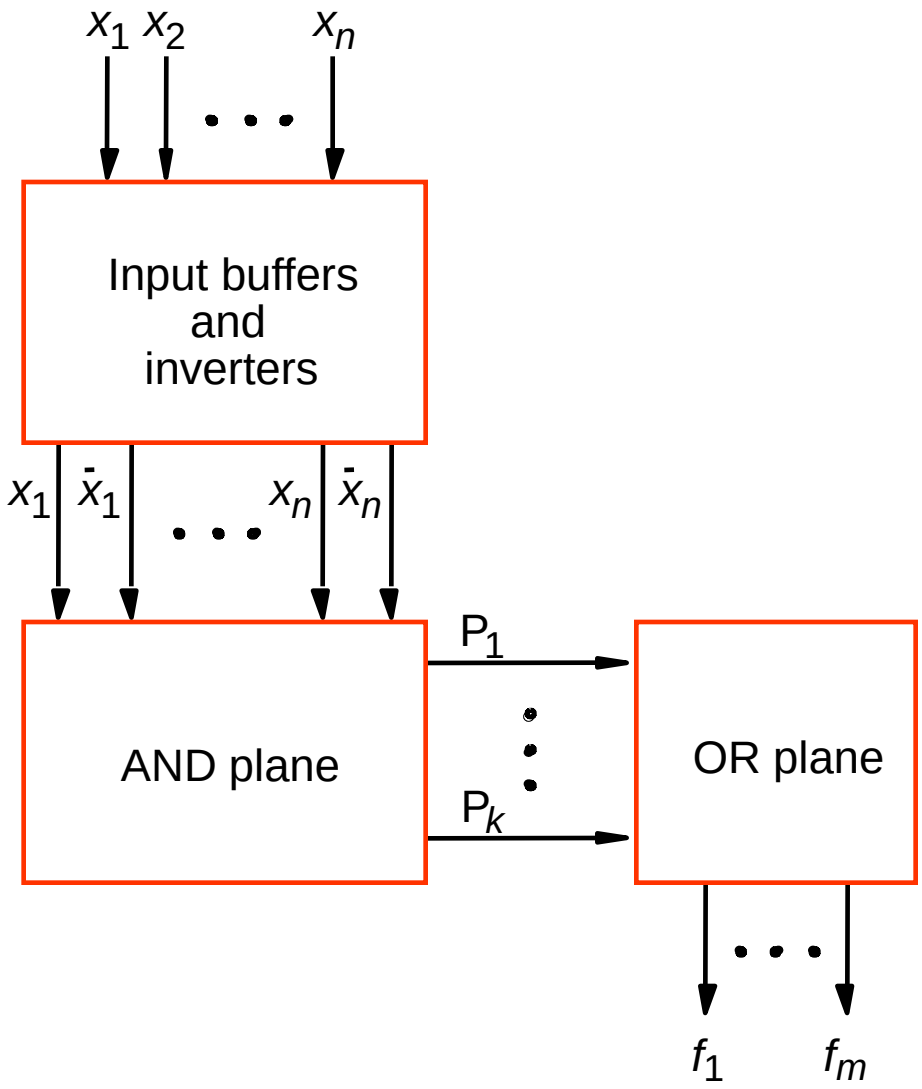
Combinational Circuit Implementation using PROM

I0	I1	I2	F0	F1	F2
0	0	0	1	0	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	1	0	0
1	1	1	0	1	0



Programmable Logic Array (PLA)

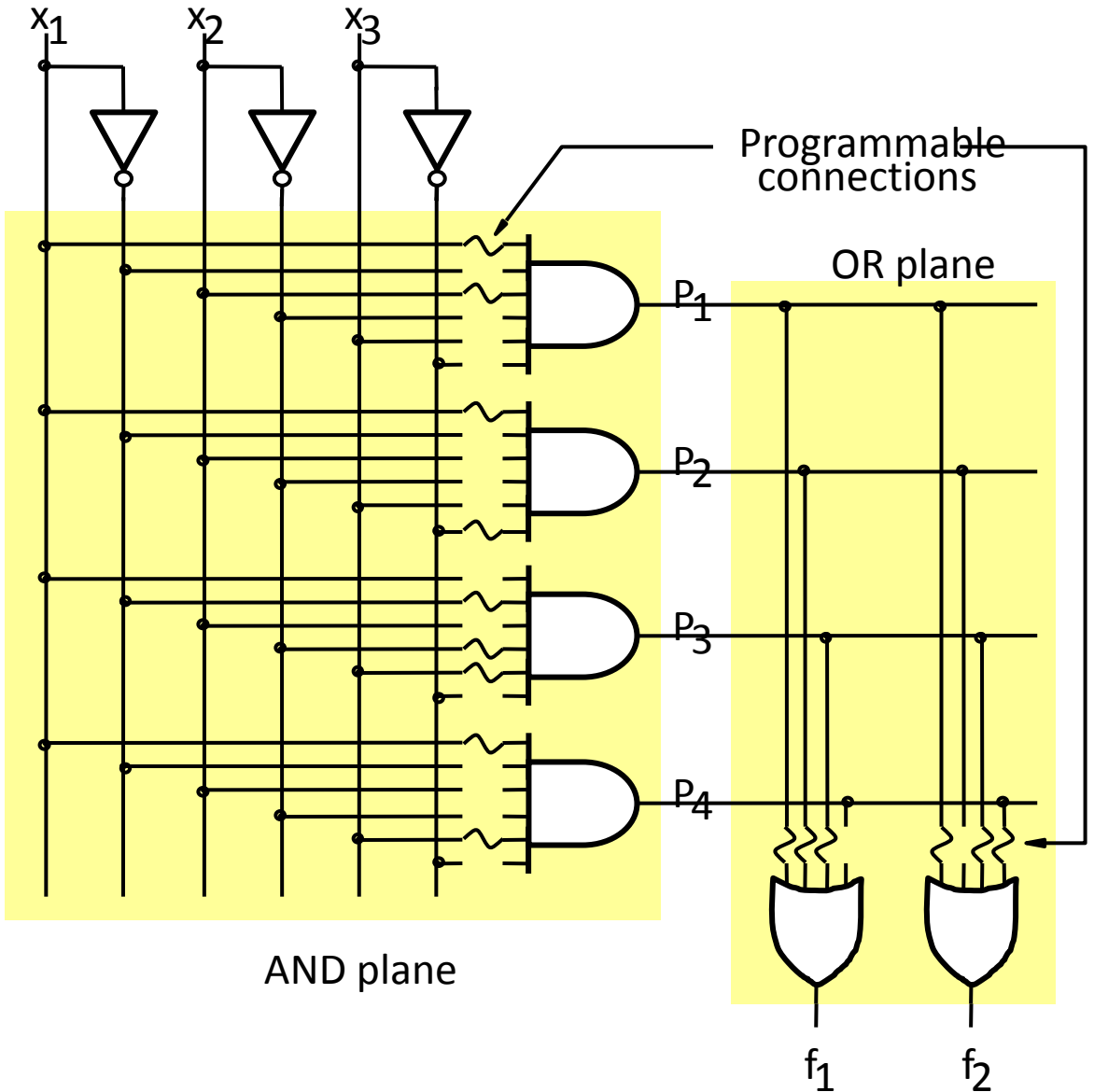
- Use to implement circuits in SOP form
- The connections in the AND plane are programmable
- The connections in the OR plane are programmable



Gate Level Version of PLA

f1 = x1x2+x1x3'+x1'x2'x3

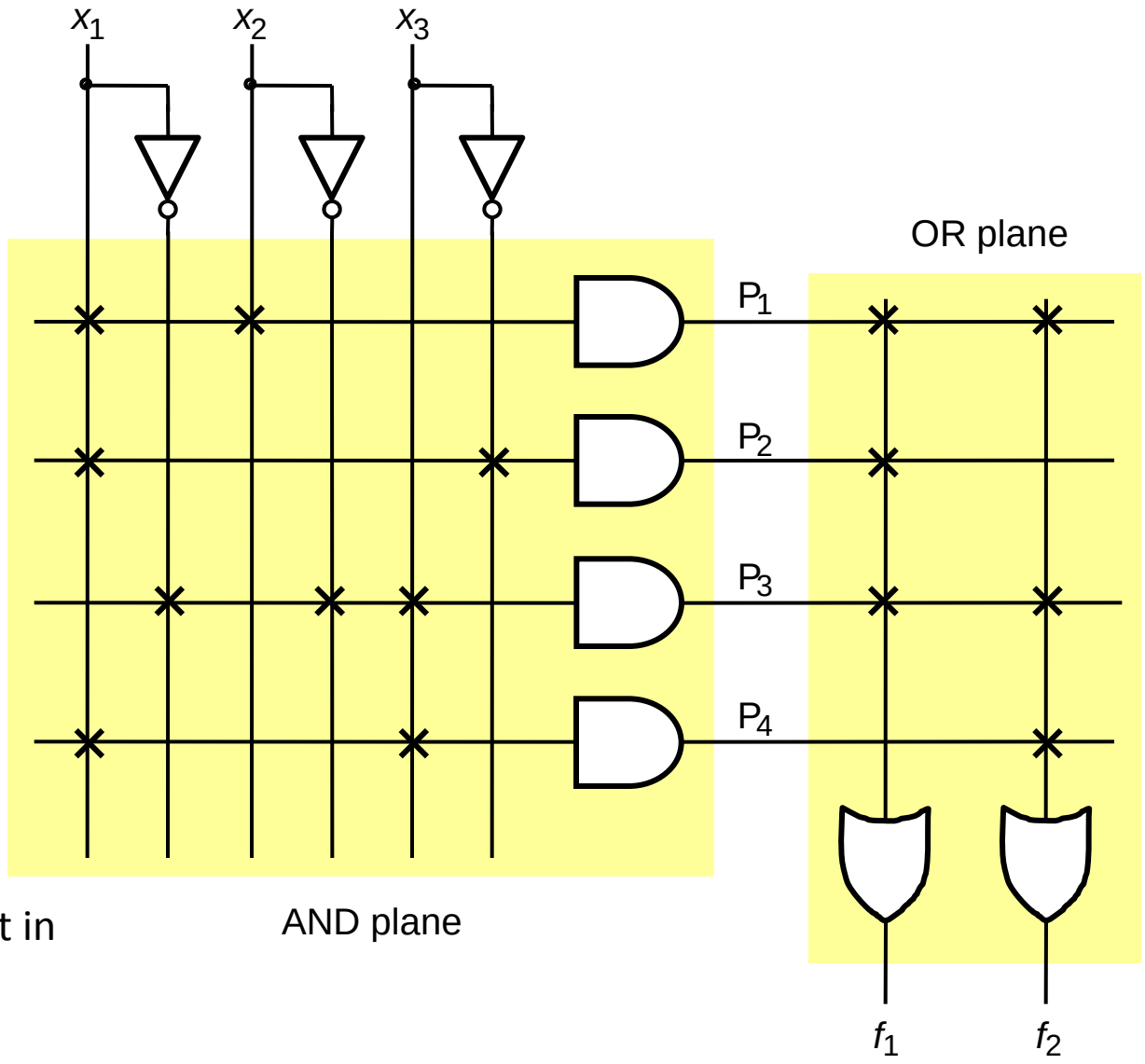
f2 = x1x2+x1'x2'x3+x1x3



Customary Schematic of a PLA

$f_1 = x_1x_2+x_1x_3'+x_1'x_2'x_3$

$f_2 = x_1x_2+x_1'x_2'x_3+x_1x_3$



x marks the connections left in place after programming