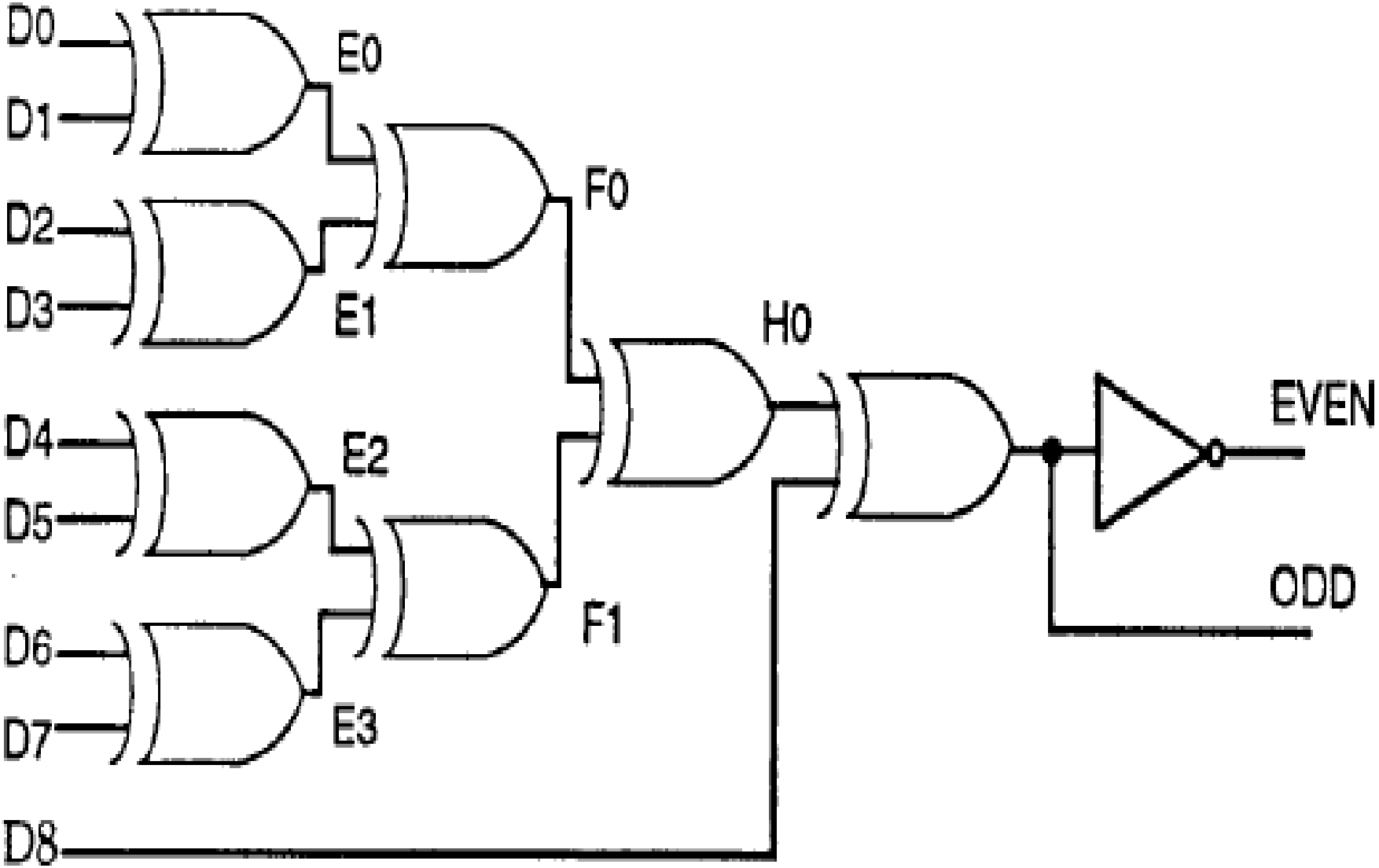
9 bit parity generator



```
entity PARITY_9_BIT is
        port (D: in BIT_VECTOR(8 downto 0); EVEN: out BIT;
                ODD: buffer BIT);
end PARITY_9_BIT;

architecture PARITY_STR of PARITY_9_BIT is
        component XOR2
                port (A, B: in BIT; Z: out BIT);
        end component;
        component INV2
                port (A: in BIT; Z: out BIT);
        end component;
        signal E0, E1, E2, E3, F0, F1, H0: BIT;
begin
        XE0: XOR2 port map (D(0), D(1), E0);
        XE1: XOR2 port map (D(2), D(3), E1);
        XE2: XOR2 port map (D(4), D(5), E2);
        XE3: XOR2 port map (D(6), D(7), E3);
        XF0: XOR2 port map (E0, E1, F0);
        XF1: XOR2 port map (E2, E3, F1);
        XH0: XOR2 port map (F0, F1, H0);
        XODD: XOR2 port map (H0, D(8), ODD);
        XEVEN: INV2 port map (ODD, EVEN);
end PARITY_STR;
```