## **DATA FLOW Style**

```
entity DECODER2x4 is
port (A, B, ENABLE: in SIT: Z: out BIT_VECTOR(0 to 3));
end DECODER2x4;
architscture dec dataflgw of DECODER2x4 is
signal ABAR, BBAR: BIT;
begin
   Z(3) \le not (A and B and ENABLE);
   Z(0) \le not (ABAR and BBAR and ENABLE);
   BBAR <= not B;
   Z(2) <= not (A and BBAR and ENABLE);
   ABAR <= not A;
   Z(1) <= not (ABAR and B and ENABLE);
end DEC DATAFLOW;
```

## **Behavioral Style**

```
entity DECODER2x4 is
port (A, B, ENABLE: in SIT: Z: out BIT VECTOR(0 to 3));
end DECODER2x4;
architecture DEC_SEQUENTIAL of DECODER2x4 is
begin
 process (A, B, ENABLE)
  variable ABAR, BBAR: BIT;
  begin
         ABAR := not A;
         BBAR := not B;
         if (ENABLE = '1') then
           Z(3) \le not (A and B):
           Z(0) \le not (ABAR and BBAR);
           Z(2) \le not (A and BBAR);
           Z(1) \le not (ABAR and B);
           else
           Z<= "1111";
      end if;
  end process;
End DEC SEQUENTIAL;
```