

Entity Declaration

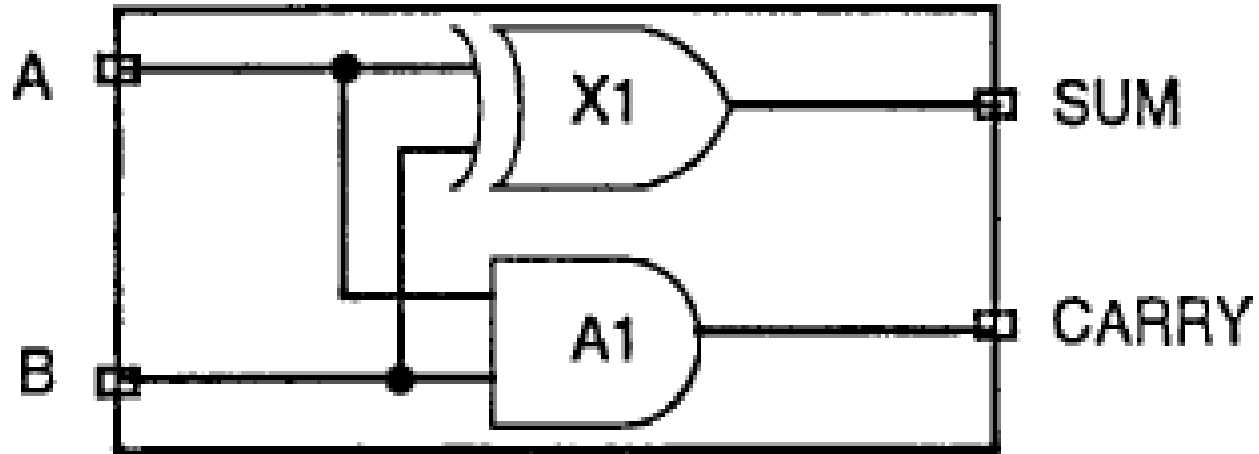


Figure 2.3 A half-adder circuit.

```
entity HALF_ADDER is  
port (A, B: in BIT; SUM, CARRY: out BIT);  
end HALF_ADDER;
```

Architecture Body

- The internal details of an entity are specified by an architecture body using any of the following modeling styles:
 - 1. As a set of interconnected components (to represent structure),**
 - 2. As a set of concurrent assignment statements (to represent dataflow),**
 - 3. As a set of sequential assignment statements (to represent behavior),**
 - 4. Any combination of the above three.**

Structural Style of Modeling

- **Example: Half Adder**

**architecture HA_STRUCTURE of HALF_ADDER is
component XOR2**

port (X, Y: in BIT; Z: out BIT);

end component;

component AND2

port (L, M: in BIT; N: out BIT);

end component;

begin

X1: XOR2 port map (A, B, SUM);

A1: AND2 port map (A, B, CARRY);

end HA_STRUCTURE;

Dataflow Style of Modeling

- **Example: Half Adder**

architecture HA_CONCURRENT of HALF_ADDER is

begin

SUM <= A xor B after 8 ns;

CARRY <= A and B after 4 ns;

end HA_CONCURRENT;

Behavioral Style of Modeling

- architecture HA_beh of HALF_ADDER is
begin
process (A, B)
begin
SUM <= A xor B ;
CARRY <= A and B ;
end process;
End HA_beh;

Mixed Style of Modeling

- It is possible to mix the three modeling styles that we have seen so far in a single architecture body

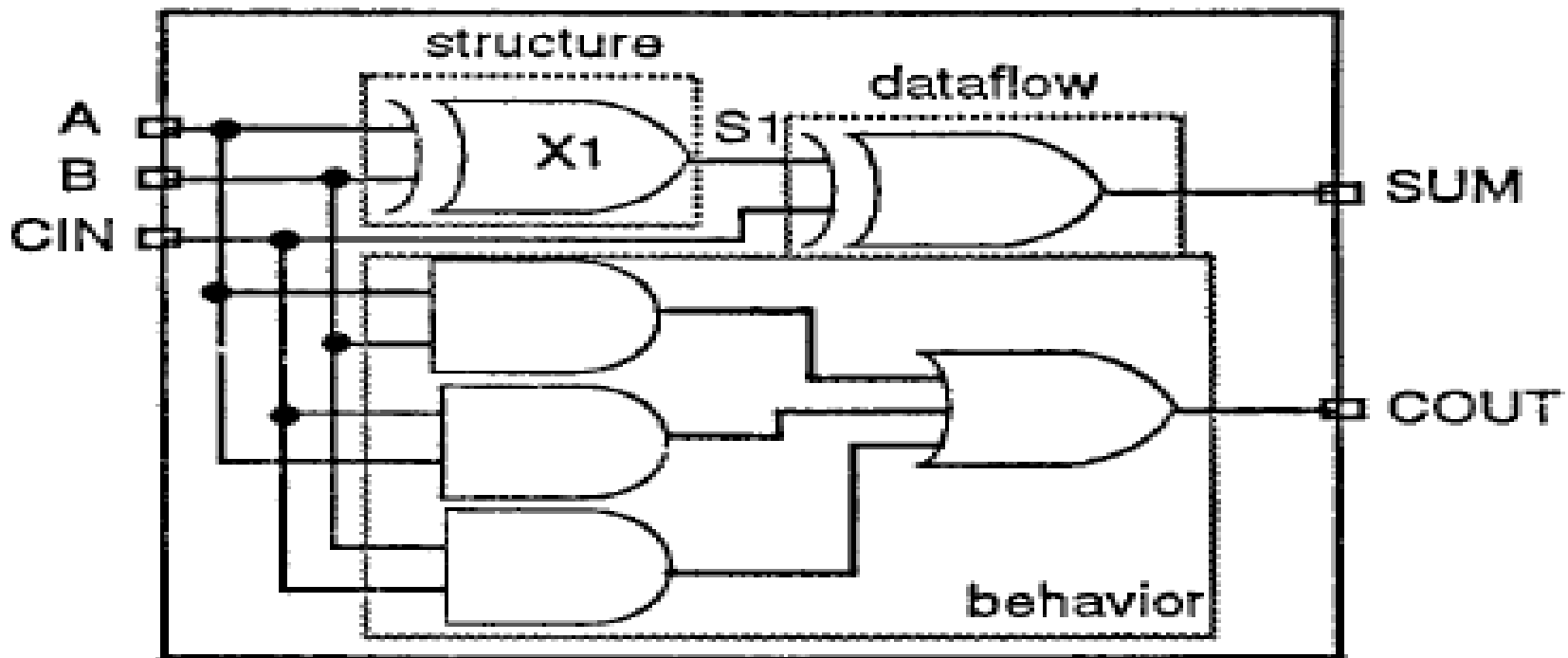


Figure 2.7 A 1-bit full-adder.

Mixed Style of Modeling cont..

```
entity FULL_ADDER is  
port (A, B, CIN: in BIT; SUM, COUT: out BIT);  
end FULL_ADDER;
```

```
architecture FA_MIXED of FULL_ADDER is  
component XOR2  
    port (X,Y: in BIT; Z: out BIT);  
end component;  
signal S1: BIT;
```

Mixed Style of Modeling cont..

begin

```
X1: XOR2 port map (A, B, S1 );  
process (A, B, CIN)  
    variable T1, T2, T3: BIT;
```

- structure.
- behavior.

begin

```
    T1 :=A and B;  
    T2 := B and CIN;  
    T3:=A and CIN;  
    COUT <= T1 or T2 or T3;  
end process;  
SUM <= S1 xor CIN;  
end FA_M!XED;
```

- *dataflow.*