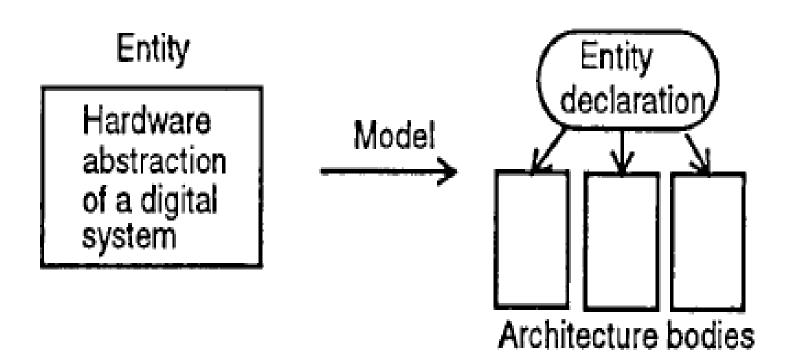
Basic Terminology

- To describe an entity, VHDL provides five different types of primary constructs, called design units.
- 1. Entity declaration
- 2. Architecture body
- 3. Configuration declaration
- 4. Package declaration
- 5. Package body

Entity & its model



1. Entity

 An entity is modeled using an entity declaration and at least one architecture body. The entity declaration describes the external view of the entity, for example, the input and output signal names.

2. Architecture body

 The architecture body contains the internal description of the entity, for example, as a set of interconnected components that represents the structure of the entity, or as a set of concurrent or sequential statements that represents the behaviour of the entity.

3. Configuration Declaration

 A configuration declaration is used to create a configuration for an entity. It specifies the binding of one architecture body from the many architecture bodies that may be associated with the entity. It may also specify the bindings of components used in the selected architecture body to other entities. An entity may have any number of different configurations.

Configuration Declaration cont..

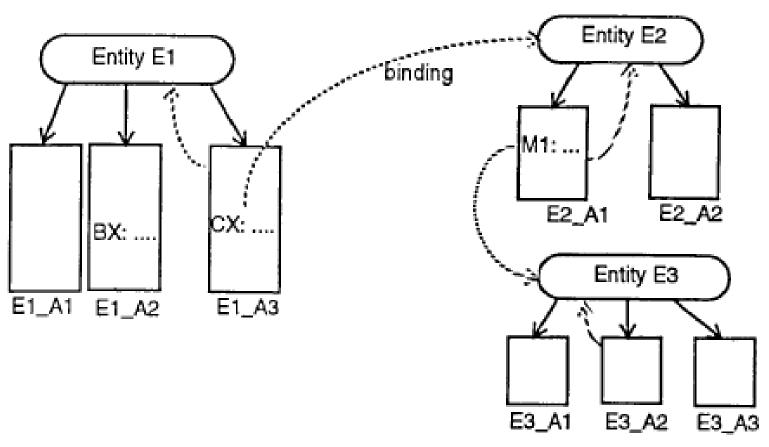


Figure 2.2 A configuration for entity El.

5. Package Body

 A package body contains the definitions of subprograms declared in a package declaration.