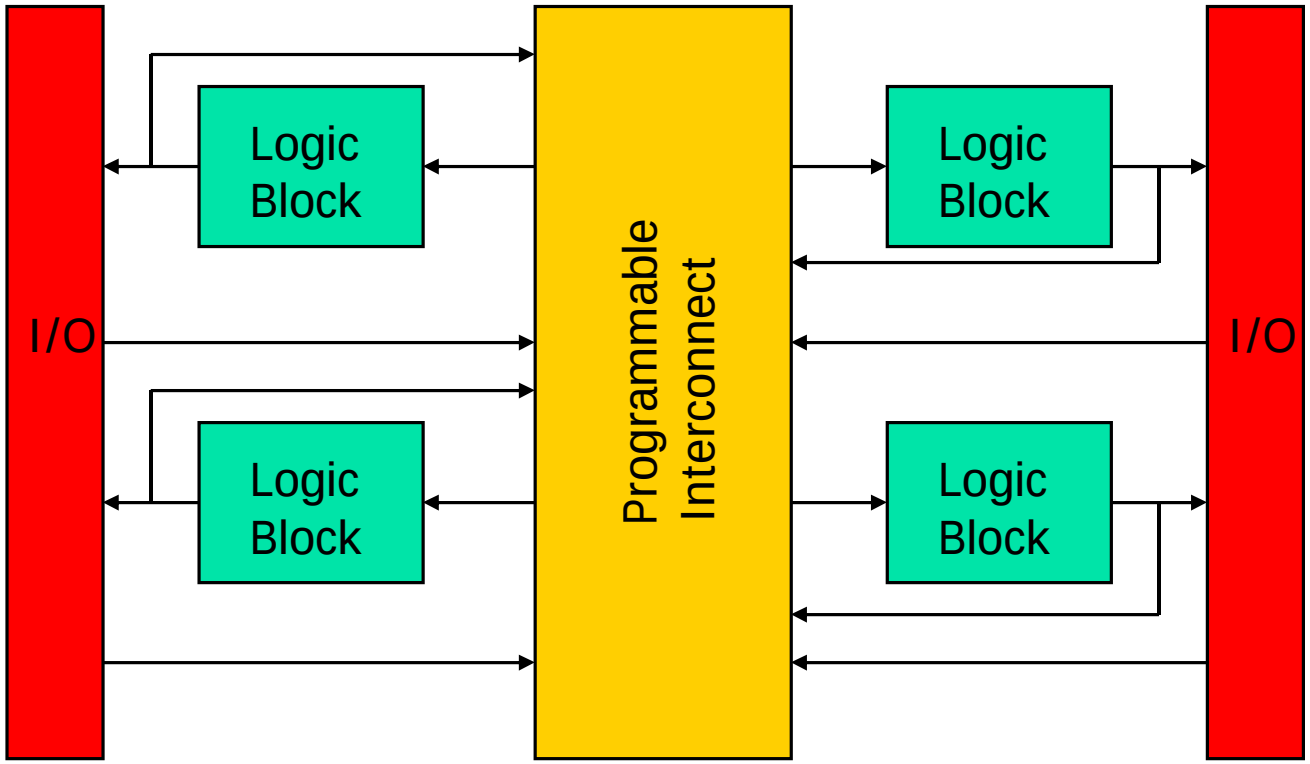
CPLDs and FPGA

CPLD


I/O
Logic Block
Logic Block
Programmable Interconnect
Logic Block
Logic Block
I/O

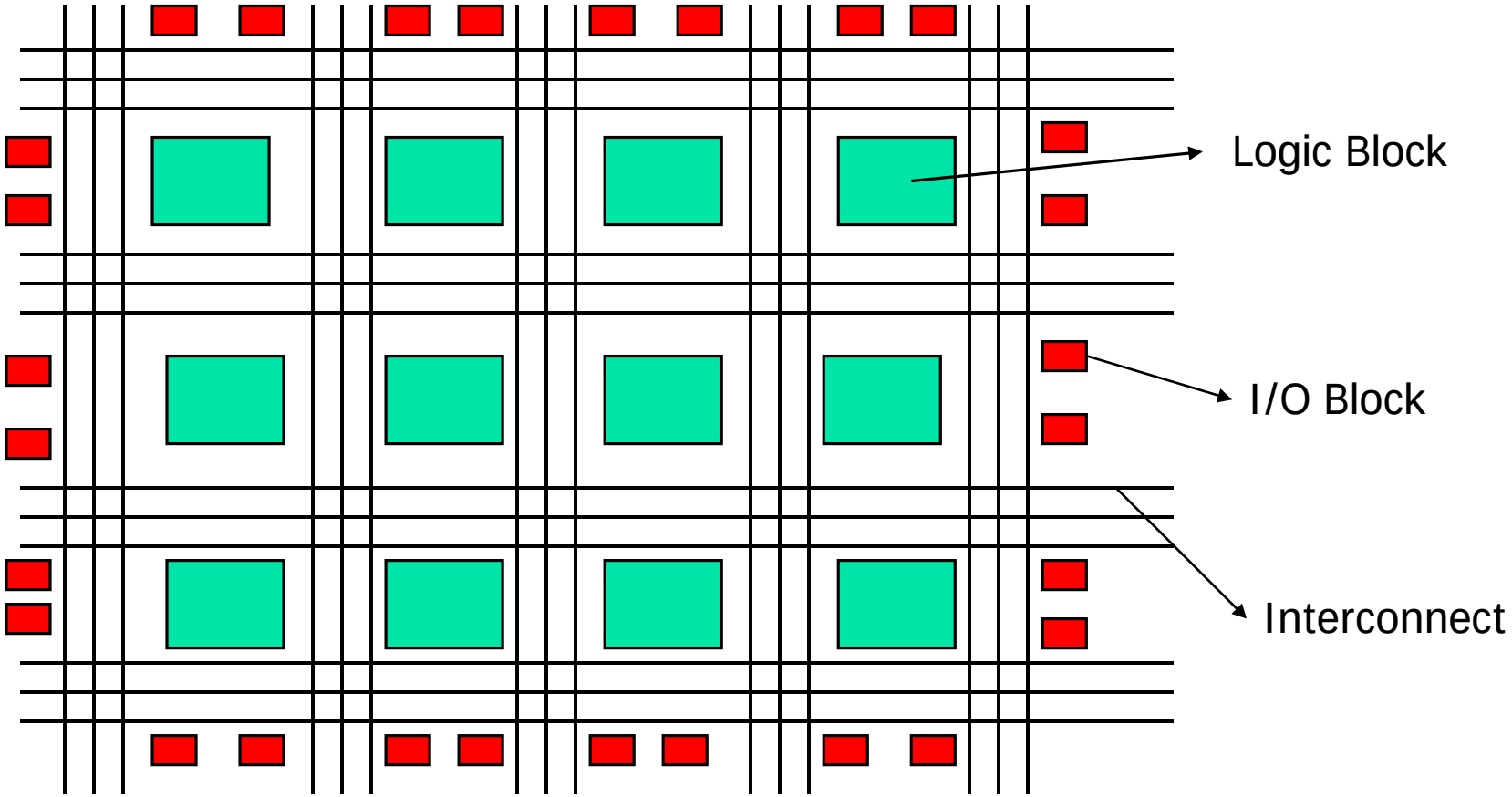
CPLD Logic Block

- Simple PLD
  - Inputs
  - Product-term array
  - Product term allocation function
  - Macro-cells (registers)
- Logic blocks executes sum-of-product expressions and stores the results in micro-cell registers
- Programmable interconnects route signals to and from logic blocks

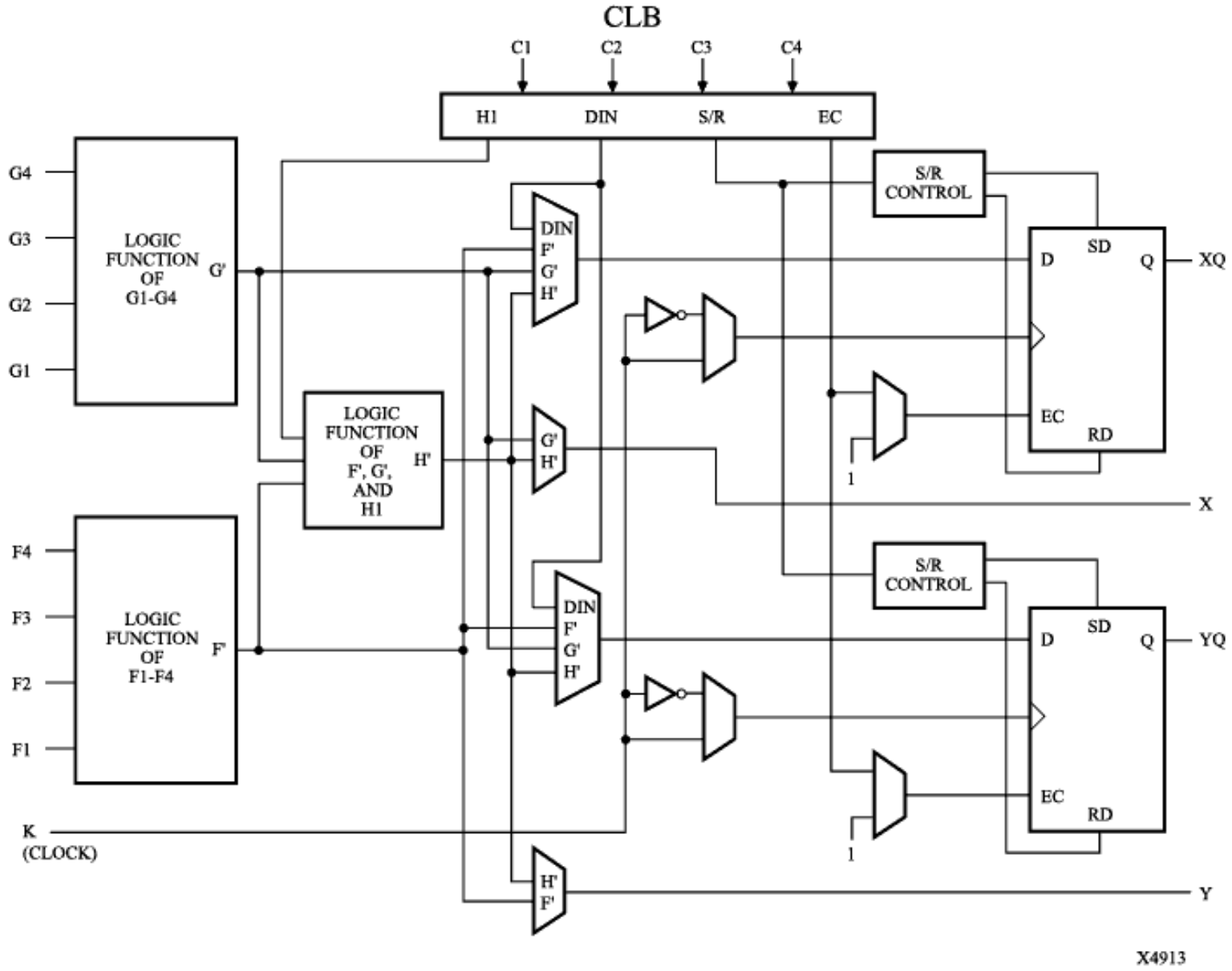
Major CPLD Resources

- Number of macro-cells per logic block
- Number of inputs from programmable interconnect to logic block
- Number of product terms in logic block

Structure of FPGA (Xilinx)



Configurable Logic Block CLB



Logic Function

- Implemented as look-up table (LUT)
- K-input LUT corresponds to 2^K x 1 bit memory
- K-input LUT can implement any k-input 1-output logic function

Configuring FPGA

- Configure CLB and IOB
- Configure interconnect
- Interconnect technology
  - SRAM
  - Anti-fuse (program once)
  - EPROM / EEPROM

Programming Technology

Name	Re-programmable	Volatile
EPROM	yes (out of circuit)	no
EEPROM	yes (in circuit)	no
SRAM	yes (in circuit)	yes
Antifuse	no	no

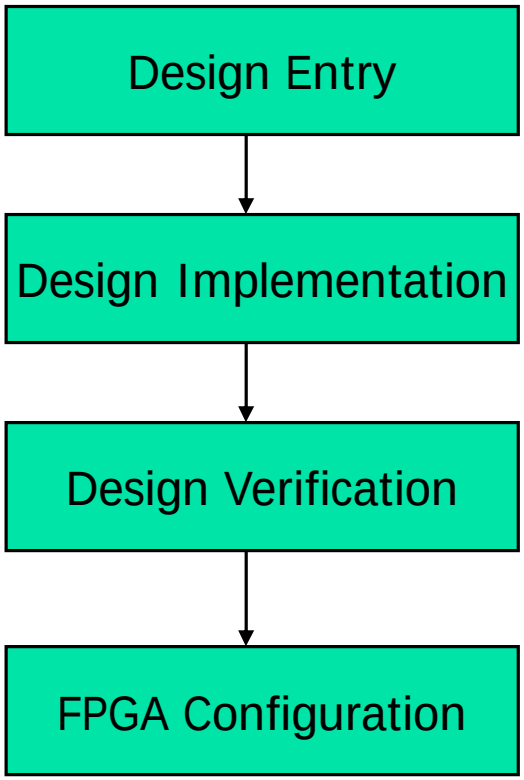
FPGA Applications

- Glue Logic (replace SSI and MSI parts)
- Rapid turnaround
- Prototype design
- Emulation
- Custom computing
- Dynamic reconfiguration

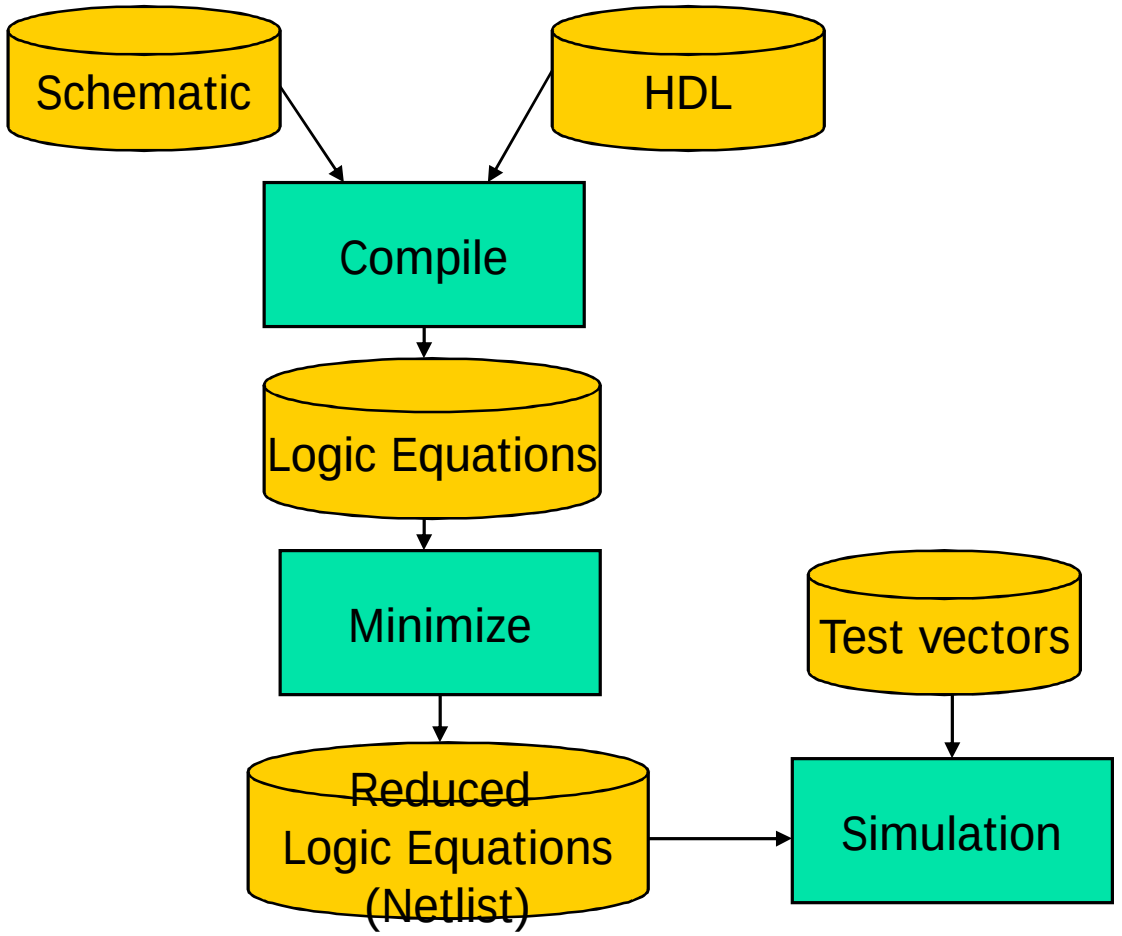
PLD Logic Capacity

- SPLD: about 200 gates
- CPLD
  - Altera FLEX (250K logic gates)
  - Xilinx XC9500
- FPGA
  - Xilinx Vertex-E (3 million logic gates)
  - Xilinx Spartan (10K logic gates)
  - Altera

FPGA Design Flow



Design Entry
(DK1 in our case)



Design Implementation

- Input: Netlist Output: bitstream
- Map the design onto FPGA resources
  - Break up the circuit so that each block has maximum n inputs
  - NP-hard problem
  - However, optimal solution is not required

Design Implementation (Cont.)

- Place: assigns logic blocks created during mapping process to specific location on FPGA
  - Goal: minimize length of wires
  - Again NP-hard
- Route: routes interconnect paths between logic blocks
  - NP-hard

Design Implementation Techniques

- Simulated annealing
- Genetic algorithm
- Mincut method
- Heuristic method

Design Verification & FPGA Configuration

- Functional Simulation
- Timing Simulation
- Download bitstream into FPGA