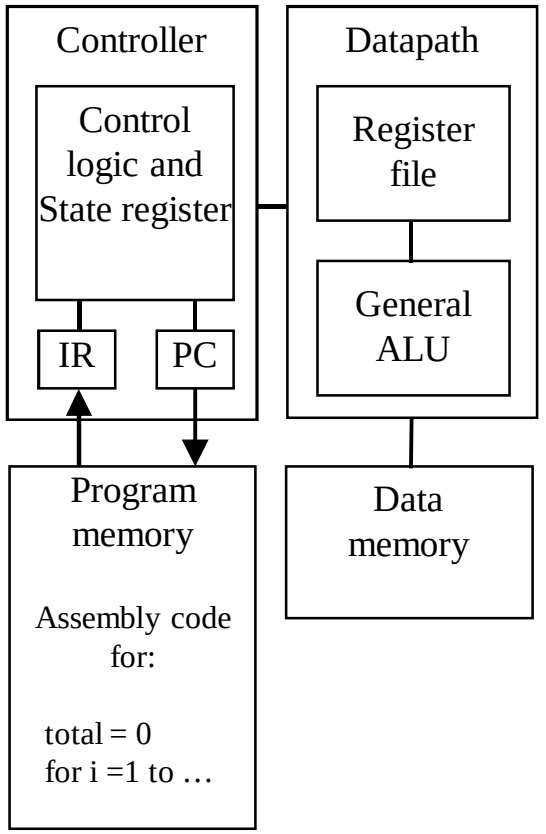
Programmable Logic Devices

Embedded Systems Technology

- Programmable Processors
- Application Specific Processor (ASIP)
- Single purpose hardware

General-purpose processors

- Programmable device used in a variety of applications
  - Also known as “microprocessor”
- Features
  - Program memory
  - General datapath with large register file and general ALU
- User benefits
  - Low time-to-market and NRE costs
  - High flexibility
- Example: Pentium, ARM, ...

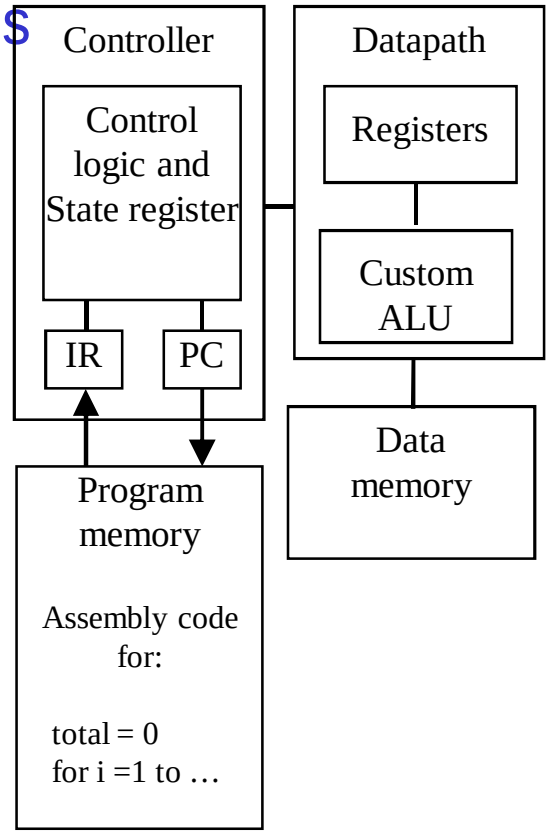


NRE and unit cost metrics

- Unit cost
  - the monetary cost of manufacturing each copy of the system, excluding NRE cost
- NRE cost (Non-Recurring Engineering cost)
  - The one-time monetary cost of designing the system
- total cost = NRE cost + unit cost * # of units
- per-product cost = total cost / # of units
  = (NRE cost / # of units) + unit cost

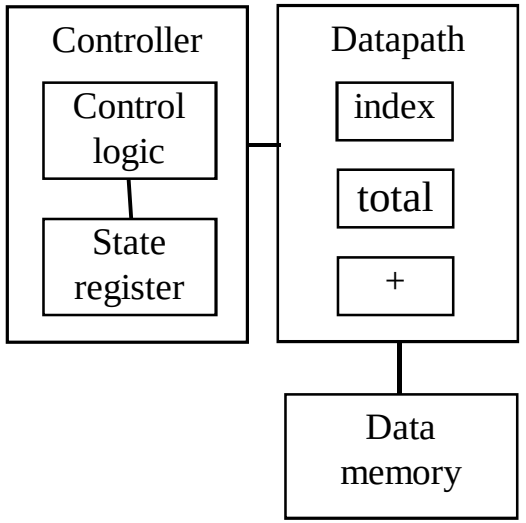
Application-specific processors

- Programmable processor optimized for a particular class of applications having common characteristics
- Features
  - Program memory
  - Optimized datapath
  - Special functional units
- Benefits
  - Some flexibility, good performance, size and power
- Example: DSP, Media Processor



Single-purpose hardware

- Digital circuit designed to execute exactly one program
  - coprocessor, accelerator
- Features
  - Contains components needed to execute a single program
  - No program memory
- Benefits
  - Fast
  - Low power
  - Small size



IC technology

- Three types of IC technologies
  - Full-custom/VLSI
  - Semi-custom ASIC (gate array and standard cell)
  - PLD (Programmable Logic Device)

Full-custom/VLSI

- All layers are optimized for an embedded system's particular digital implementation
  - Placing transistors
  - Sizing transistors
  - Routing wires
- Benefits
  - Excellent performance, small size, low power
- Drawbacks
  - High NRE cost (e.g., $300k), long time-to-market

Semi-custom

- Lower layers are fully or partially built
  - Designers are left with routing of wires and maybe placing some blocks
- Benefits
  - Good performance, good size, less NRE cost than a full-custom implementation (perhaps $10k to $100k)
- Drawbacks
  - Still require weeks to months to develop

PLD (Programmable Logic Device)

- All layers already exist
  - Designers can purchase an IC
  - Connections on the IC are either created or destroyed to implement desired functionality
  - Field-Programmable Gate Array (FPGA) very popular
- Benefits
  - Low NRE costs, almost instant IC availability
- Drawbacks
  - Bigger, expensive (perhaps $30 per unit), power hungry, slower

Comparison

Technology	Performance/ Cost	Time until running	Time to high performance	Time to change code functionality
ASIC	Very High	Very Long	Very Long	Impossible
FPGA	Medium	Medium	Long	Medium
ASIP/ DSP	High	Long	Long	Long
Generic	Low-Medium	Very Short	Not Attainable	Very Short

Roadmap

- PROM
- PLA
- PAL
- CPLD
- FPGA

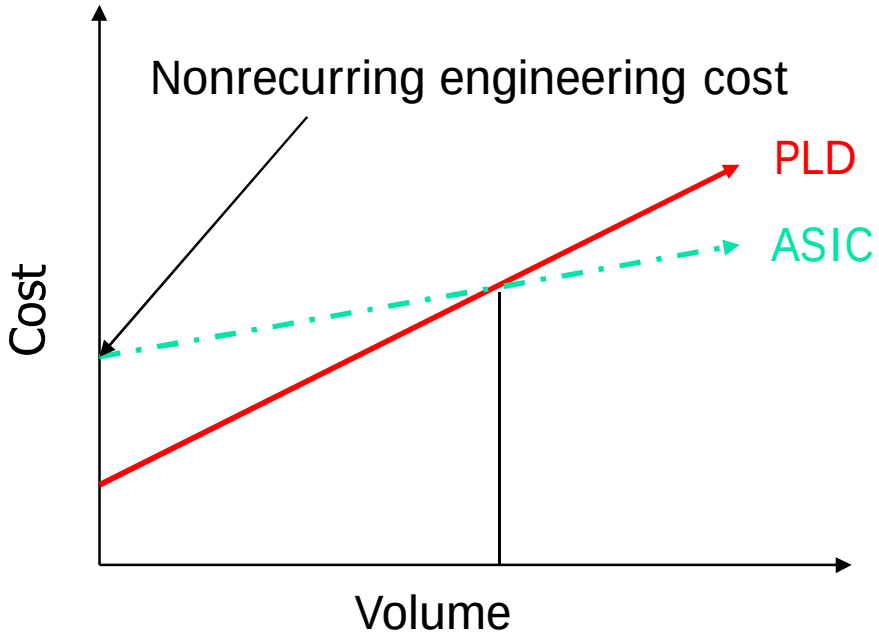
Reading

- *Digital Logic Circuit Analysis and Design* by Nelson, Nagle, Carrol, and Irwin : Chapter 5.3, 5.4, 5.5, 11.2
- *Architectures of FPGAs and CPLDs: A Tutorial* by Stephen Brown and Jonathan Rose [Available on the web: check out the link from lectures page]

PLD Definition

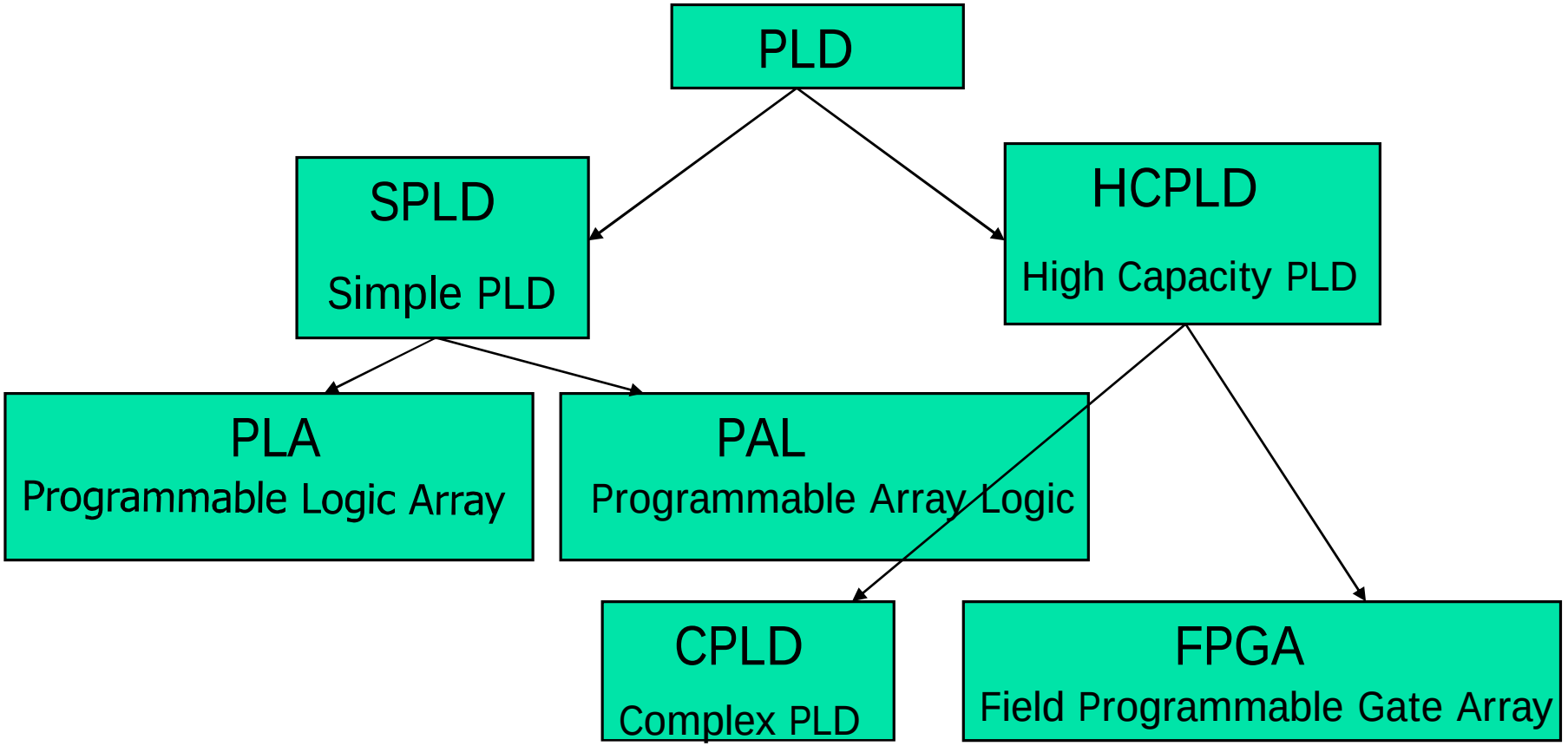
- Programmable Logic Device (PLD):
  - An integrated circuit chip that can be configured by end use to implement different digital hardware
  - Also known as “Field Programmable Logic Device (FPLD) “

PLD Advantages

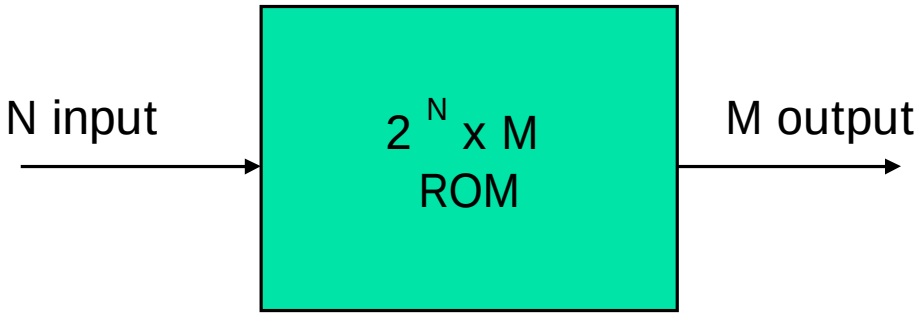


- Short design time
- Less expensive at low volume

PLD Categorization

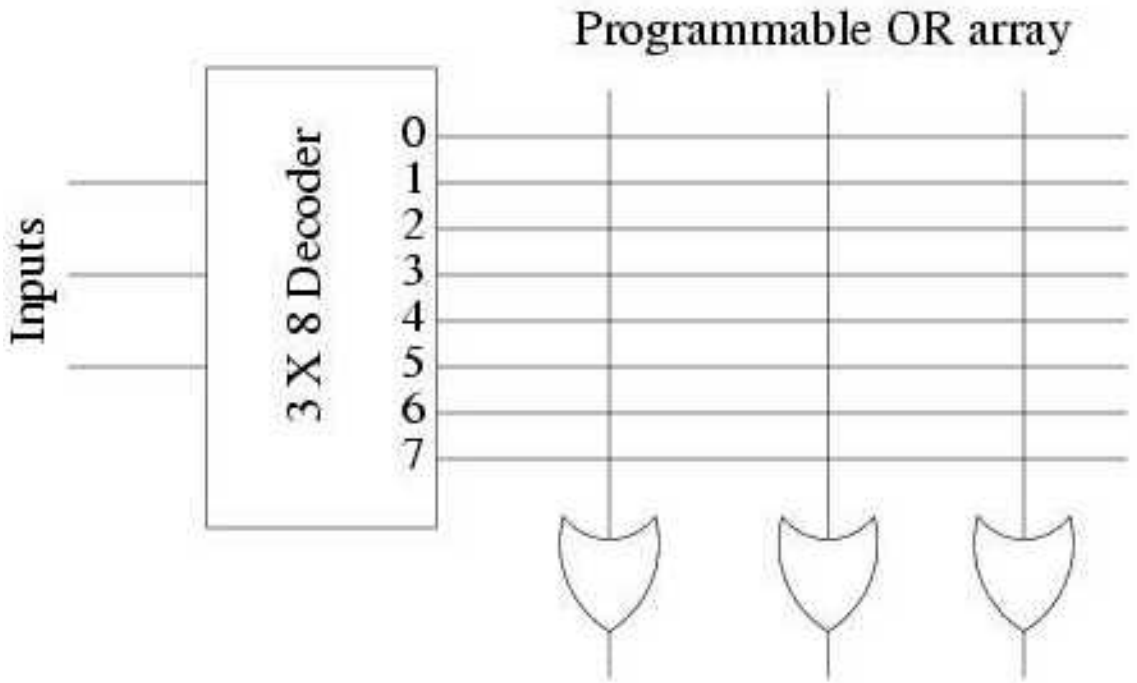


Programmable ROM (PROM)



- Address: N bits; Output word: M bits
- ROM contains 2^N words of M bits each
- The input bits decide the particular word that becomes available on output lines

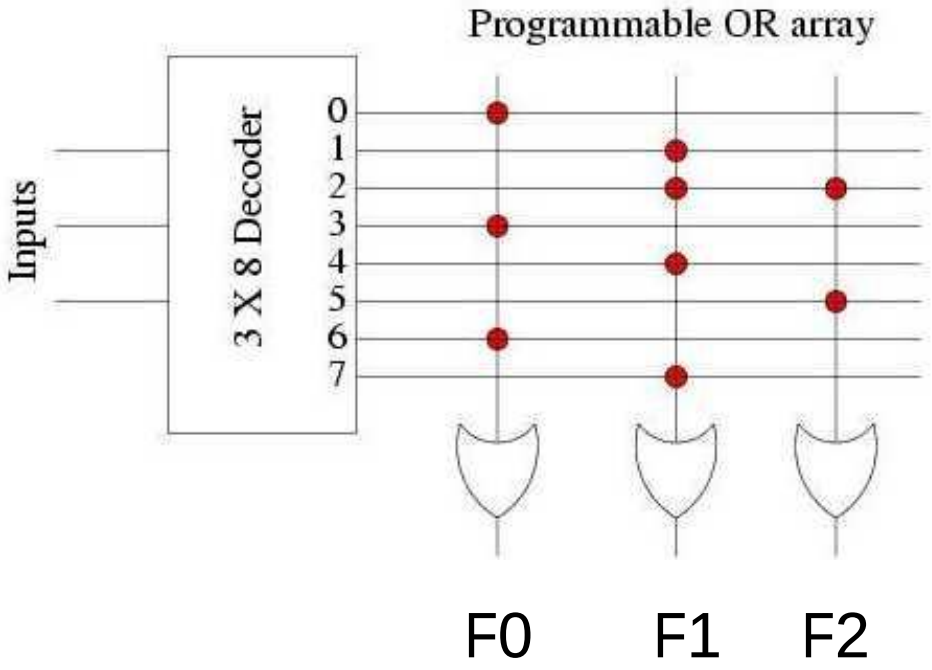
Logic Diagram of 8x3 PROM



Sum of minterms

Combinational Circuit Implementation using PROM

I0	I1	I2	F0	F1	F2
0	0	0	1	0	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	1	0	0
1	1	1	0	1	0



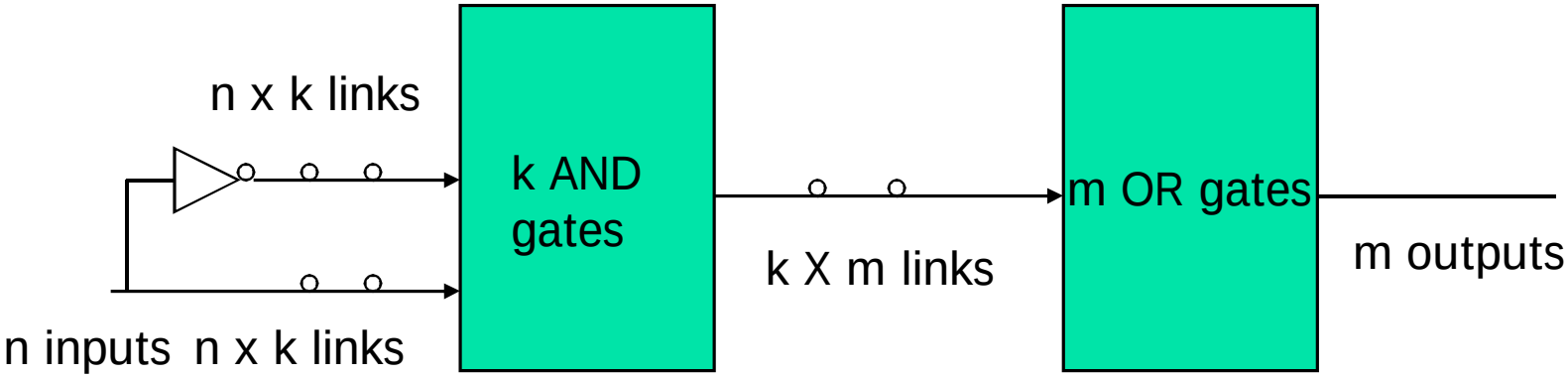
PROM Types

- Programmable PROM
  - Break links through current pulses
  - Write once, Read multiple times
- Erasable PROM (EPROM)
  - Program with ultraviolet light
  - Write multiple times, Read multiple times
- Electrically Erasable PROM (EEPROM)/ Flash Memory
  - Program with electrical signal
  - Write multiple times, Read multiple times

PROM: Advantages and Disadvantages

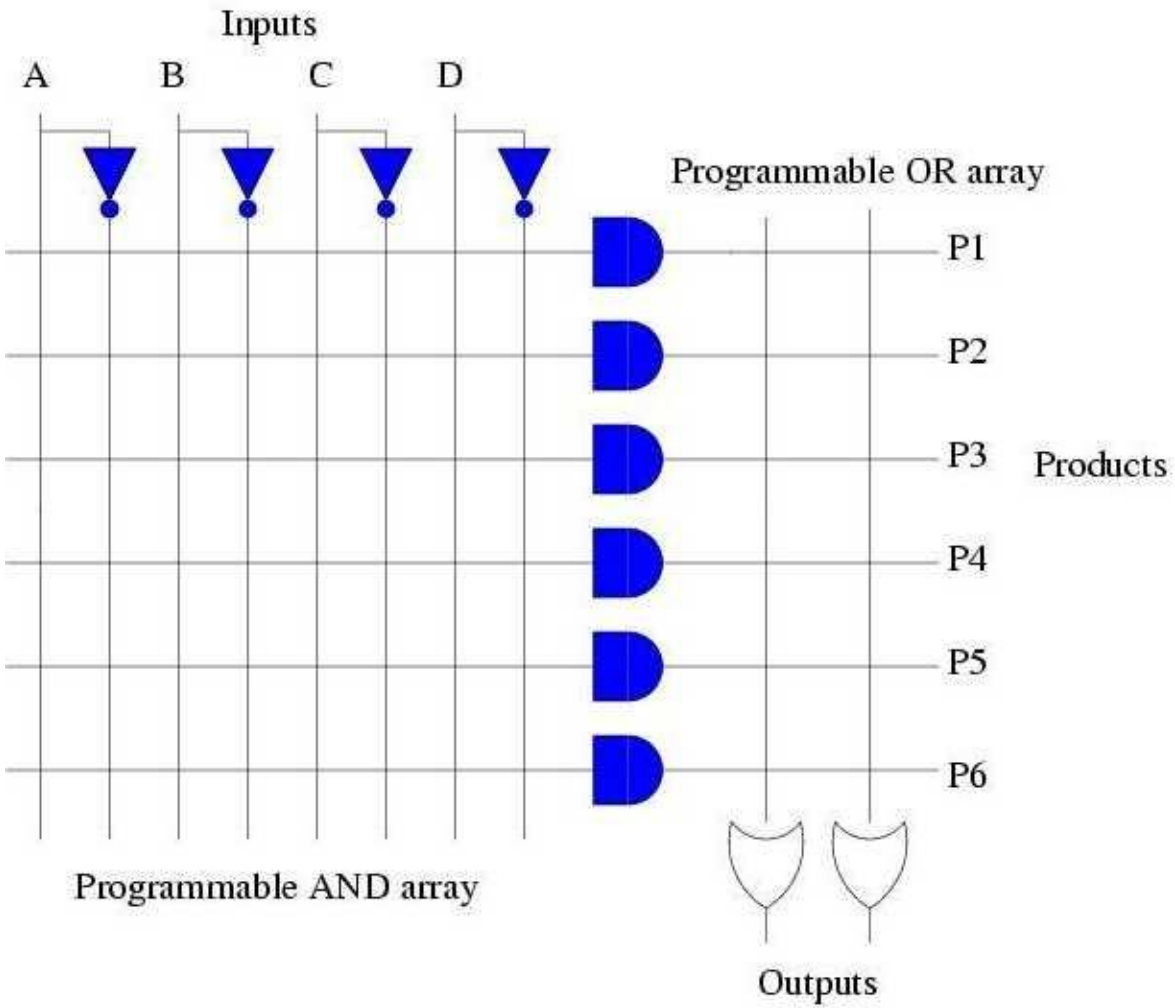
- Widely used to implement functions with large number of inputs and outputs
- Design of control units (Micro-programmed control units)
- For combinational circuits with lots of don't care terms, PROM is a wastage of logic resources

Programmable Logic Array



- Programmable AND array + programmable OR array
- n x k x m PLA has 2n x k + k x m links
- Sum of products

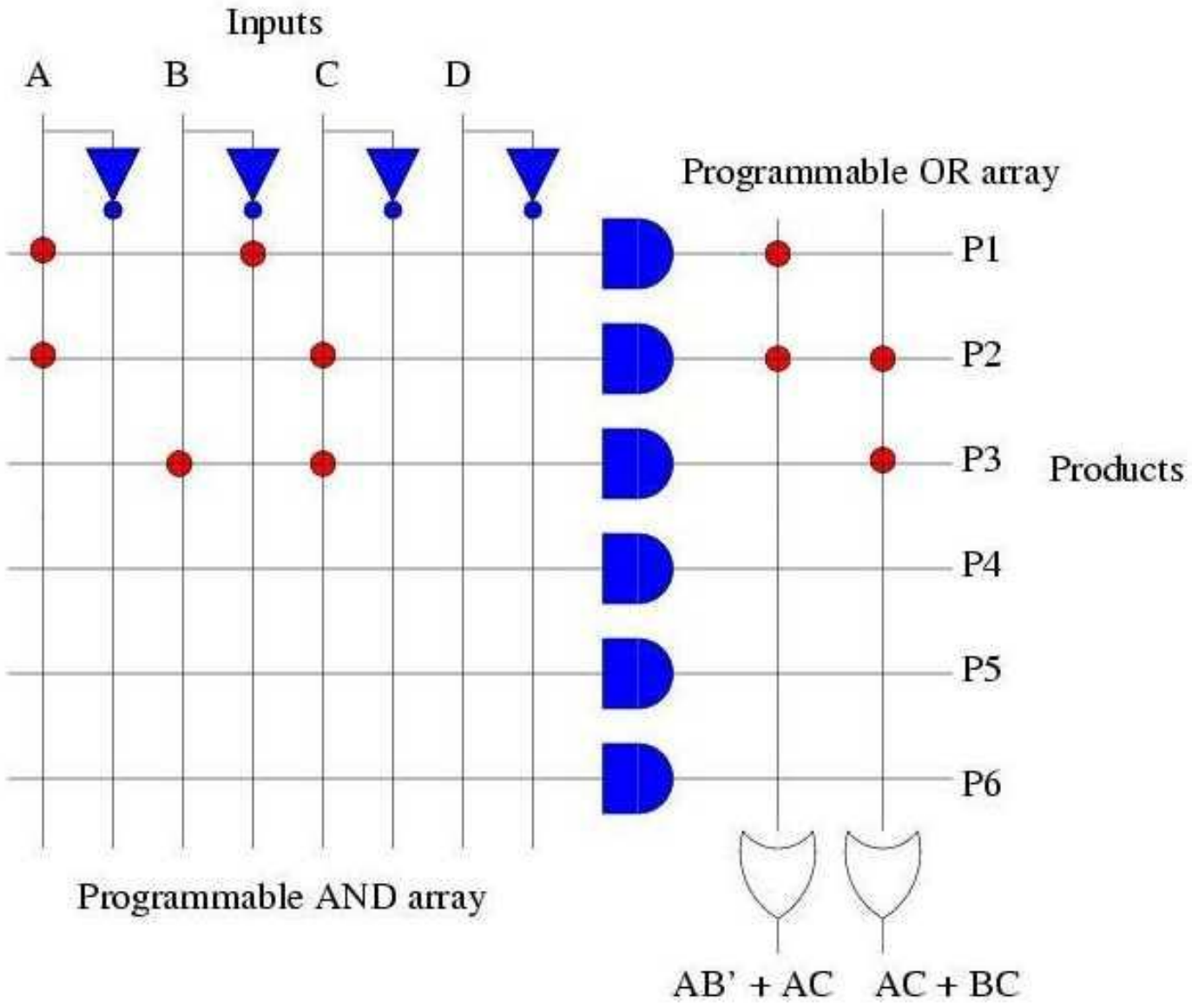
PLA 4 X 6 X 2


Inputs
A
B
C
D
Programmable OR array
P1
P2
P3
P4
P5
P6
Products
Programmable AND array
Outputs

Logic Implementation with PLA

- Finite number of AND gates => simplify function to minimum number of product terms
- Number of literals in a product term is not important since we have all the input variables
- Sharing of product terms between outputs => multiple-output minimization

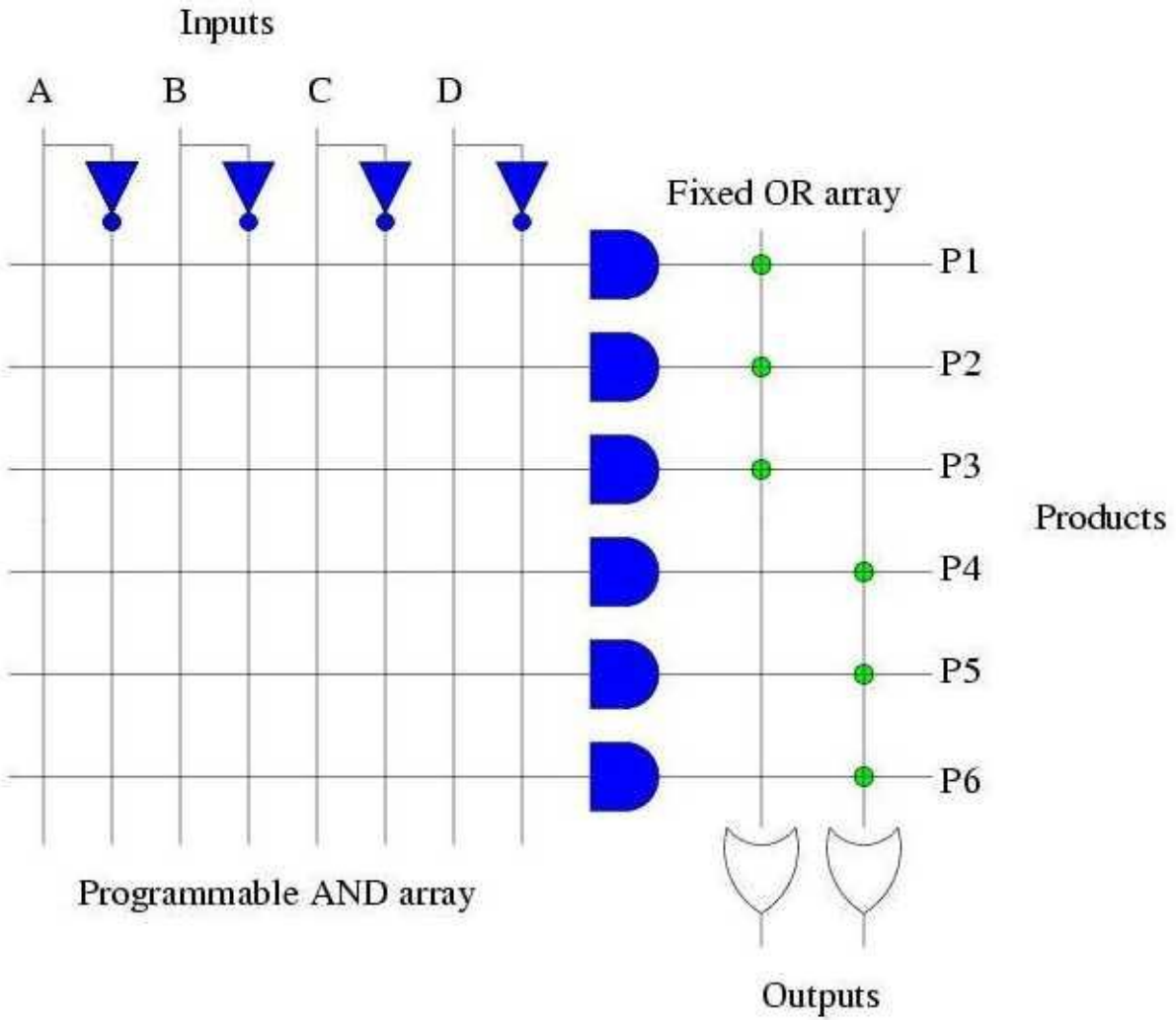
Design with PLA



Programmable Array Logic (PAL)

- Programmable AND array
- Fixed OR array
  - Each output line permanently connected to a specific set of product terms
- Number of switching functions that can be implemented with PAL are more limited than PROM and PLA

PAL Logic Diagram



PAL Implications

- Number of product terms per output > number of product terms in each sum-of-product expression
- No sharing of product terms between outputs

Design with PAL