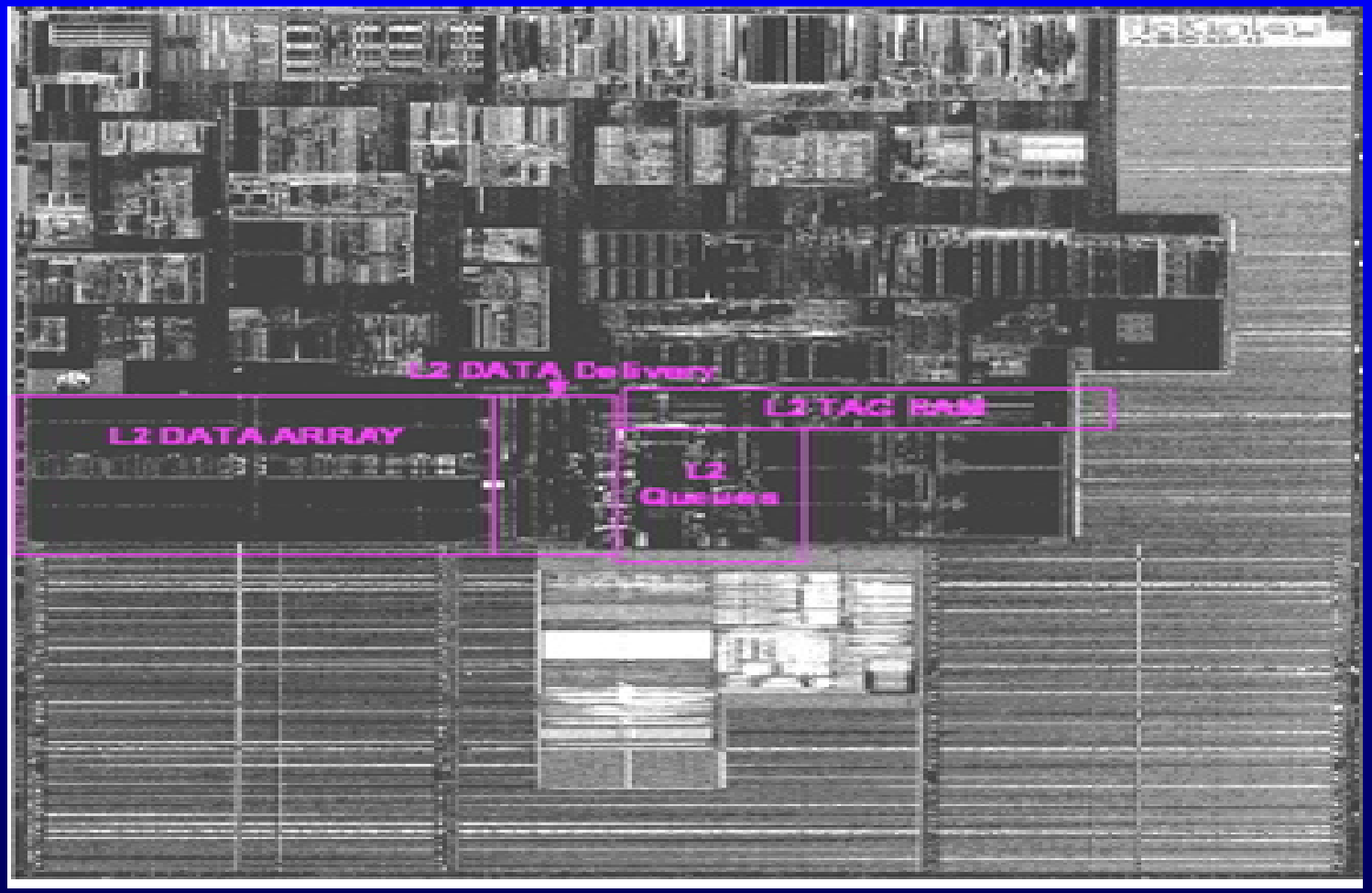
Power Issues in VLSI Design



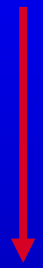
Outline of the talk

- CMOS Energy and Power – Why is it an issue?
- Clock Gating.
- Dynamic Voltage Scaling.
- Dynamic Power Management.
- Battery Awareness.

CMOS Energy and Power

$$E = C_L V_{DD}^2 P_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} P_{0/1\rightarrow1/0} + V_{DD} I_{leak}/f$$

$$f = P * f_{clock}$$



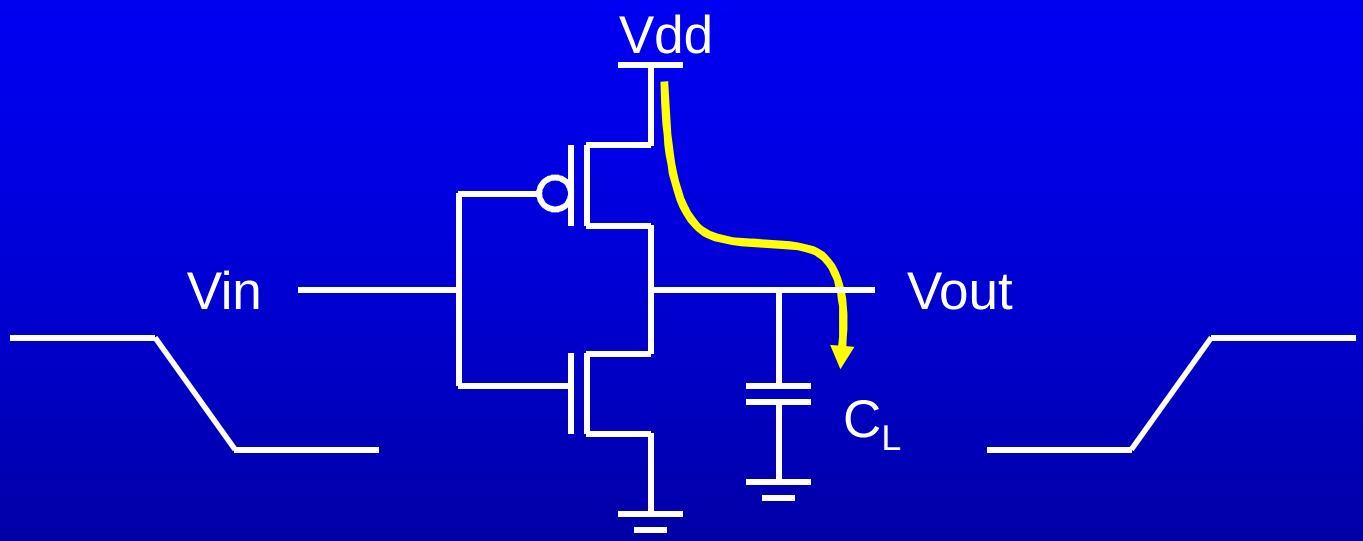
$$P = C_L V_{DD}^2 f + t_{sc} V_{DD} I_{peak} f + V_{DD} I_{leak}$$

Dynamic power (~80% today and decreasing relatively)

Short-circuit power (~5% today and decreasing absolutely)

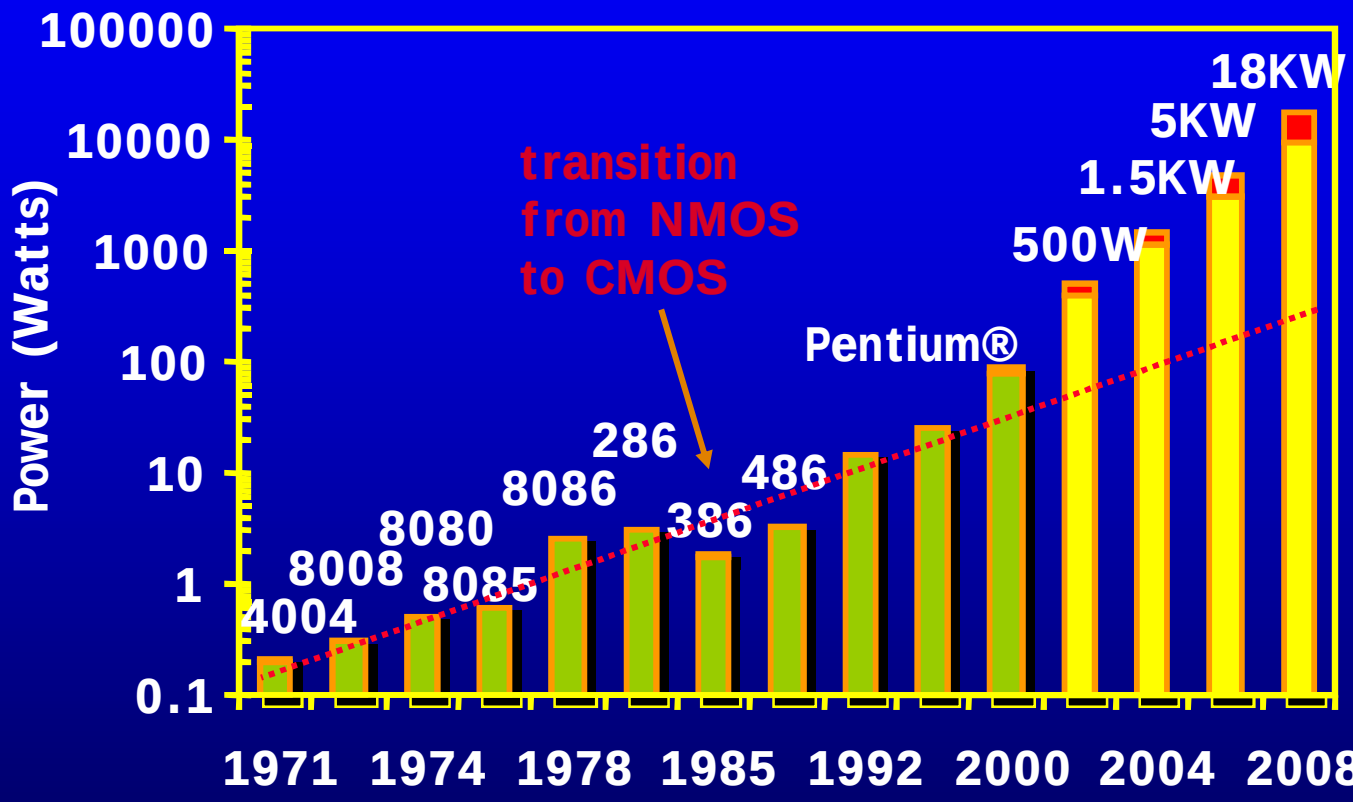
Leakage power (~15% today and increasing)

Dynamic Energy Consumption



Energy/transition = $C_L * V_{DD}^2 * P_{0\rightarrow1}$

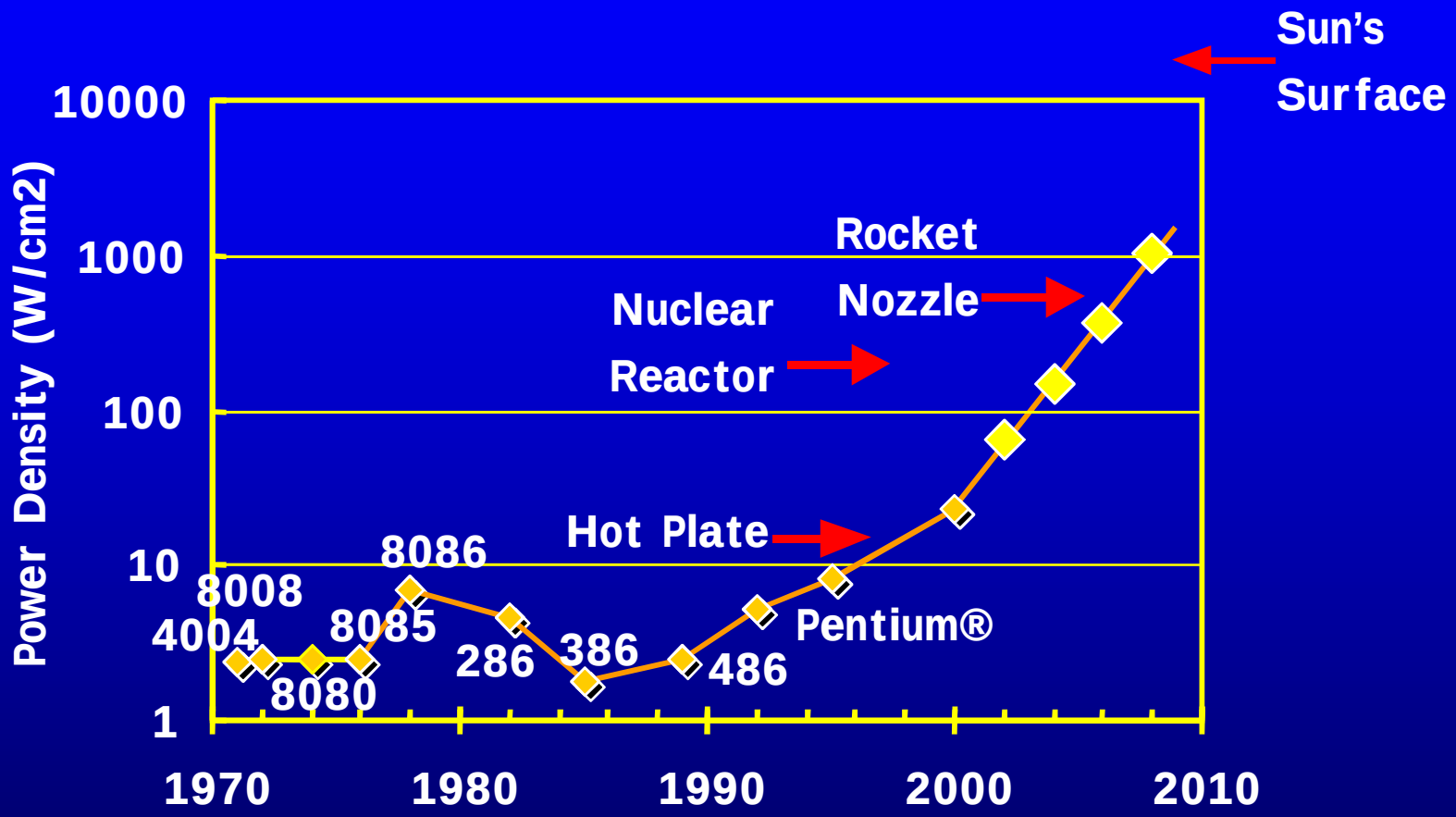
Scaling is worsening the problem



Power delivery and dissipation will be prohibitive !

Source: Borkar, De Intel®

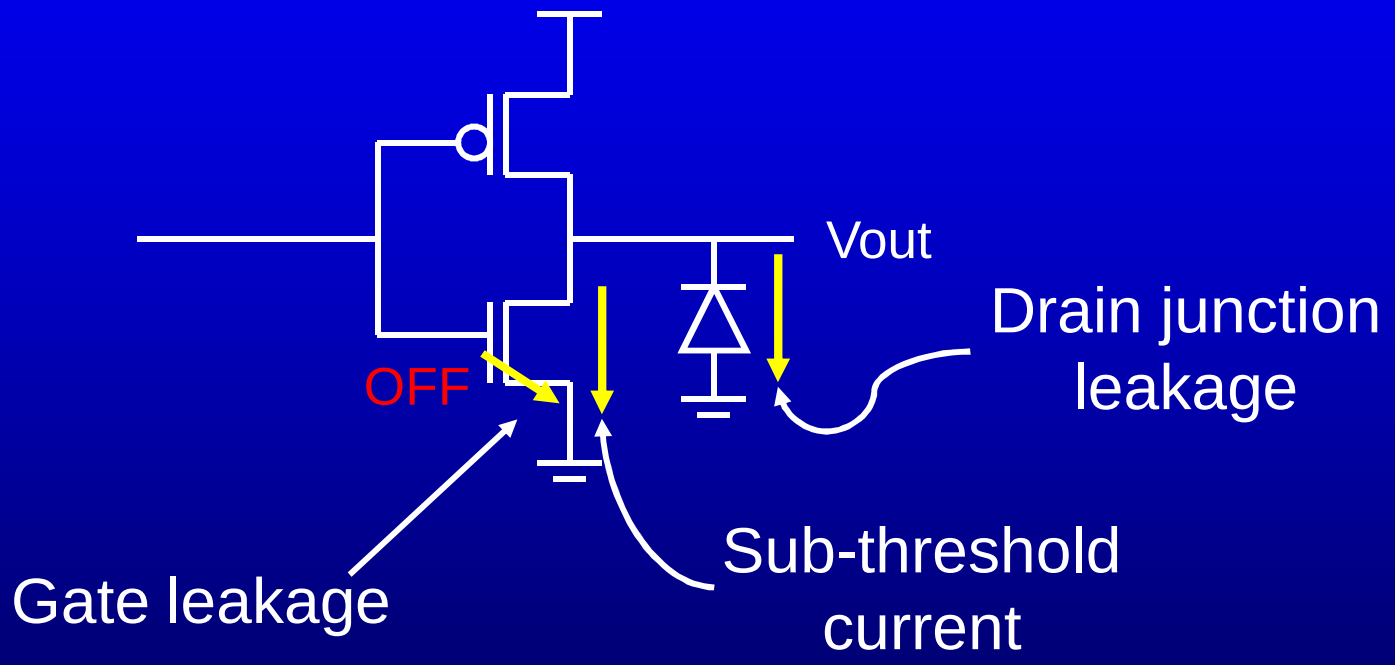
Power Density will Increase



Power densities too high to keep junctions at low temps

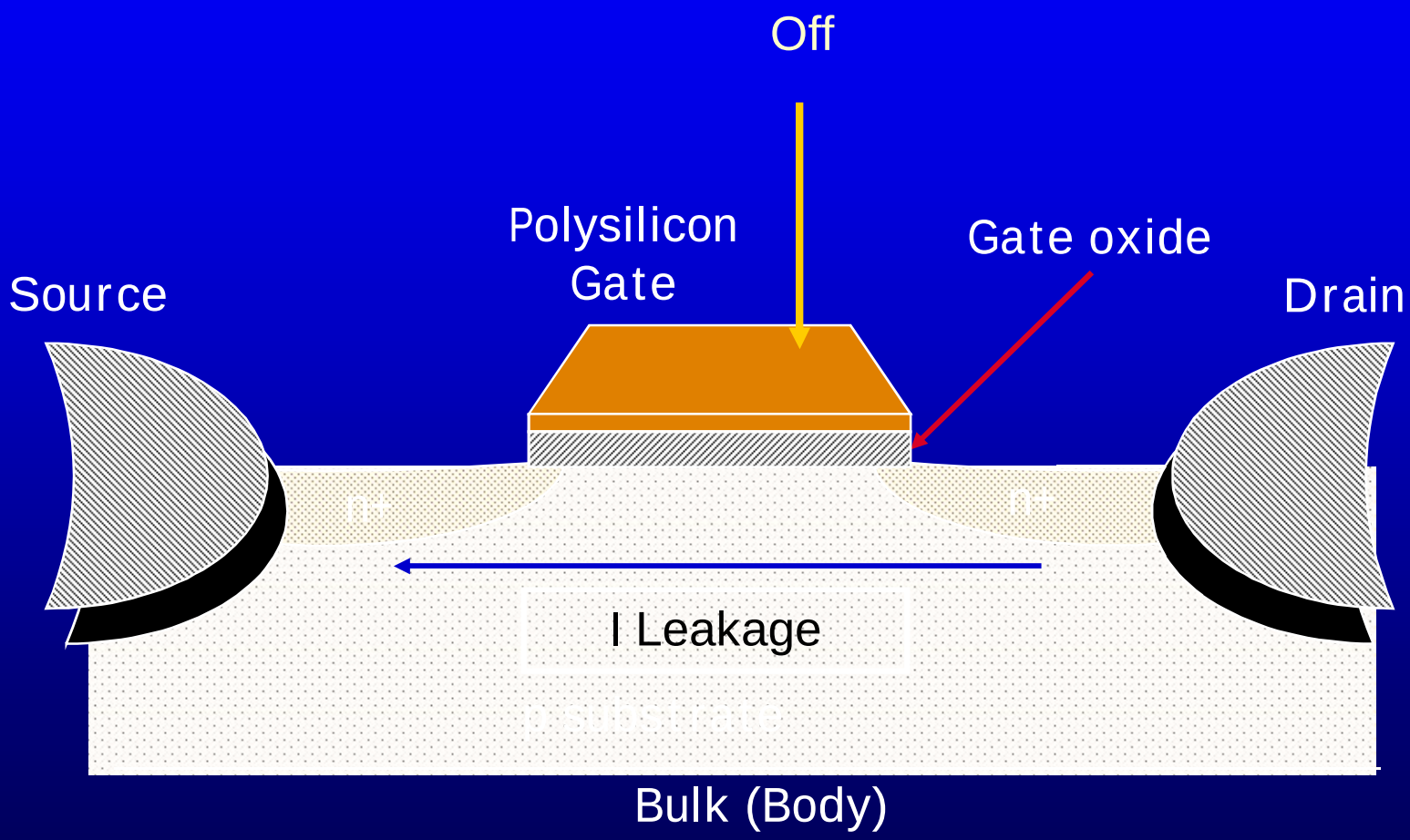
Source: Borkar, De Intel®

Leakage Power



Independent of switching

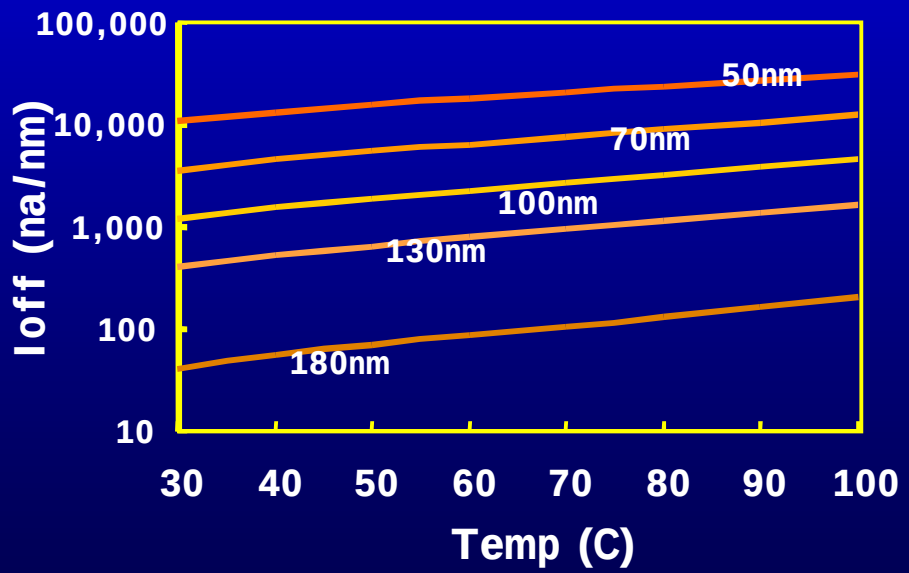
Leakage Current

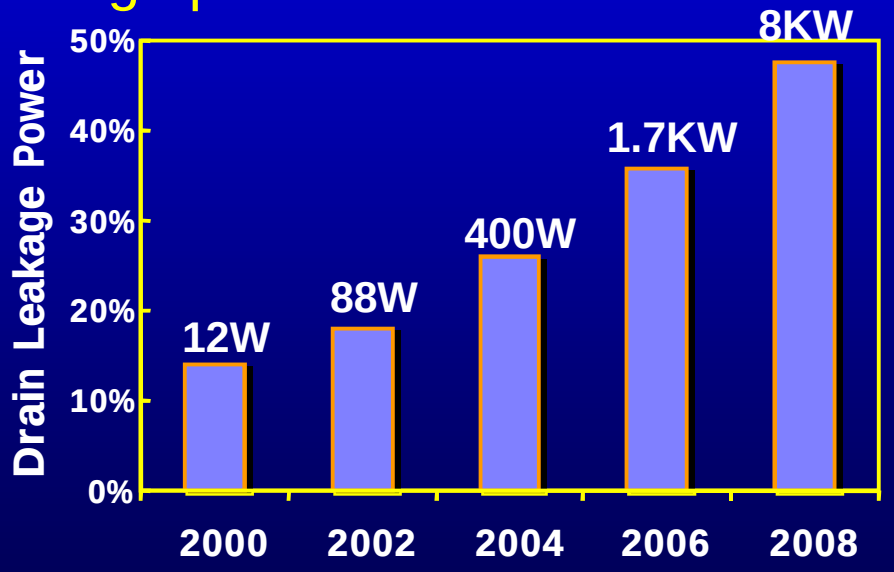


Scaling worsens leakage power

Year	1999	2002	2005	2008	2011	2014
Feature size (nm)	**180**	**130**	**100**	**70**	**50**	**35**
Logic trans/Chip (M)	**15**	**60**	**235**	**925**	**3,650**	**14,400**
Power supply V_{dd} (V)	**1.8**	**1.5**	**1.2**	**0.9**	**0.7**	**0.6**
Threshold V_T (V)	**0.5**	**0.4**	**0.4**	**0.35**	**0.3**	**0.25**

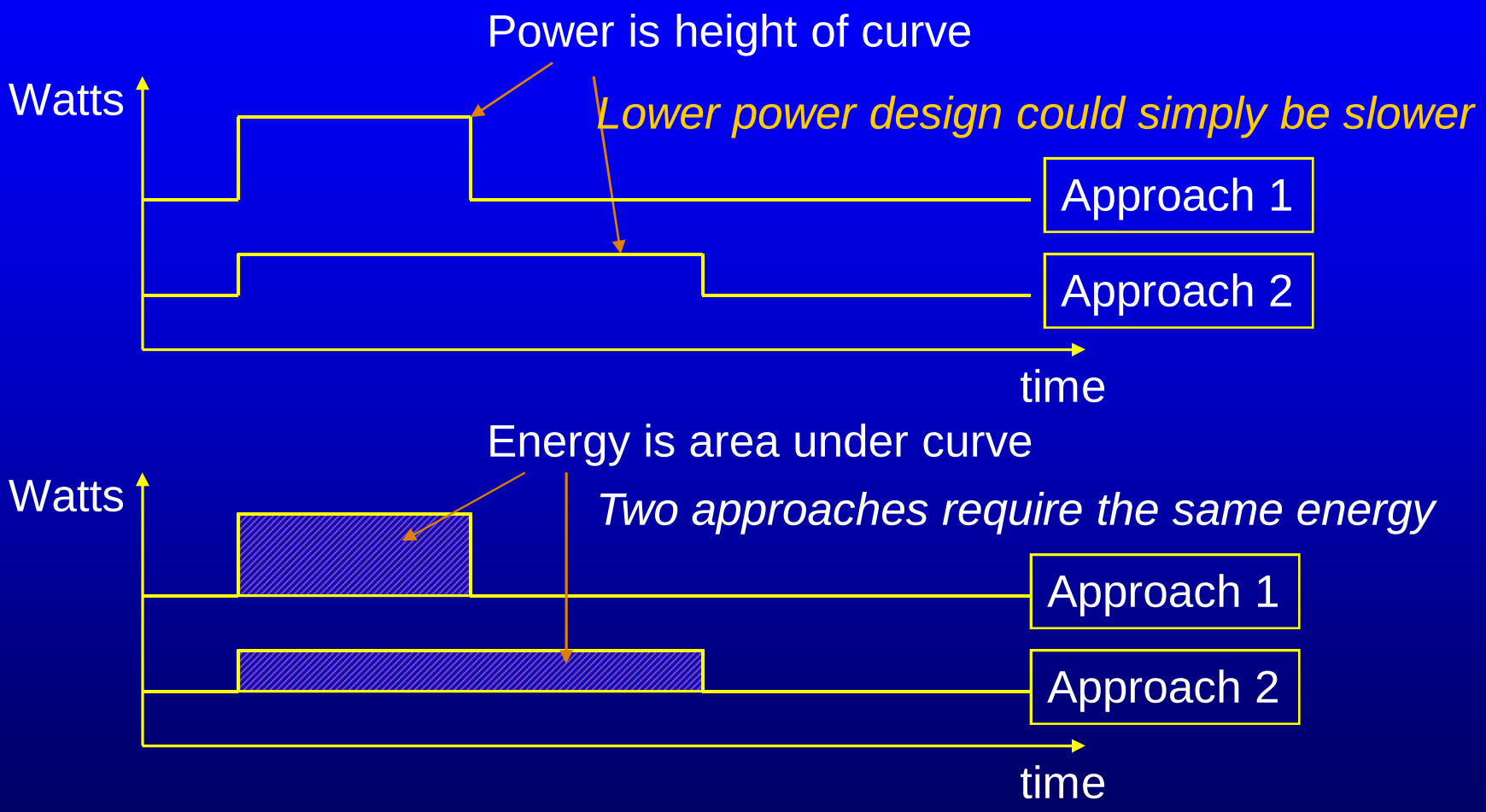
Drain leakage increases as V_T decreases to meet frequency demands leading to excessive leakage power.





Source: Borkar, Intel®

Power versus Energy



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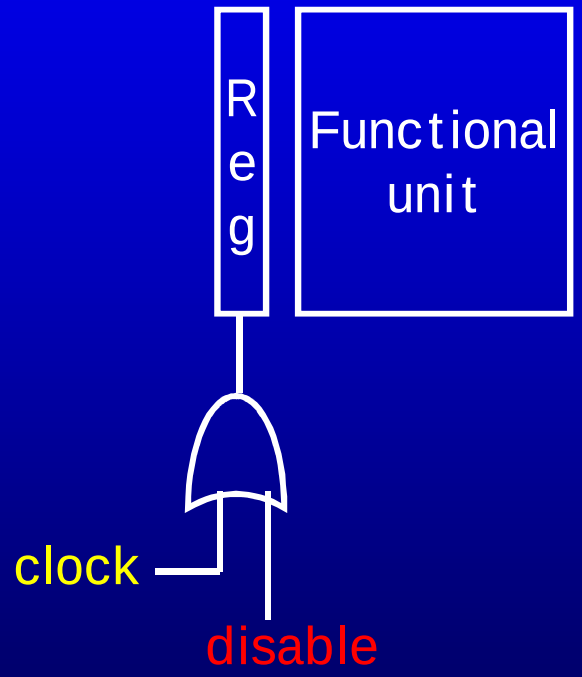
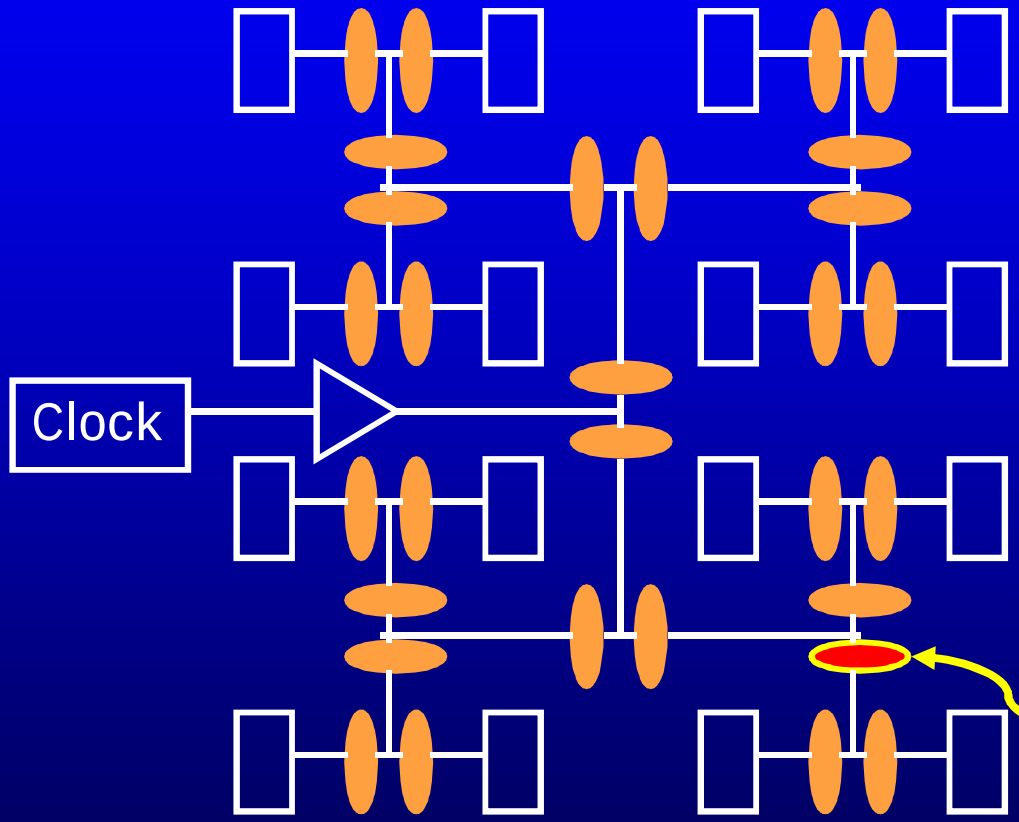
Clock Gating

Most popular method for power reduction of clock signals and functional units



Gated Clock Distribution

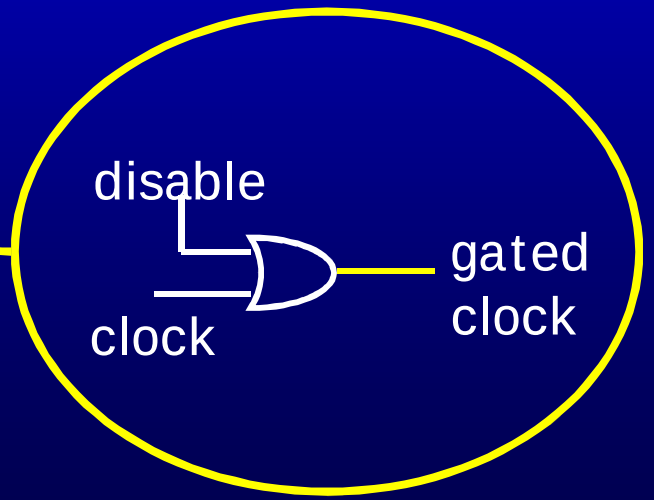
If the paths are perfectly balanced, clock skew is zero



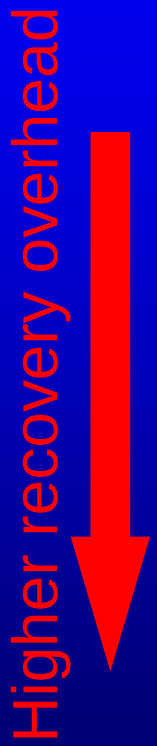
H-Tree Clock Network

Can insert clock gating at multiple levels in clock tree

Can shut off entire subtree if all gating conditions are satisfied



Clock Gating Levels



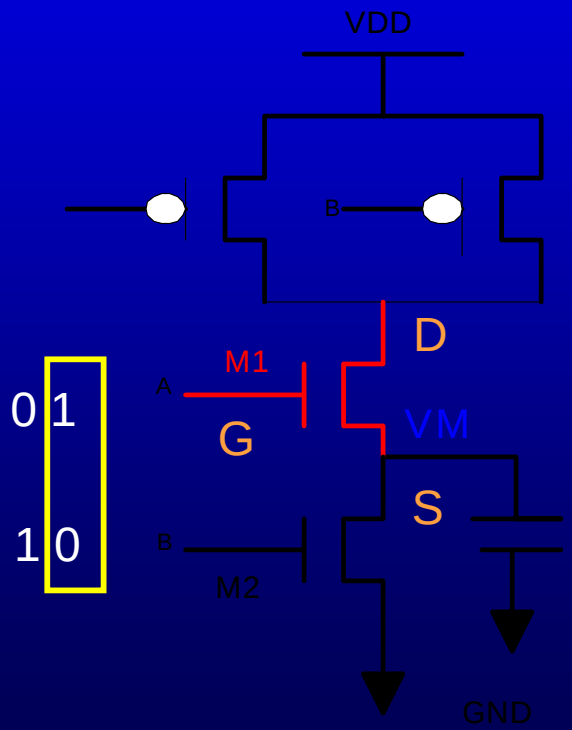
- **Fine-grain**
  - E.g., portions of the pipeline register are disabled depending on whether the information they hold is used in the next stages
- **Medium-grain**
  - E.g., disable cache precharging during cache miss
- **Coarse-grain**
  - E.g., eliminate switching of the clock's main driver

Reducing Leakage

- Static power in “off-state” is a serious concern in nanometer technologies
- Techniques tradeoff leakage reduction for ease of recovery from shutdown
  - Most of the techniques have non-negligible recovery cost
  - Dual-mode CT model does not hold!

I. Input Vector Control

- **Transistor Stack Effect: the leakage reduction effect in a transistor stack when more than one transistor is turned off.**



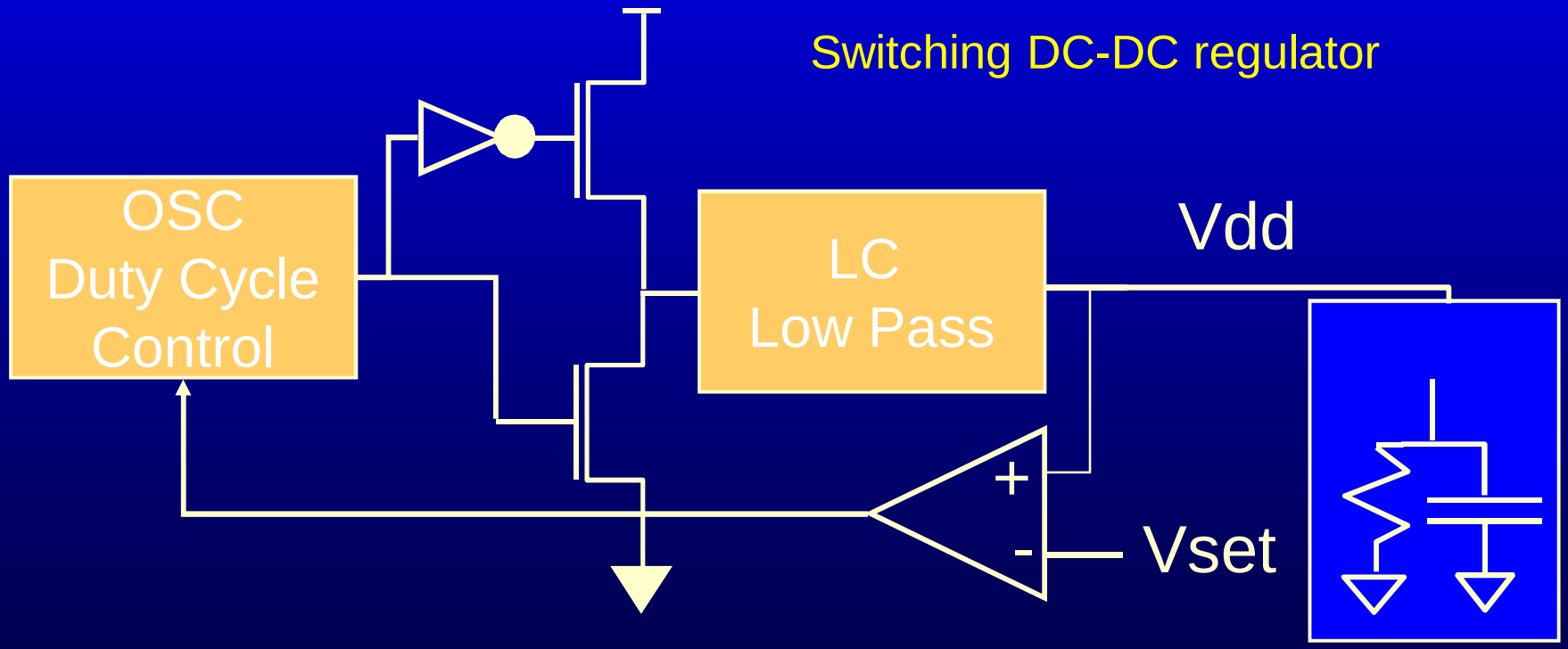
A simple 2-input NAND gate

II. Supply Gating

- Gating the Power Supply
  - The power supply is shut down so that idle units do not consume leakage power
- If there is intention to provide support for Dynamic Voltage Scaling (DVS):
  - Switching regulators
  - On-chip voltage generators (PLL)

Power Supply Switching

- **Requires re-stabilization of Vdd**
- **Significant time and power cost**



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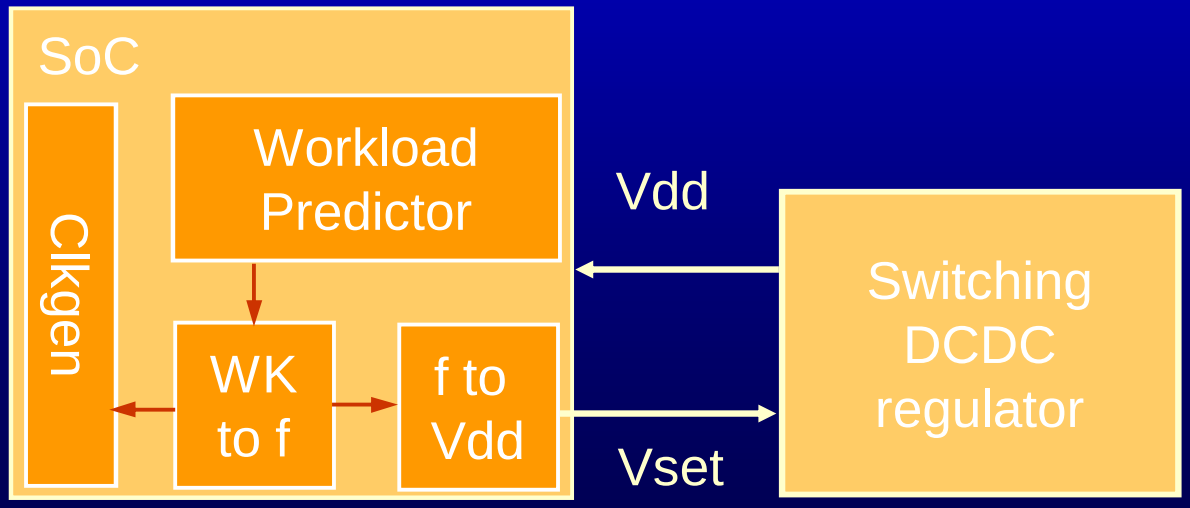
Exploiting Variable Supply

- Supply voltage can be dynamically changed during system operation
  - Cubic power savings
  - Circuit slowdown
- Just-in-time computation
  - Stretch execution time up to the max tolerable

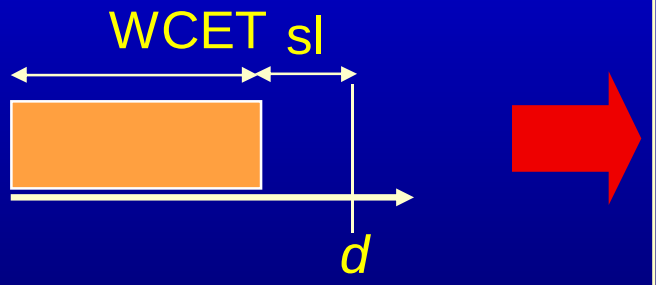
Variable-supply Architectures

- High-efficiency adjustable DC-DC converter
- Adjustable synchronization
  - Variable-frequency clock generator [Chandrakasan96]
  - Self-timed circuits [Nielsen94]



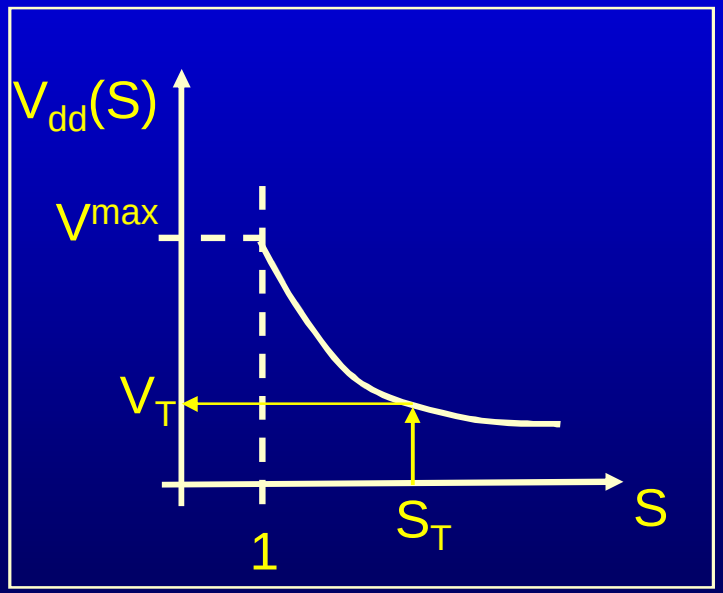
Basic problem formulation

- **Given a task, with known WCET and deadline *d***
  - **Find the optimal voltage for the processor that runs it (minimize energy without violating *d*)**



S_T=(WCET+sl)/WCET

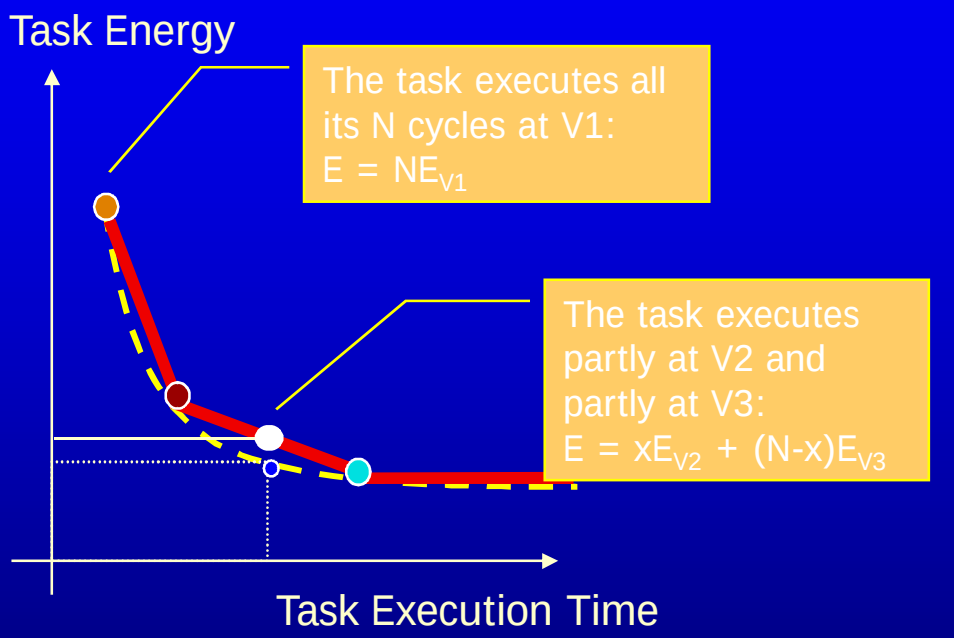
S=1/(Utilization)



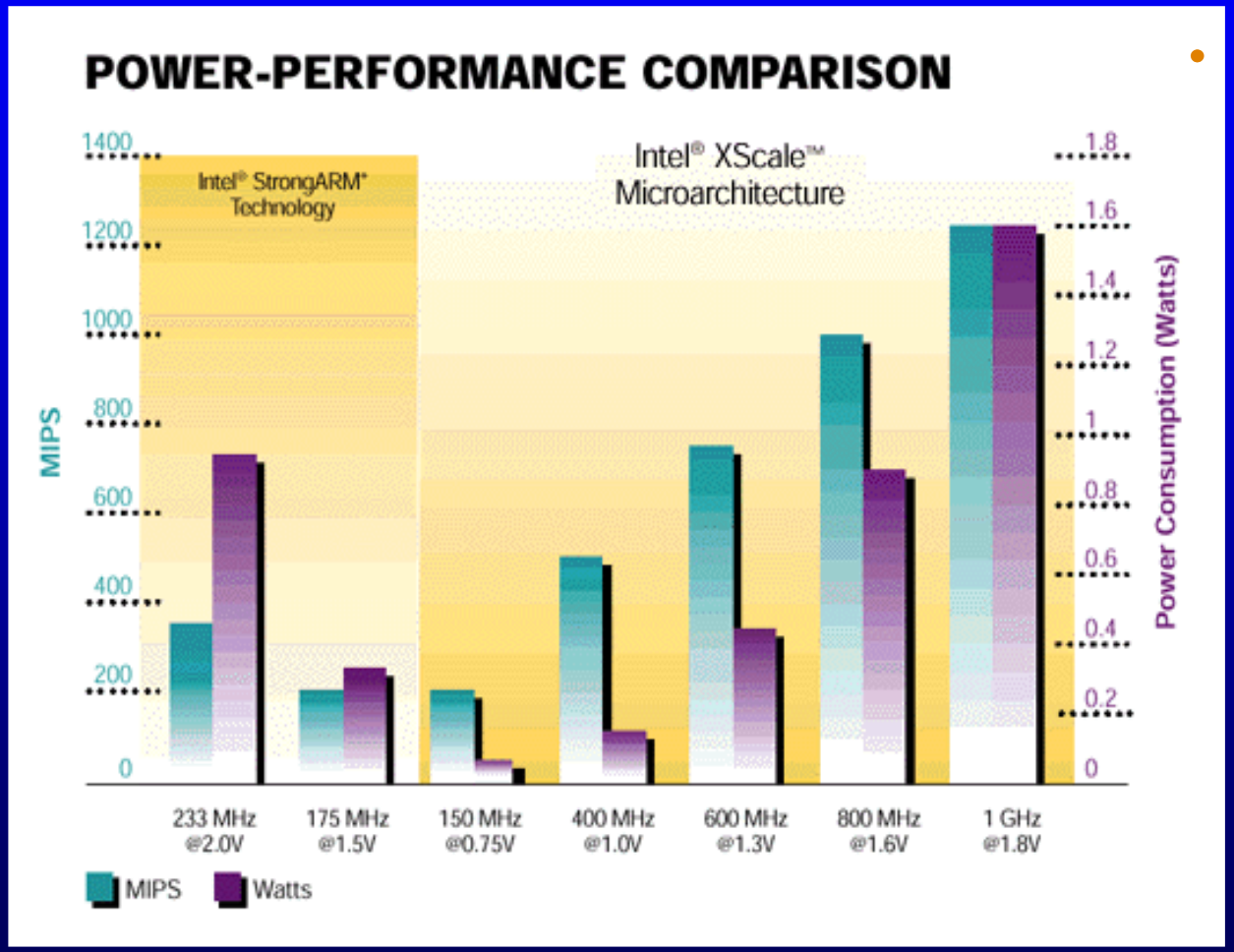
Accounting for limited (f,V_{dd}) resolution

- **Frequency interpolation**
  - **Given a task with N operations**
  - **Compute optimum ($f_{ideal},V_{dd,ideal}$)**
  - **Find the two closest available frequencies**
    - » $f_L<f_{ideal}<f_H$
  - **Run for X at f_L and (N-X) at f_H**

    $N*f_{ideal}= X*f_L + (N-X)*f_H$



Intel Xscale – Supports DVS



- **Transition penalties**
  - **Dominated by supply voltage transient**
  - **1mV / 2µsec**

From Intel's Web Site

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Battery Awareness

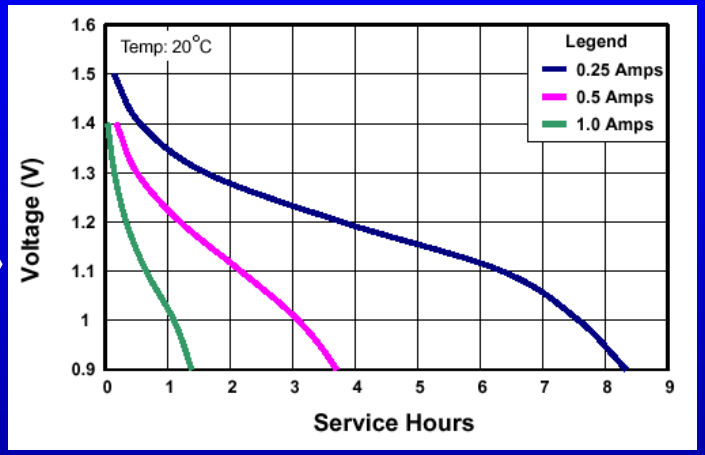
- **The traditional algorithms on DVS considers battery as an ideal power source, *i.e.* energy delivered by the battery is constant under varying conditions of voltages and currents.**

Battery is Important!!

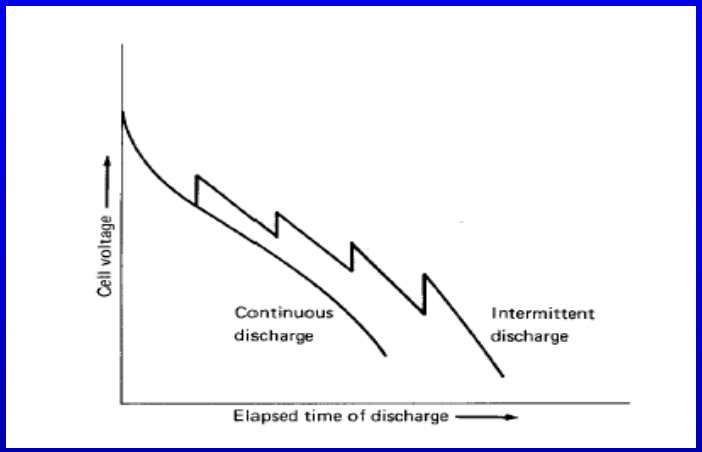
- Battery behaviour is very complex which is the result of complex electro-chemical reactions inside battery.
- Energy/charge delivered by the battery is dependent on discharge profile (voltages and currents).
- An accurate battery model is required.

Battery Life Modeling

- effect

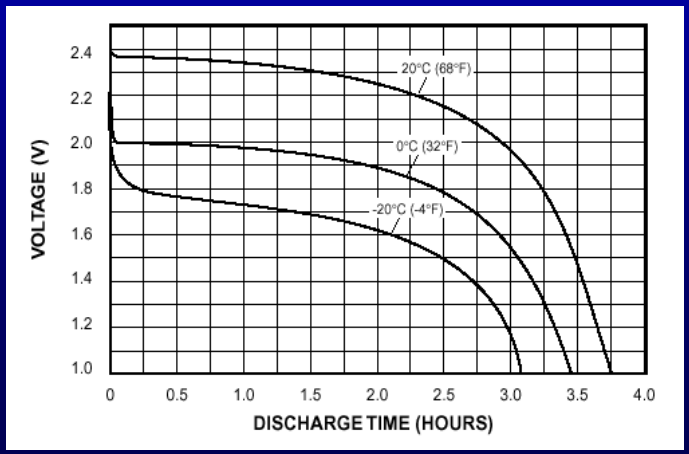


Rate Capacity Effect

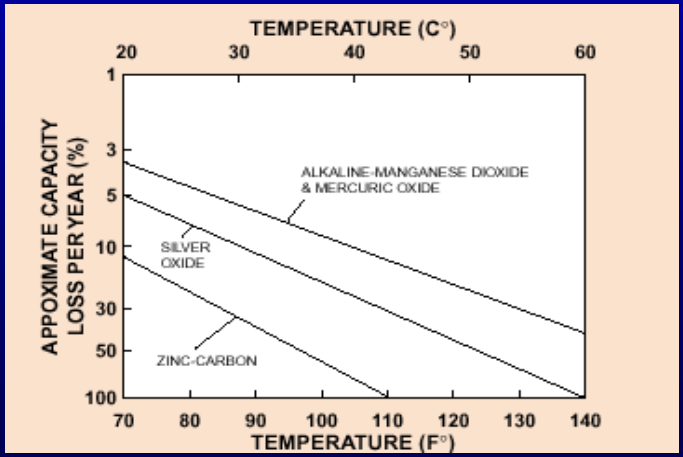


+ effect

Recovery Effect



Temperature Effect



Shelf Life Effect

Summary

- **Power is becoming the restraining factor in further miniaturization and scaling.**
- **Various methodologies available but still a lot of scope for improvement.**
- **Need for developing of infrastructure.**
- **Combining of discrete power saving techniques into a single integrated system.**
- Rate Capacity effect -> **Battery efficiency decreases with increase in current.**
- Recover effect -> **Battery tends to recover some charge if even rest periods.**