Introduction to CMOS VLSI Design

MOS devices: static and dynamic behavior

Activity

1) If the width of a transistor increases, the current will

increase decrease not change

2) If the length of a transistor increases, the current will

increase decrease not change

3) If the supply voltage of a chip increases, the maximum transistor current will

increase decrease not change

4) If the width of a transistor increases, its gate capacitance will

increase decrease not change

5) If the length of a transistor increases, its gate capacitance will

increase decrease not change

6) If the supply voltage of a chip increases, the gate capacitance of each transistor will

increase decrease not change

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increase **decrease** not change

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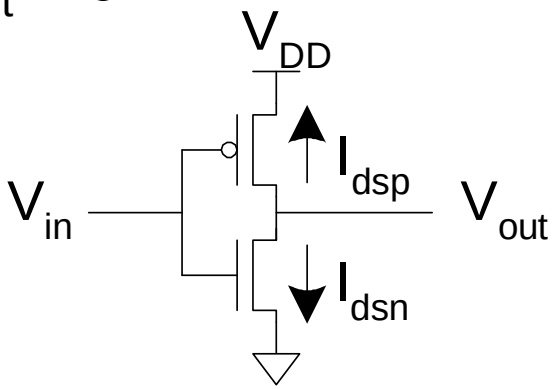
6) If the supply voltage of a chip increases, the gate capacitance of each transistor will

increase decrease **not change**

DC Response

- DC Response: V_{out} vs. V_{in} for a gate
- Ex: Inverter
  - When $V_{in} = 0$ -> $V_{out} = V_{DD}$
  - When $V_{in} = V_{DD}$ -> $V_{out} = 0$
  - In between, V_{out} depends on transistor size and current
  - By KCL, must settle such that $I_{dsn} = |I_{dsp}|$
  - We could solve equations
  - But graphical solution gives more insight

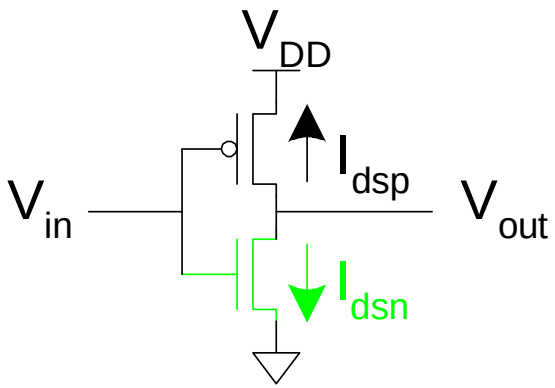


Transistor Operation

- Current depends on region of transistor behavior
- For what V_{in} and V_{out} are nMOS and pMOS in
  - Cutoff?
  - Linear?
  - Saturation?

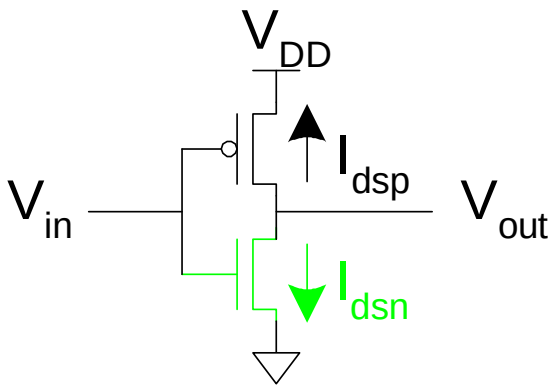
nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} <$	$V_{gsn} >$	$V_{gsn} >$
	$V_{dsn} <$	$V_{dsn} >$



nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$

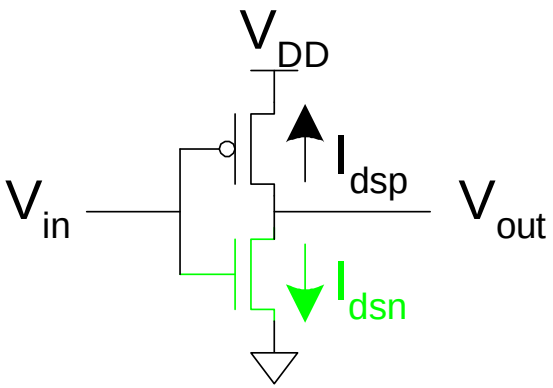


nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$

$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$

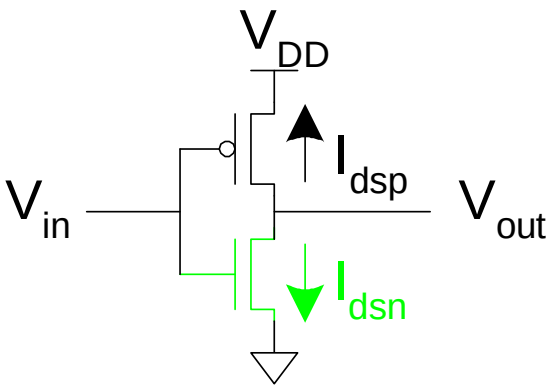


nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
	$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
	$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$

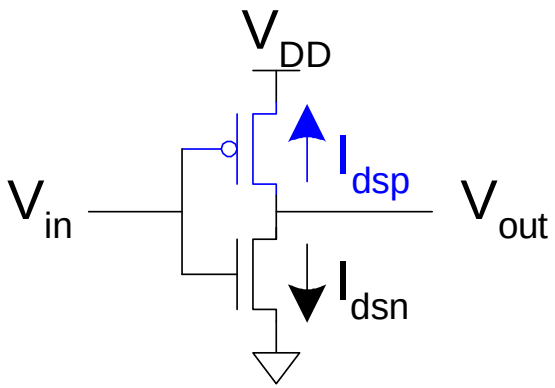
$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$



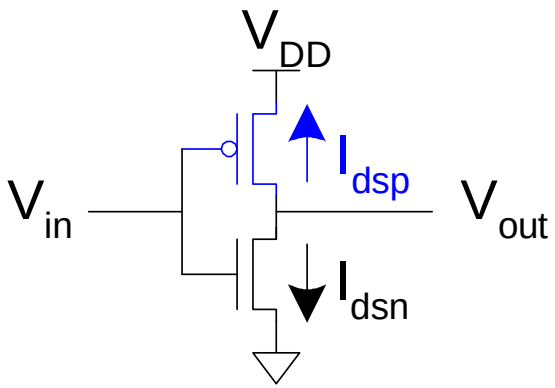
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} >$	$V_{gsp} <$	$V_{gsp} <$
	$V_{dsp} >$	$V_{dsp} <$



pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$



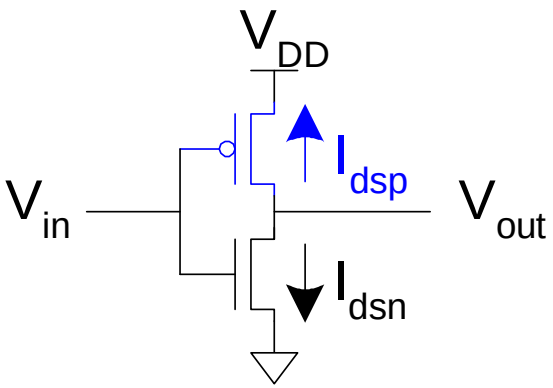
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$

$V_{gsp} = V_{in} - V_{DD}$

$V_{dsp} = V_{out} - V_{DD}$

$V_{tp} < 0$



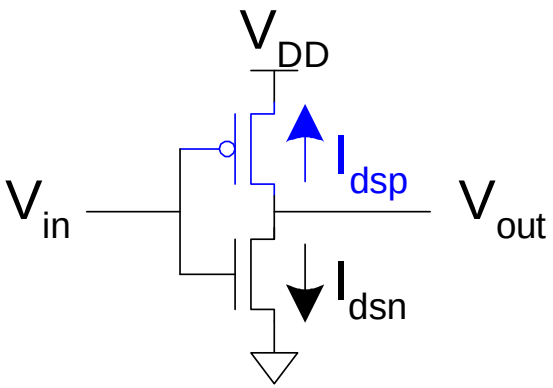
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$ $V_{in} > V_{DD} + V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} > V_{gsp} – V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} < V_{gsp} – V_{tp}$ $V_{out} < V_{in} - V_{tp}$

$V_{gsp} = V_{in} - V_{DD}$

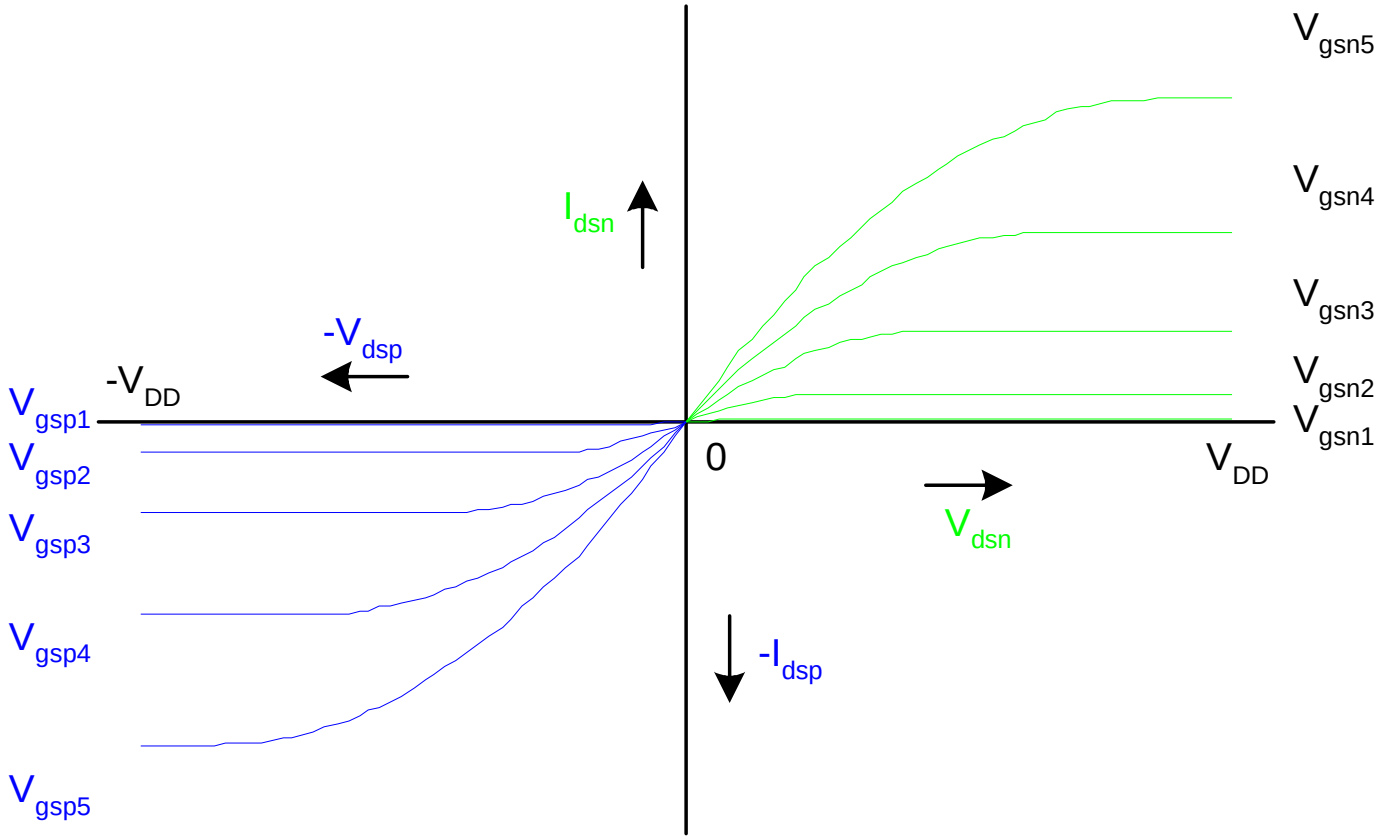
$V_{dsp} = V_{out} - V_{DD}$

$V_{tp} < 0$

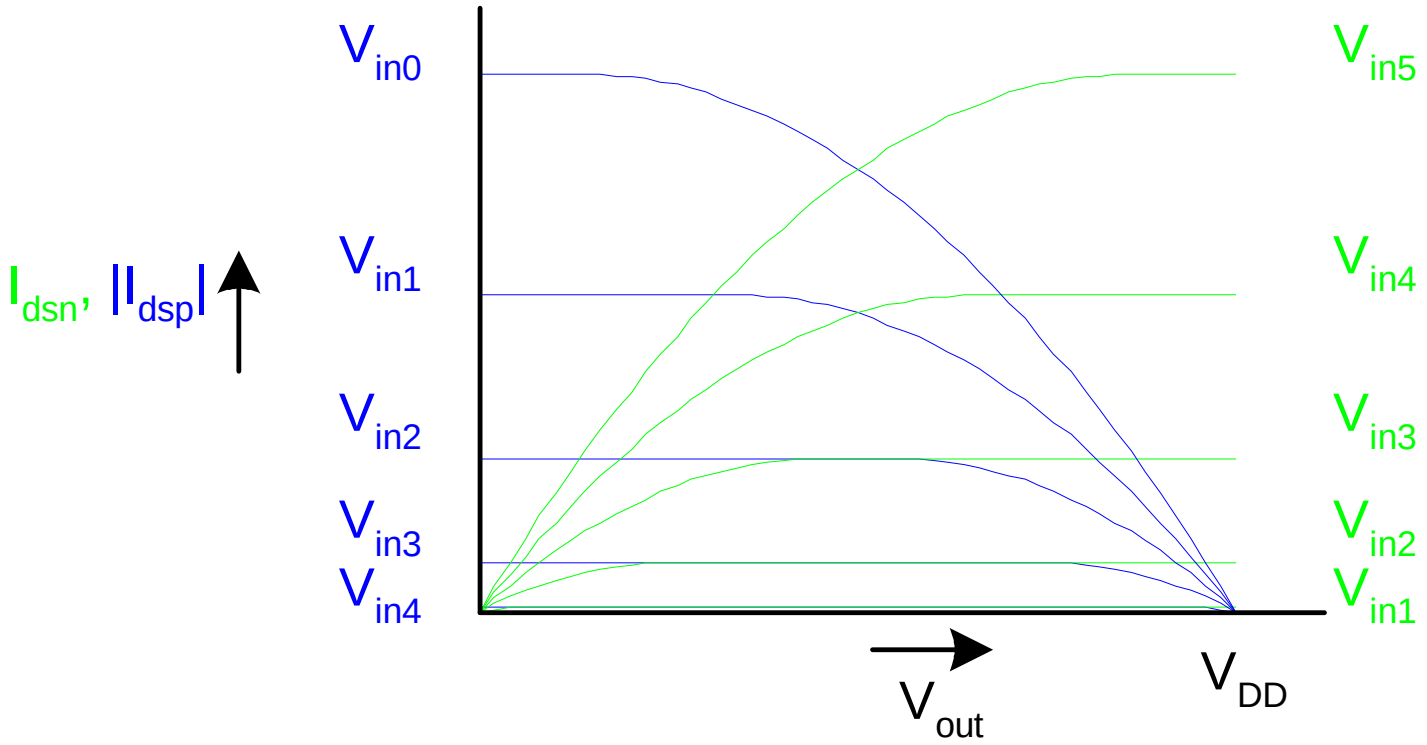


I-V Characteristics

- Make pMOS is wider than nMOS such that $\beta_n = \beta_p$

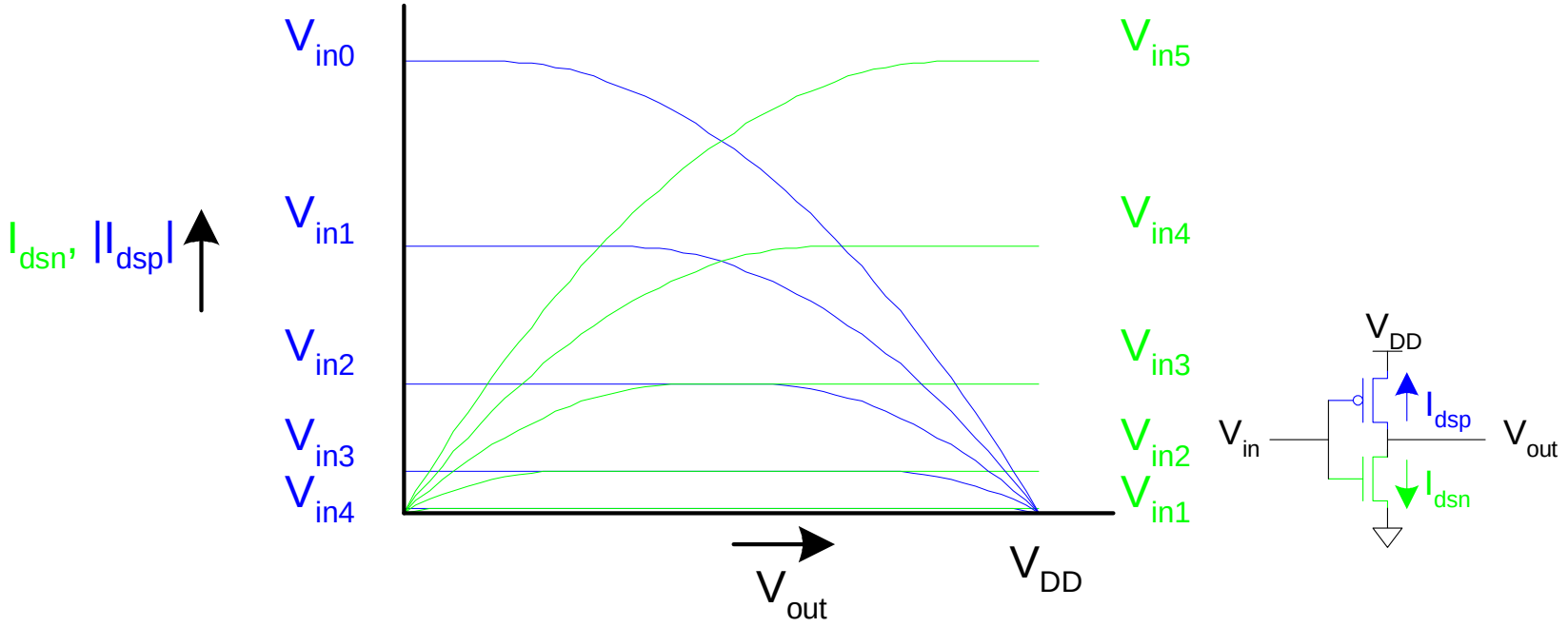


Current vs. V_{out}, V_{in}



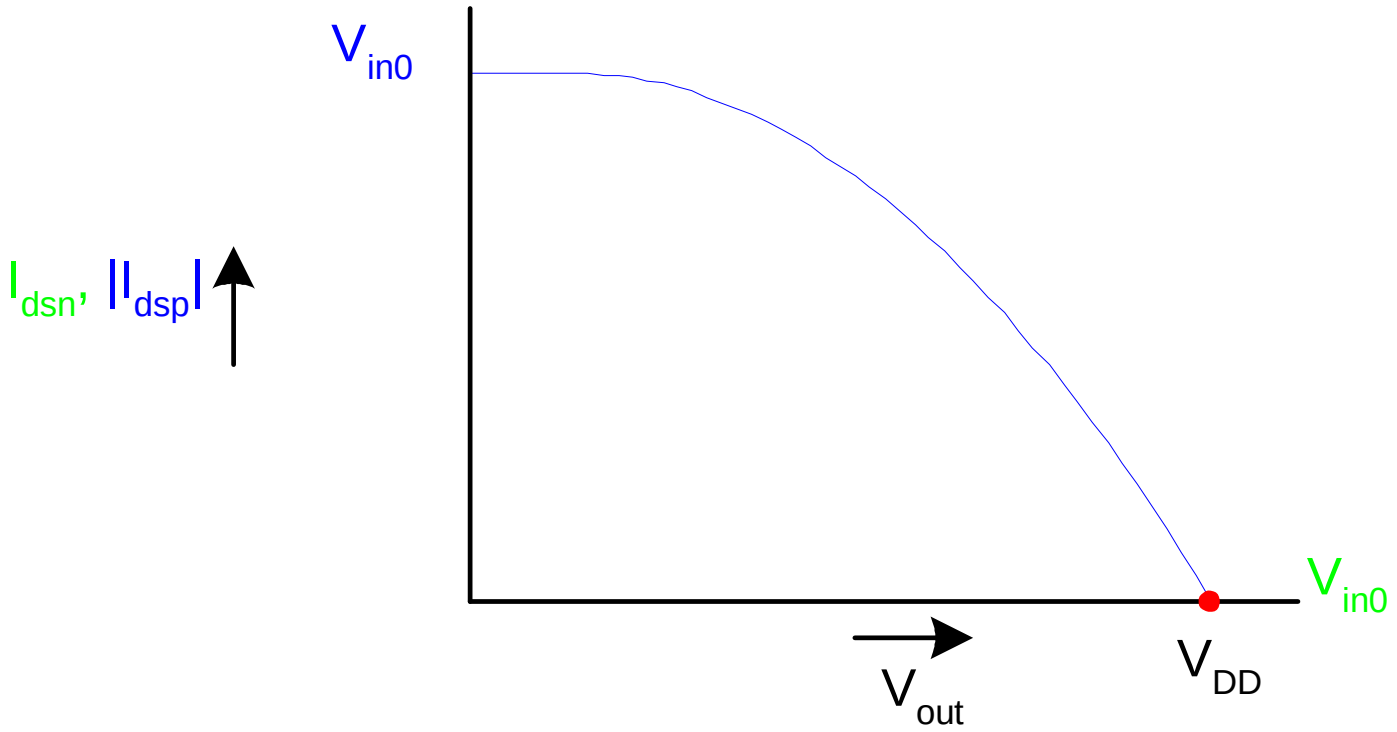
Load Line Analysis

- For a given V_{in}:
  - Plot I_{dsn}, I_{dsp} vs. V_{out}
  - V_{out} must be where |currents| are equal in



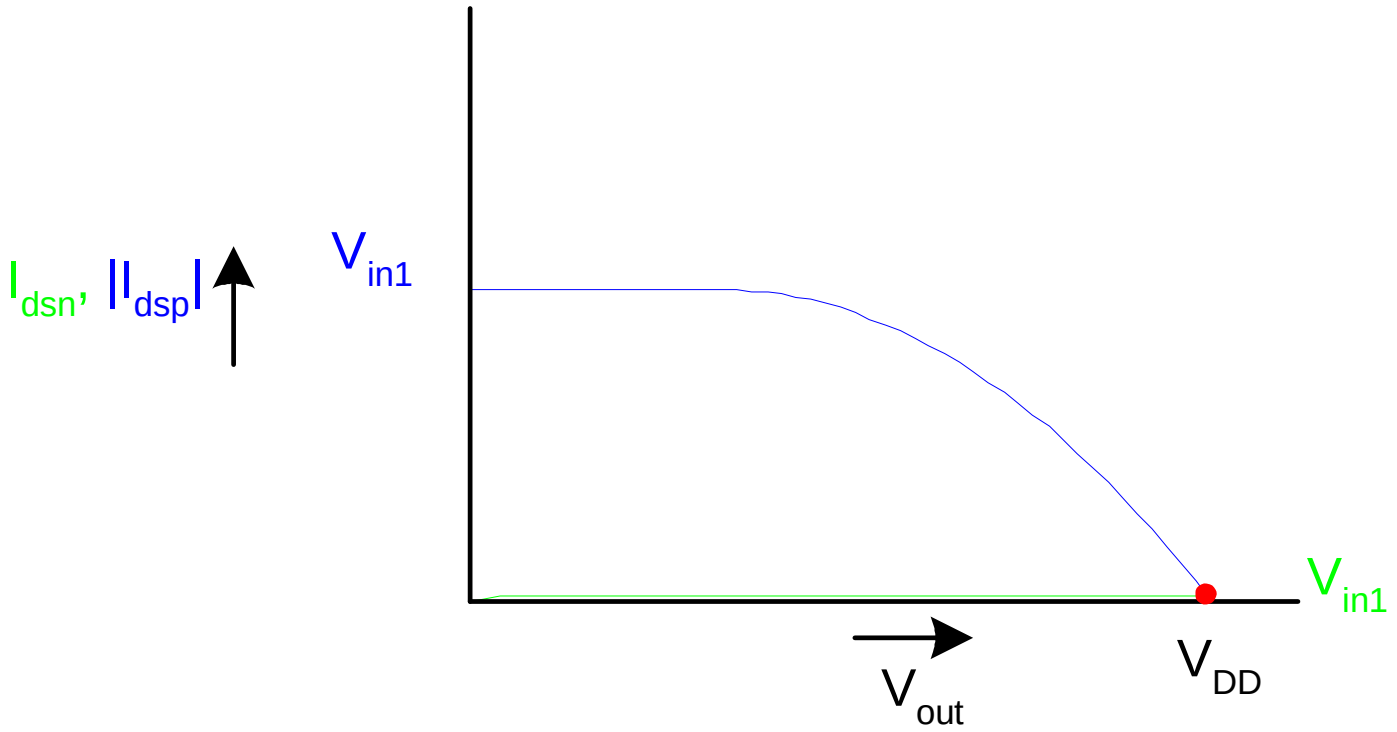
Load Line Analysis

- $V_{in} = 0$



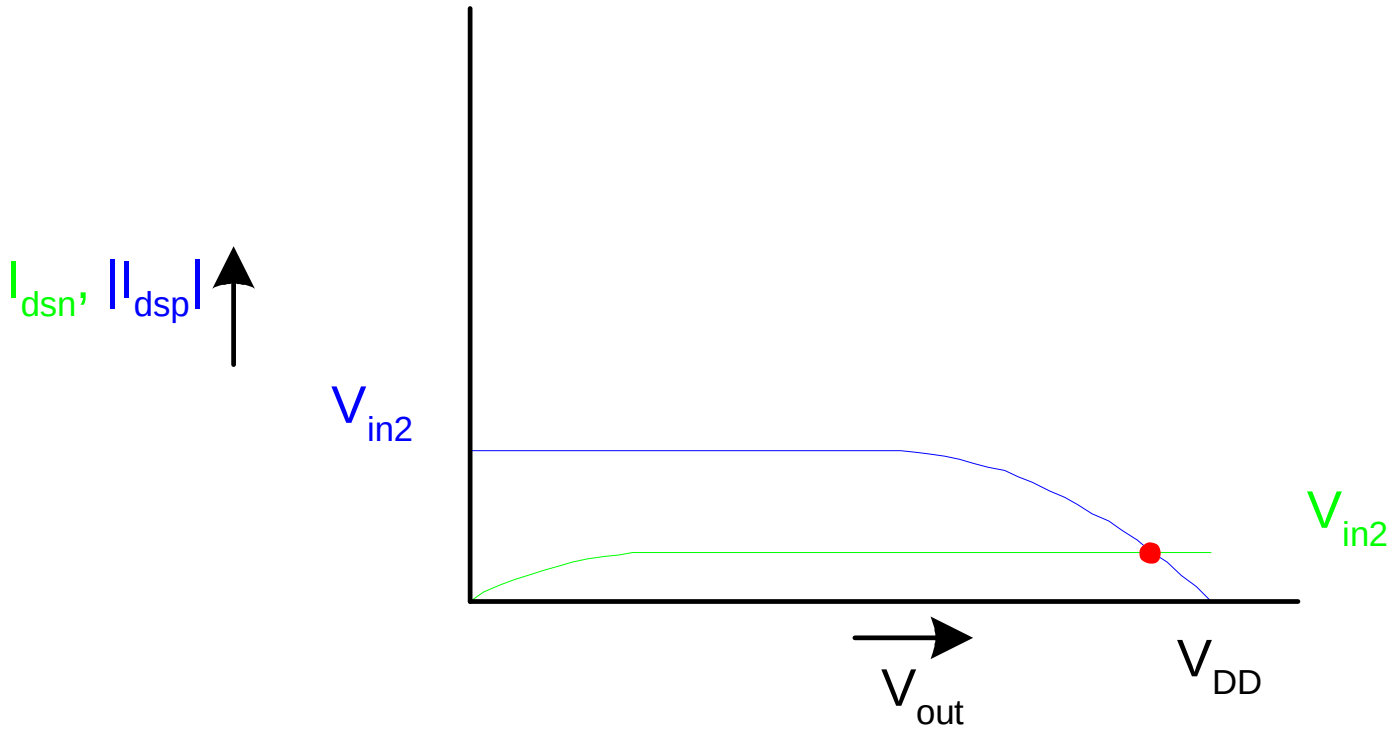
Load Line Analysis

- $V_{in} = 0.2V_{DD}$



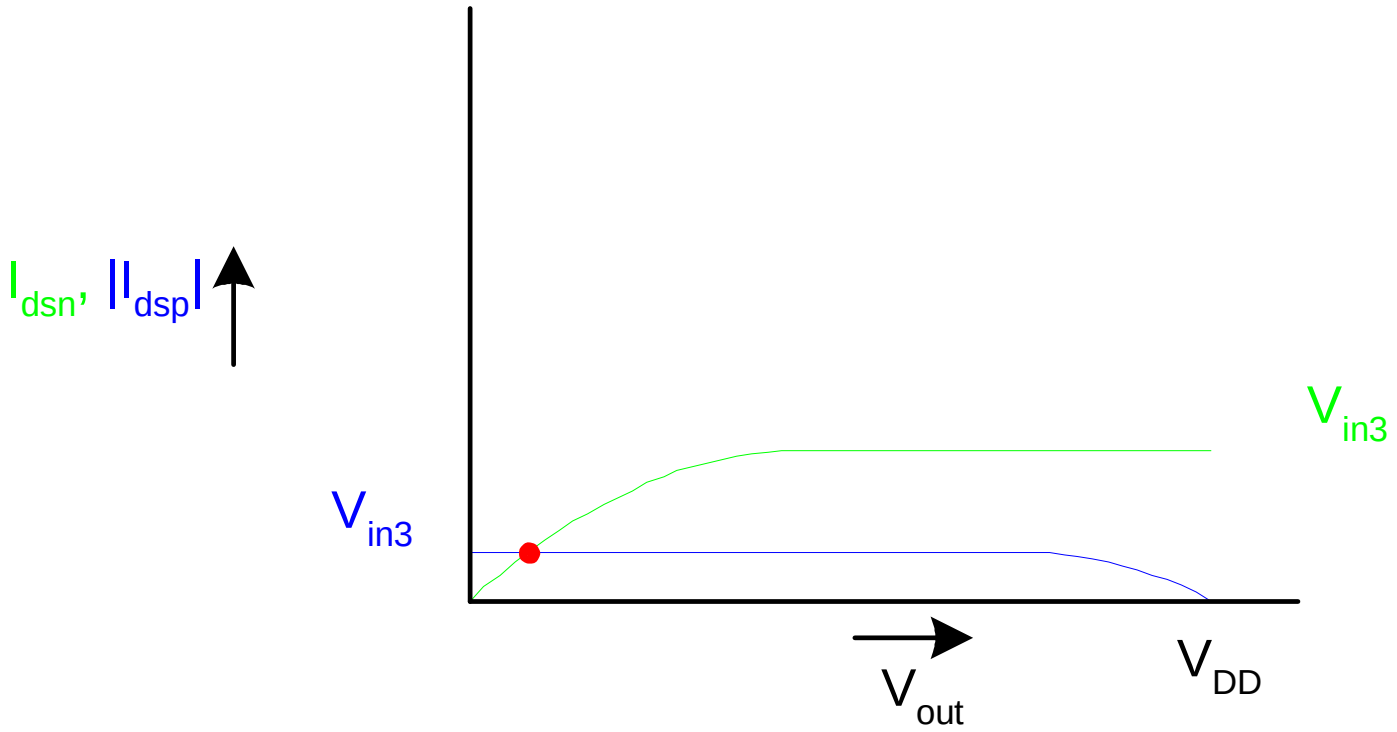
Load Line Analysis

- $V_{in} = 0.4V_{DD}$



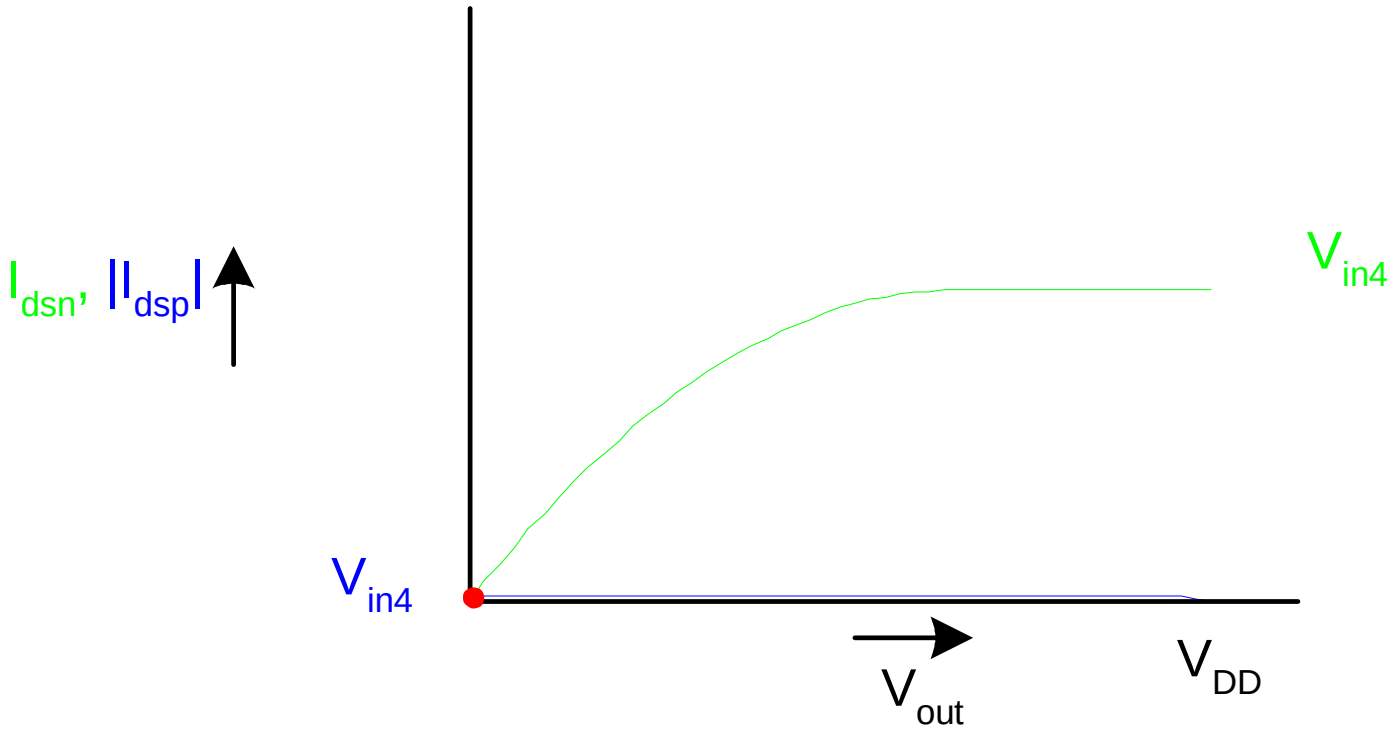
Load Line Analysis

- $V_{in} = 0.6V_{DD}$



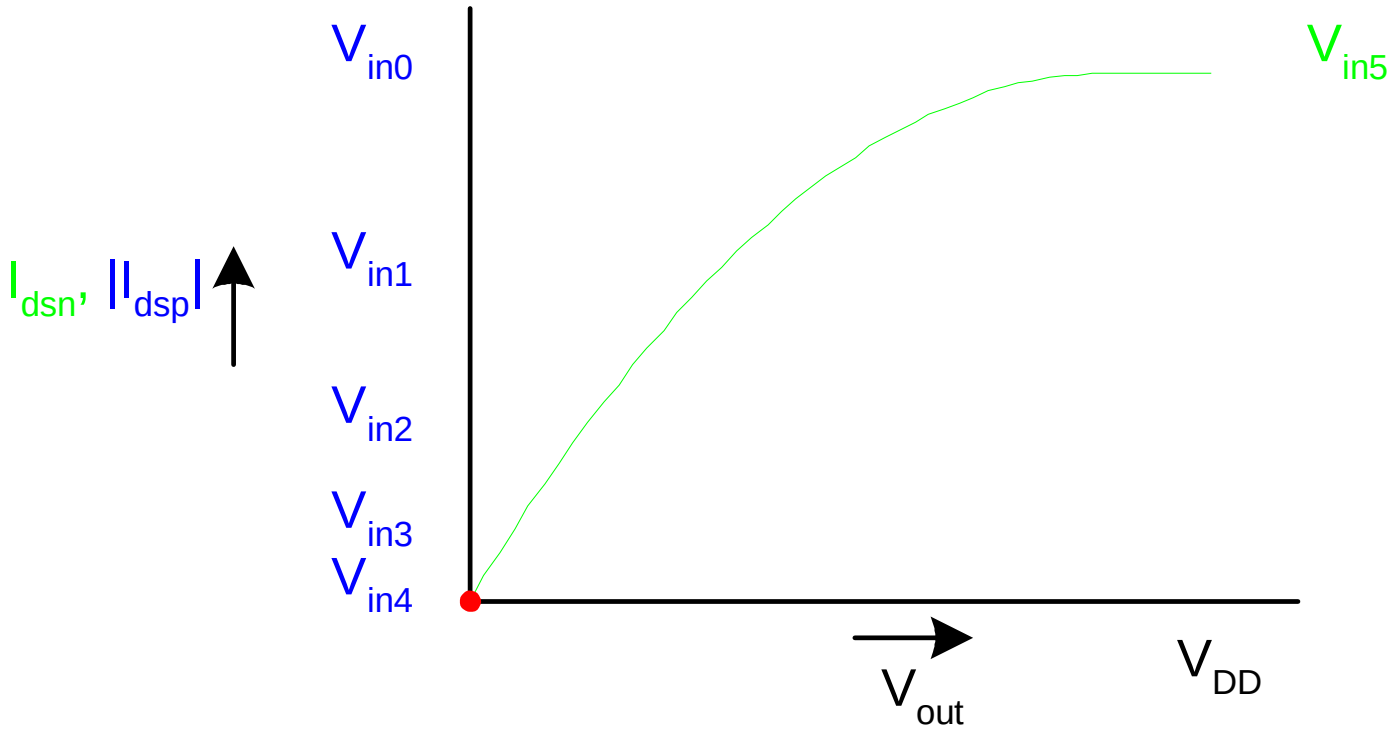
Load Line Analysis

- $V_{in} = 0.8V_{DD}$

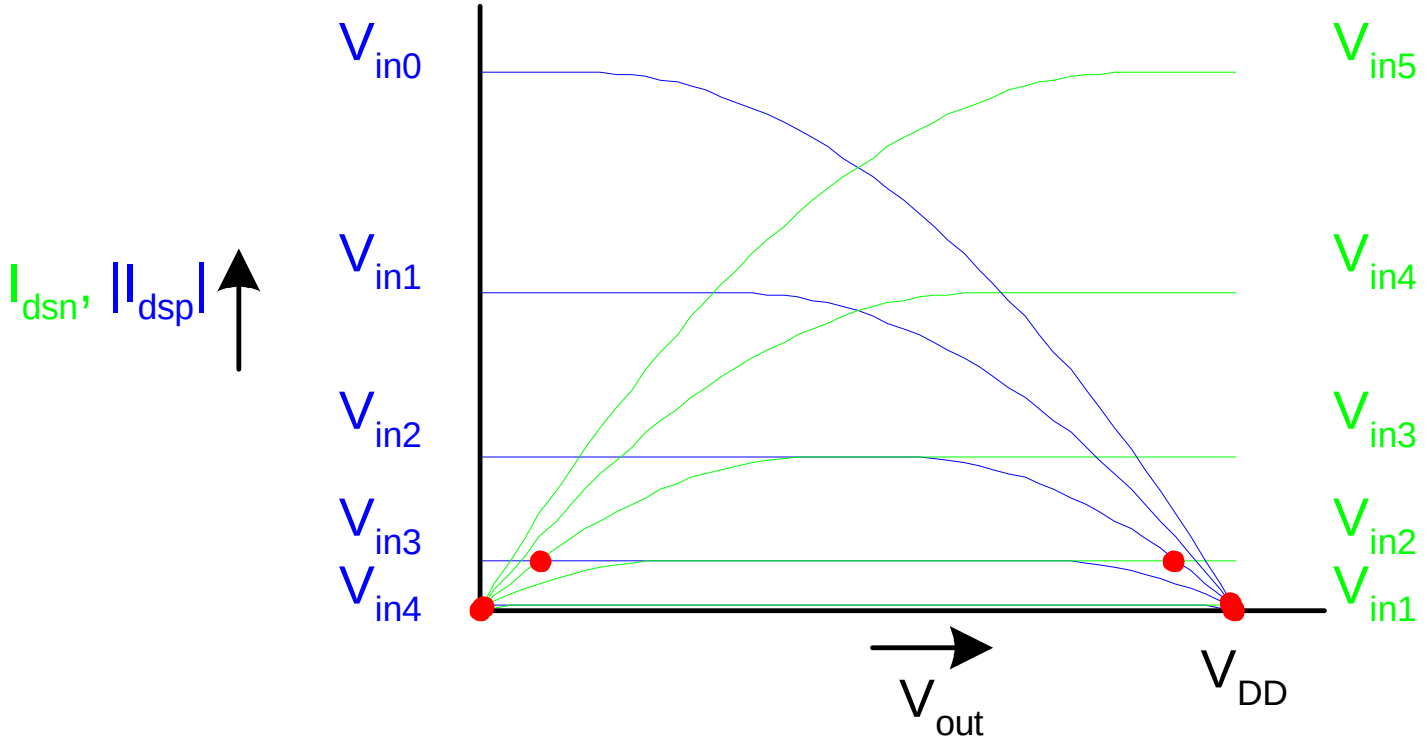


Load Line Analysis

- $V_{in} = V_{DD}$

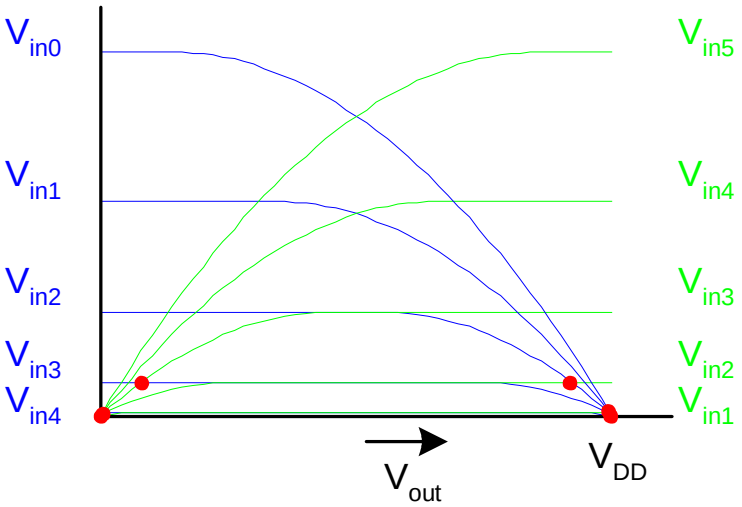


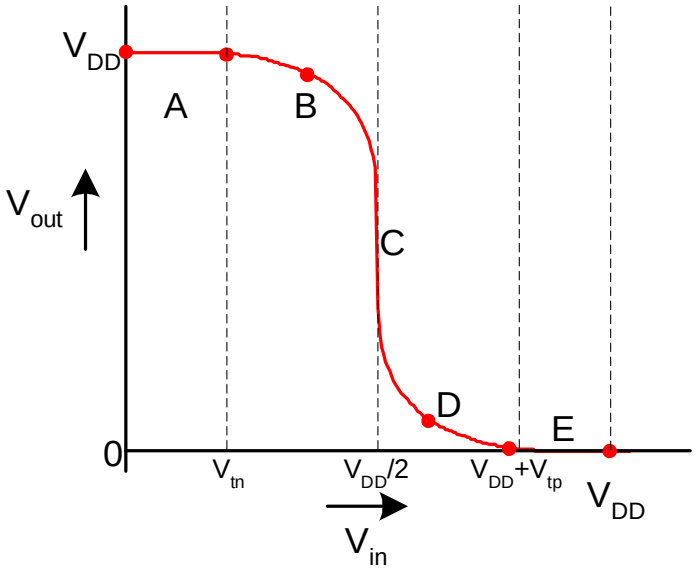
Load Line Summary



DC Transfer Curve

- Transcribe points onto V_{in} vs. V_{out} plot

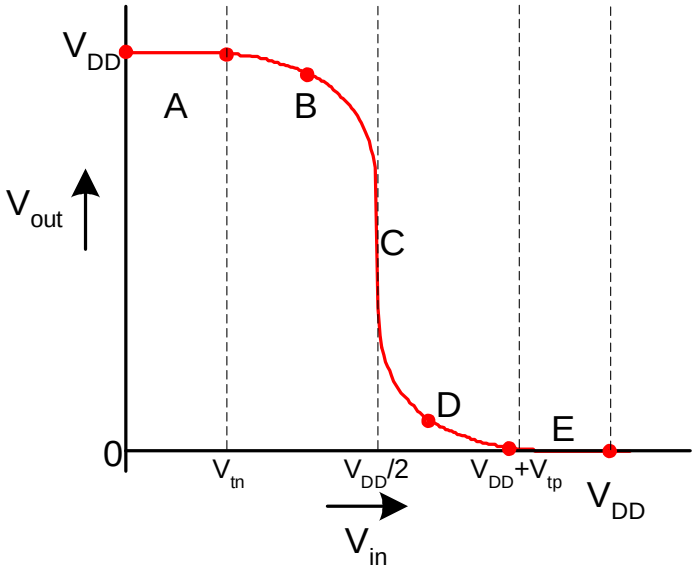




Operating Regions

- Revisit transistor operating regions

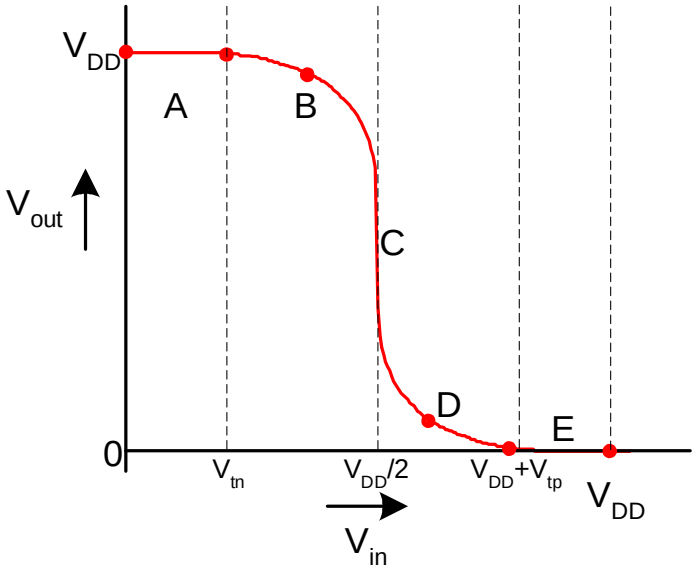
Region	nMOS	pMOS
A		
B		
C		
D		
E		



Operating Regions

- Revisit transistor operating regions

Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff



Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate
- Other gates: collapse into equivalent inverter