VLSI Design

N MOS Fabrication Process

- An Integrated Circuit (IC) is an electronic network fabricated in a single piece of a semiconductor material.
- The semiconductor surface is subjected to various processing steps in which impurities and other materials are added with specific geometrical patterns.

N-MOS Fabrication Process

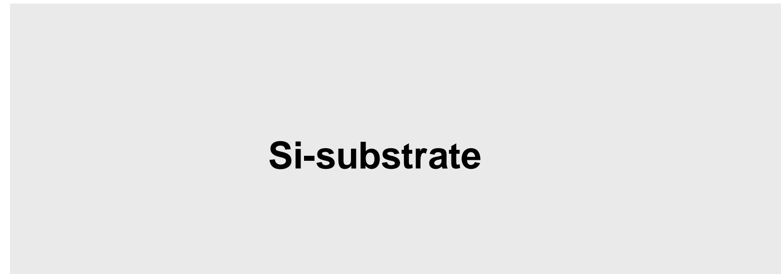


Fig. Pure Si single crystal

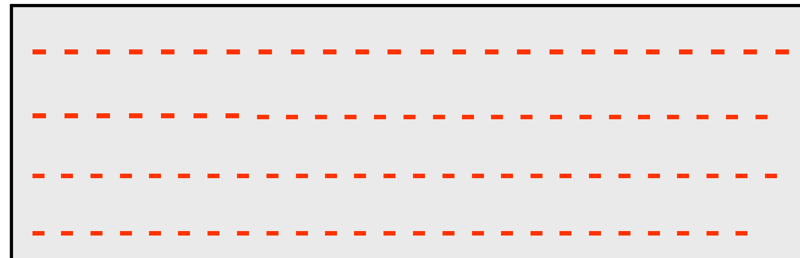


Fig. P-type impurity is lightly doped

N-MOS Fabrication Process

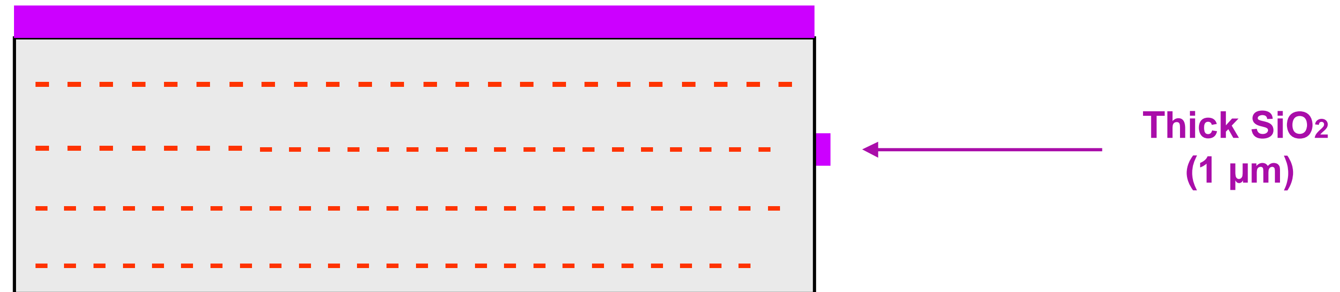


Fig. SiO_2 Deposited over si surface

Thick layer of Sio2 is grown over the surface of p substrate by the process of thermal oxidation. And the surface of substrate when exposed by oxygen is converted into SiO2 layer.

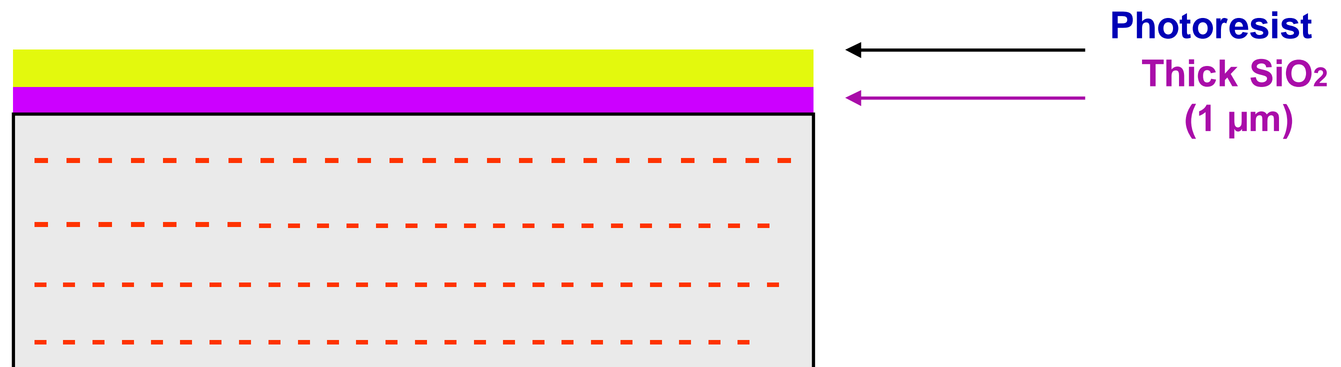


Fig. Photoresist is deposited over SiO_2 layer

Photoresist is basically an organic polymer having following properties.

- It is light sensitive. When this material is exposed by ultraviolet light, then the exposed area becomes soluble. But it is initially insoluble.
- Whole material can be exposed or its selective area can be exposed.
- For selective exposure, we can cover some of the area with a Mask.

- Mask:- It is having opaque(Resistant to the transmission of certain kinds of radiation, usually light) features and used for shielding the area on to which it is placed by UV rays.
- Area uncovered by mask gets exposed by UV rays and hence becomes soluble.

N-MOS Fabrication Process

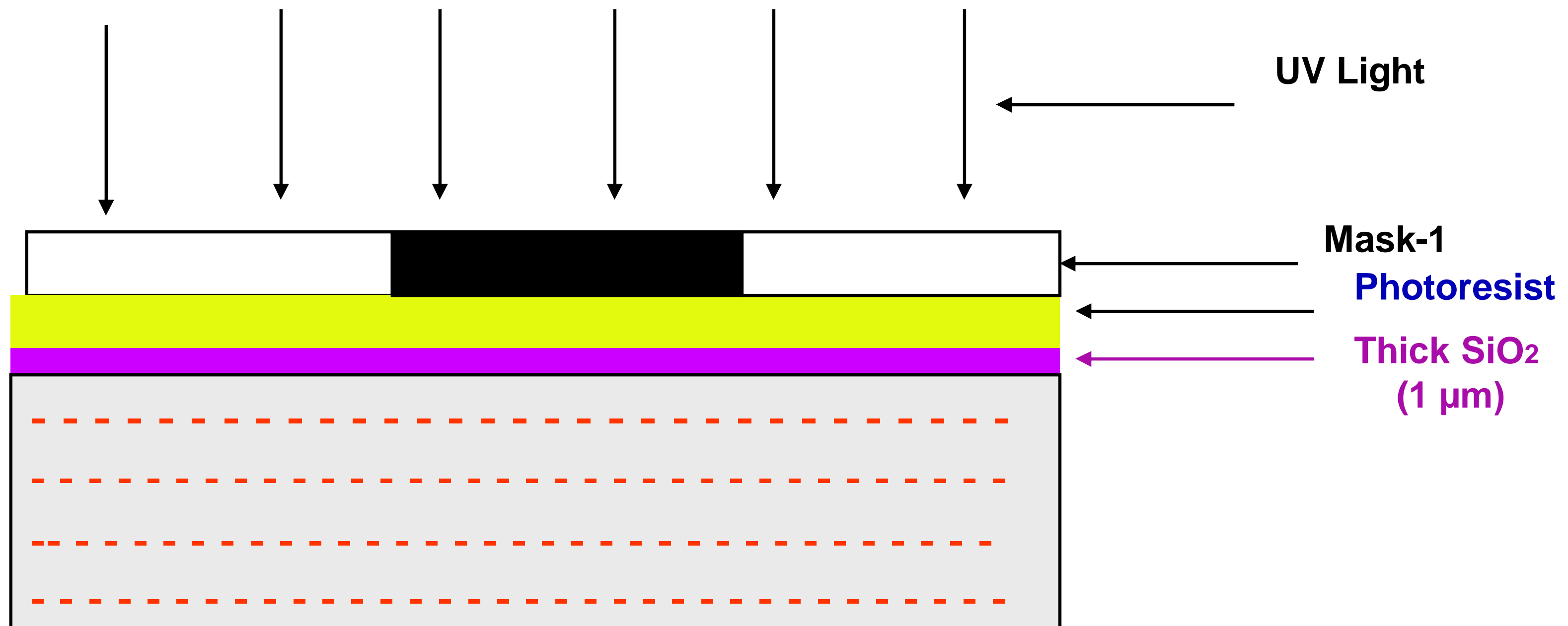


Fig. Photoresist layer is exposed to UV Light through a mask .Exposed photoresist becomes soluble.

N-MOS Fabrication Process

Sio2 regions which are not covered by hardened photoresist can be etched away.

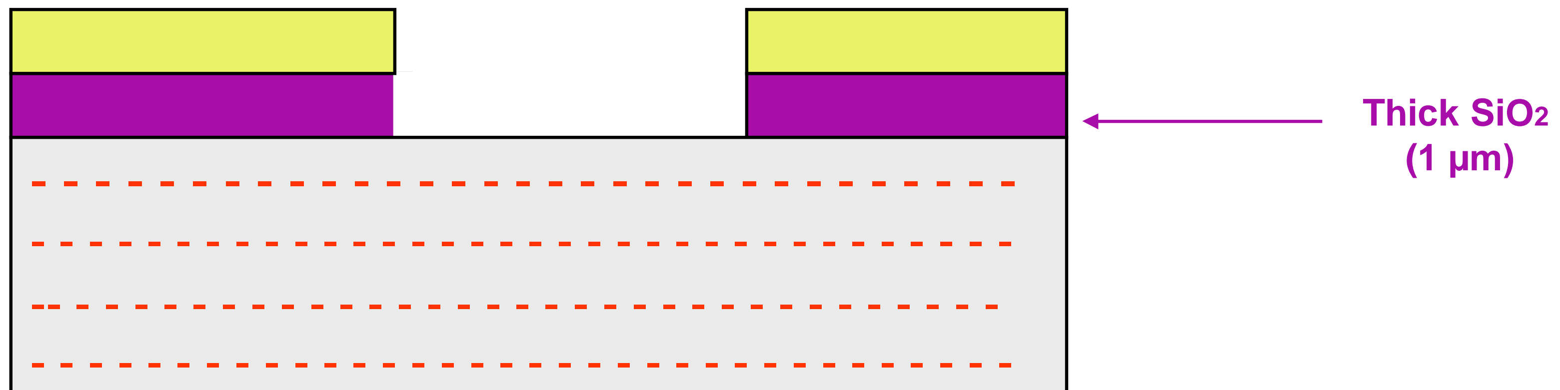


Fig. Etching [HF acid is used] will remove SiO2 layer

N-MOS Fabrication Process

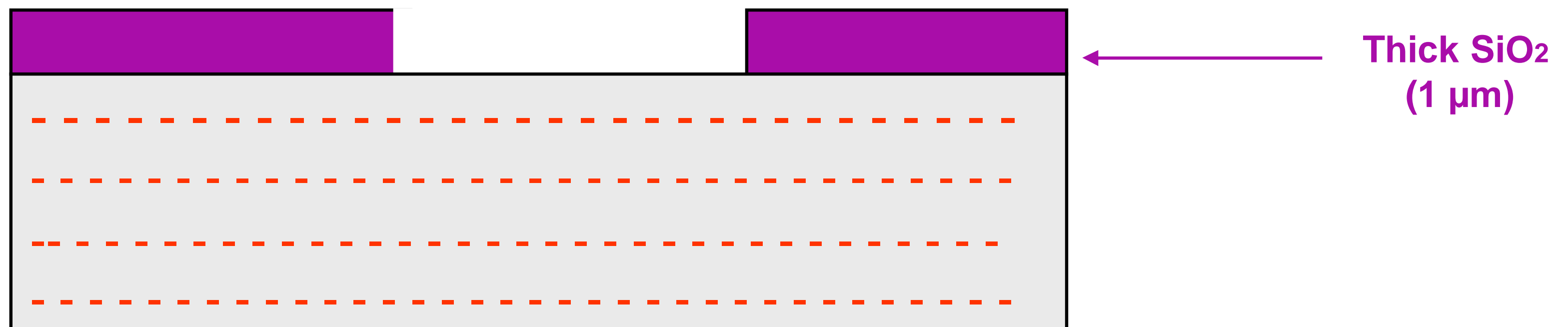


Fig. Photoresist is also etched away [using H2SO4].Etched Si substrate is shown here.

- Thus we have a single pattern transferred on Sio2 surface. This type of transferring a pattern to Sio2 layer in Si substrate is known as lithography.

N-MOS Fabrication Process

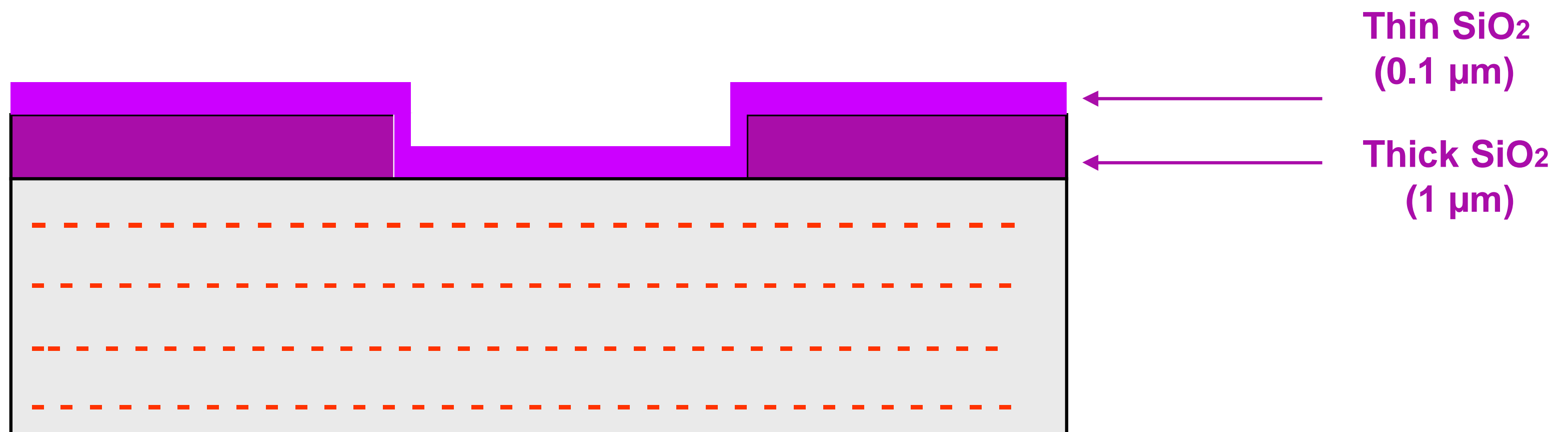


Fig. (8) A thin layer of SiO_2 grown over the entire chip surface

N-MOS Fabrication Process

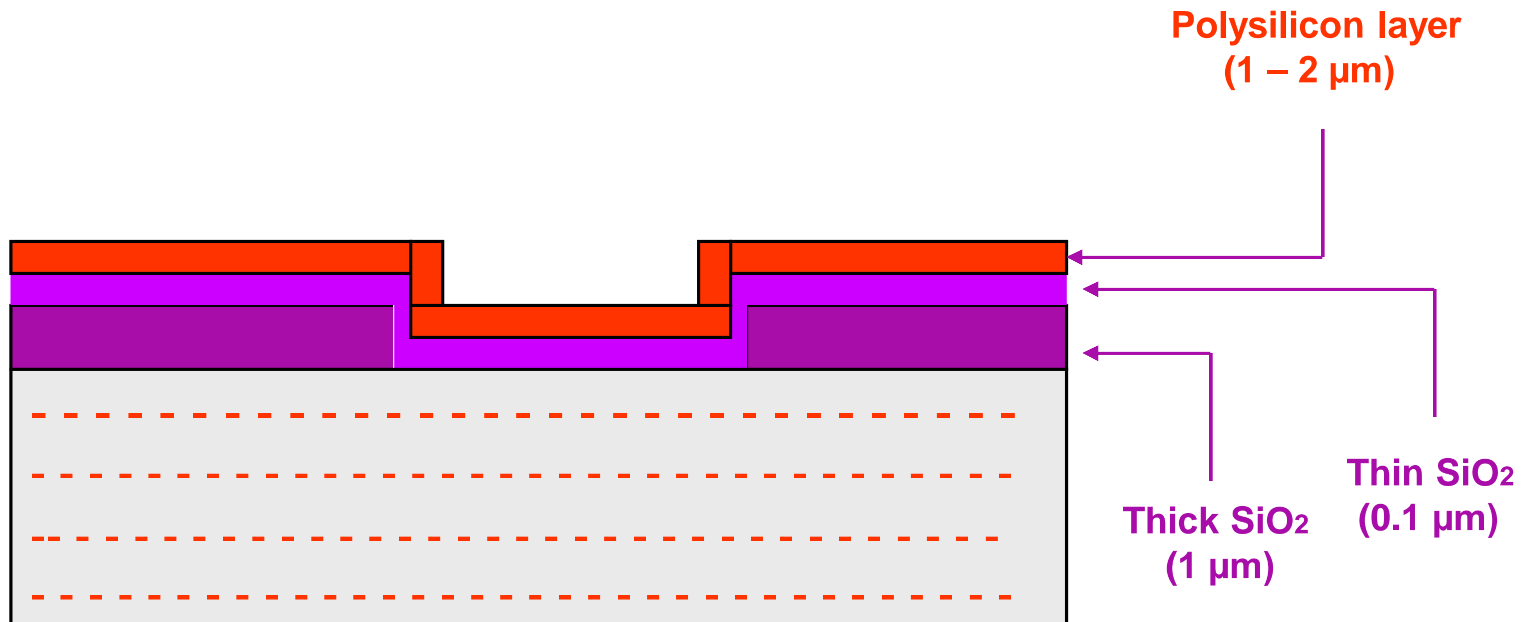


Fig. (9) A thin layer of polysilicon is grown over the entire chip surface to form GATE

N-MOS Fabrication Process

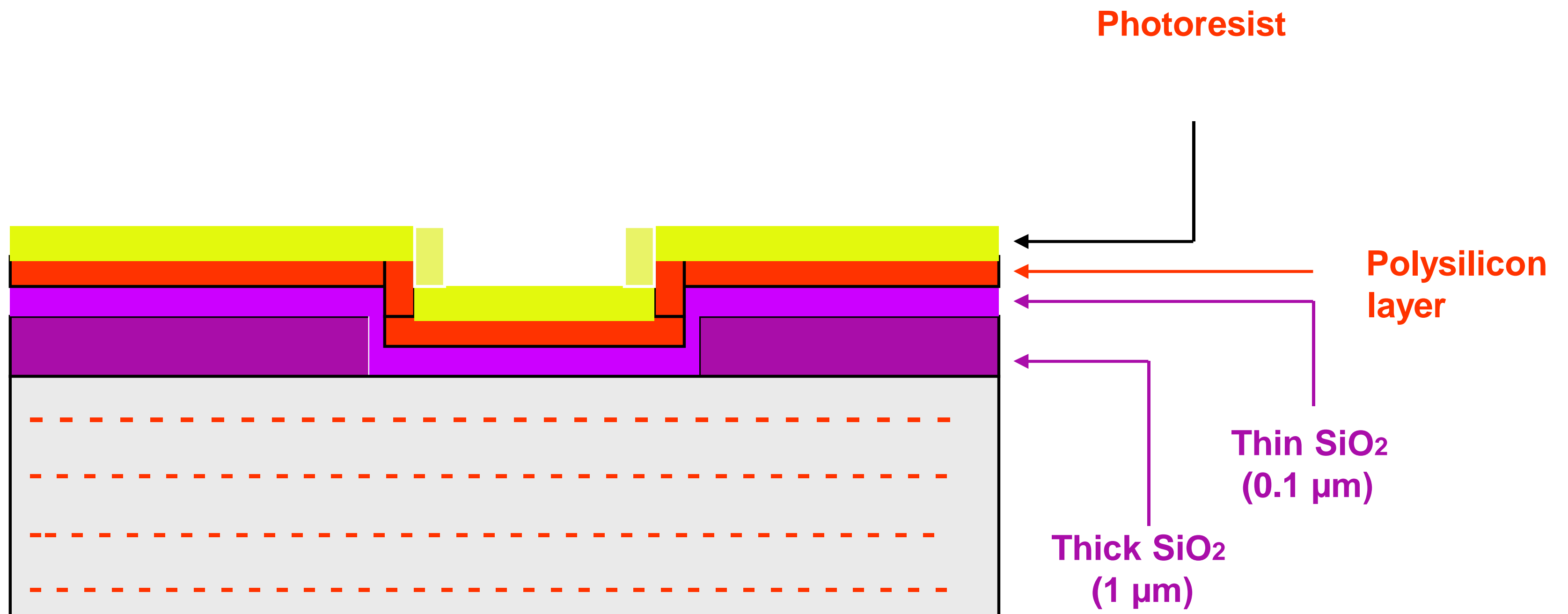
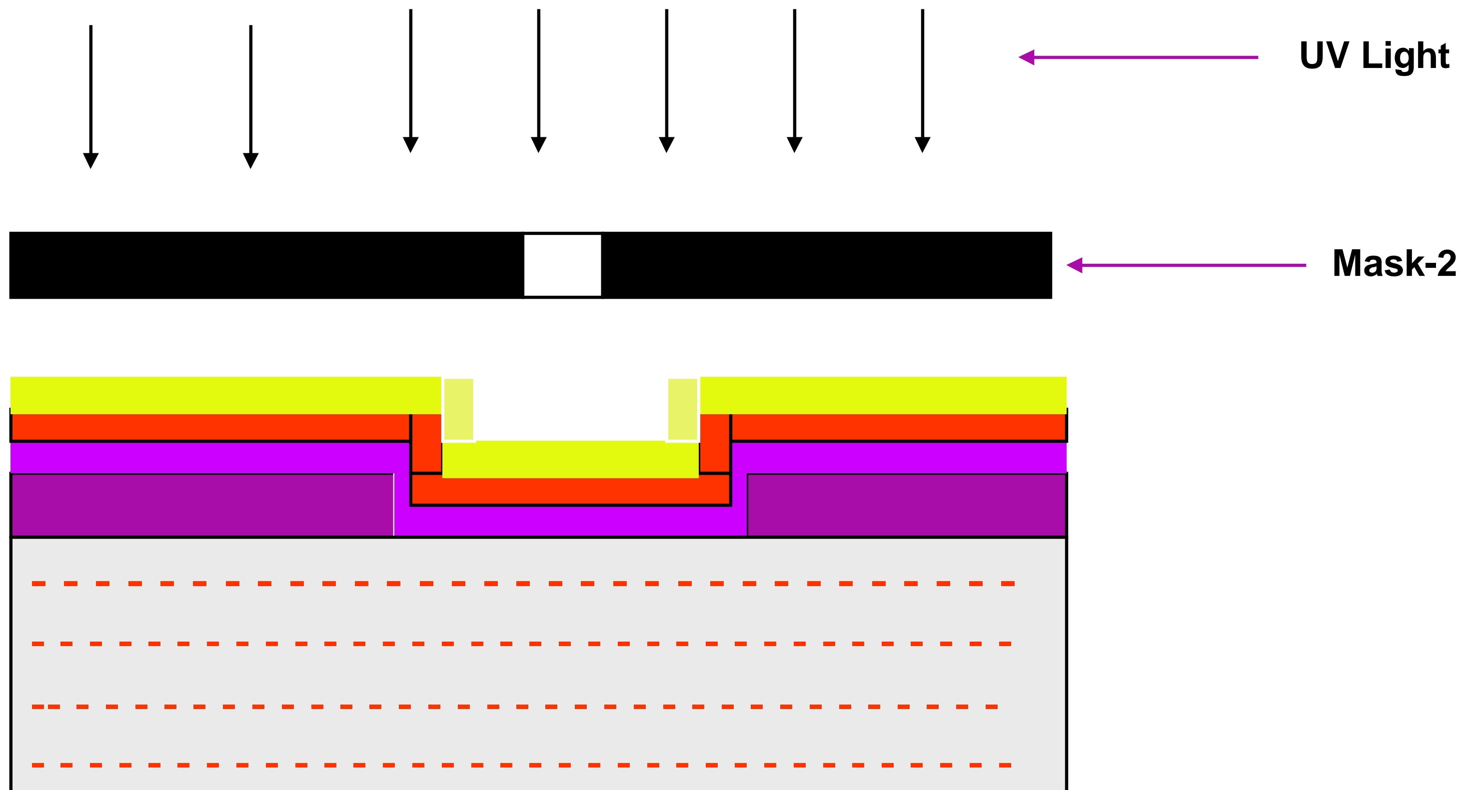


Fig. (10) A layer of photoresist is grown over polysilicon layer

- By the process of lithography,we have to pattern polysilicon in such a way that we just have polysilicon in the region in which we have to mount the gate. Patterening is again done by masking process and exposure of UV rays for selective area.

N-MOS Fabrication Process



Mask-2 is used to deposit Polysilicon to form gate.

Fig. (11) Photoresist is exposed to UV Light

N-MOS Fabrication Process

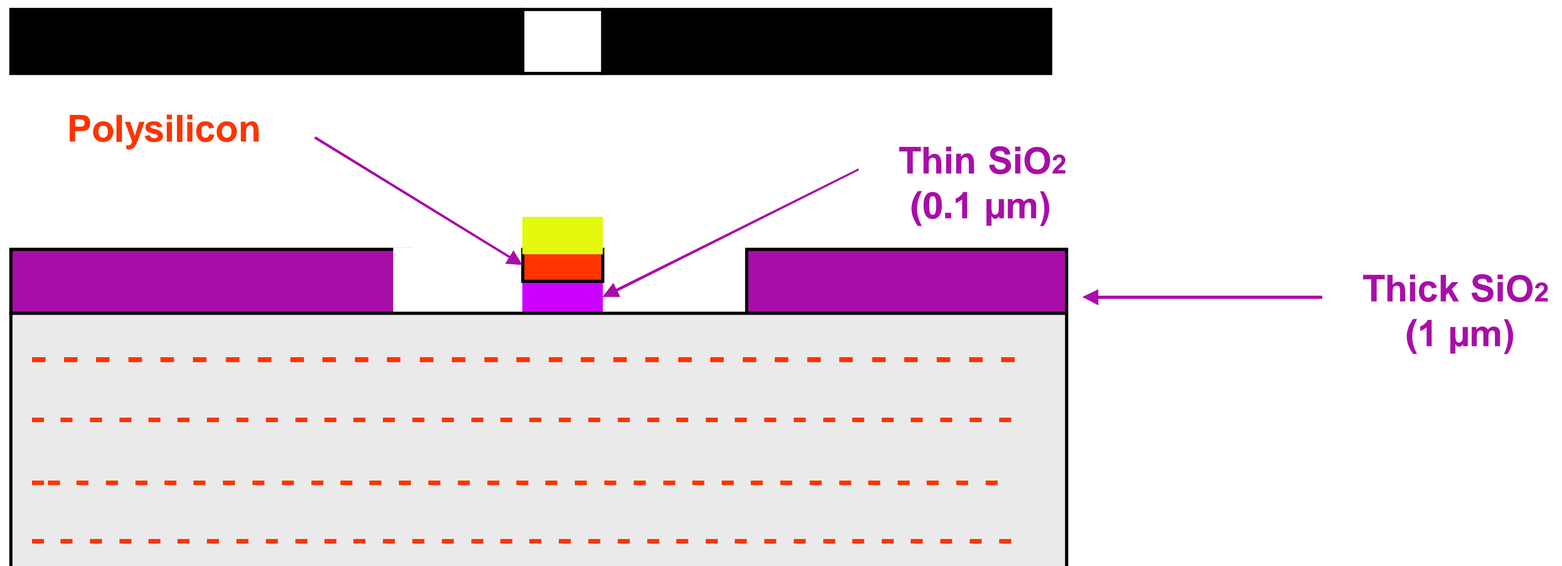


Fig. (12) Etching will remove that portion of Thin SiO2 which is not exposed to UV light

N-MOS Fabrication Process

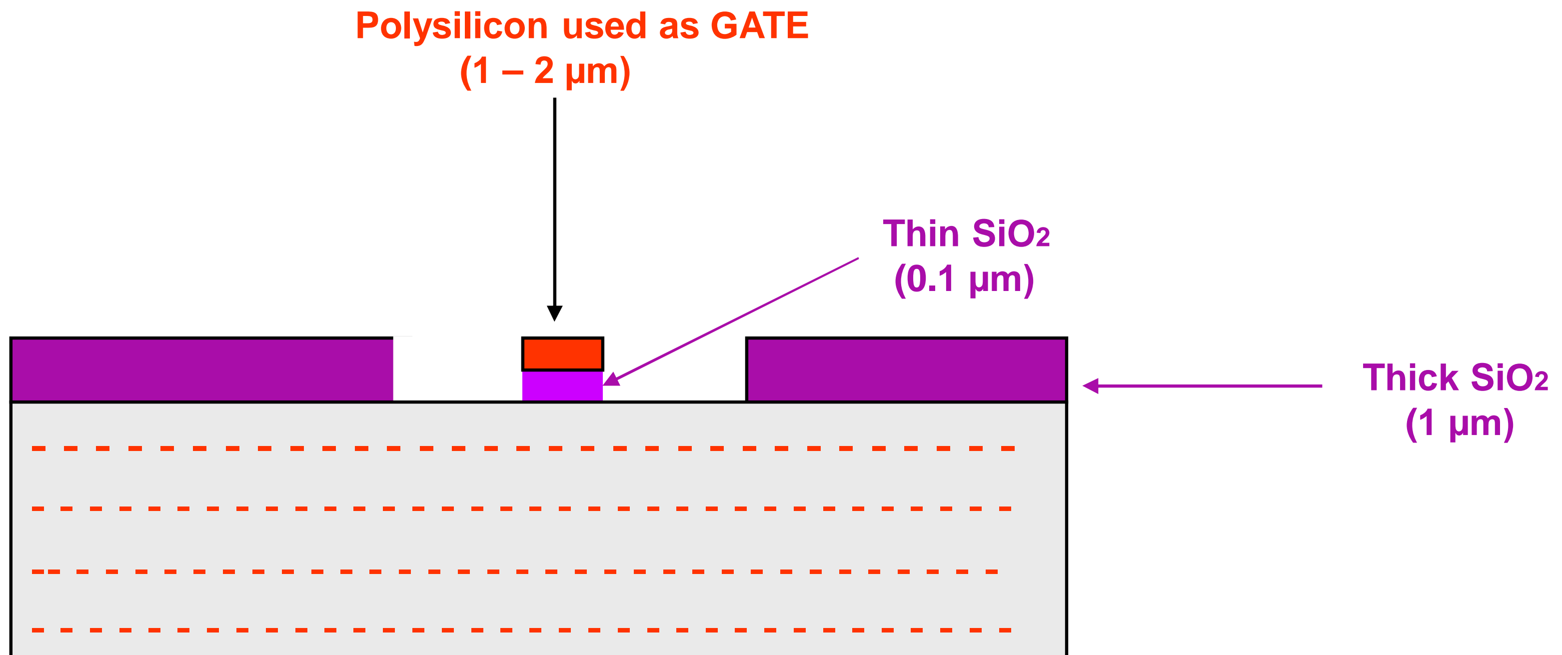


Fig. (13) Polymerised photoresist is also stripped away

N-MOS Fabrication Process

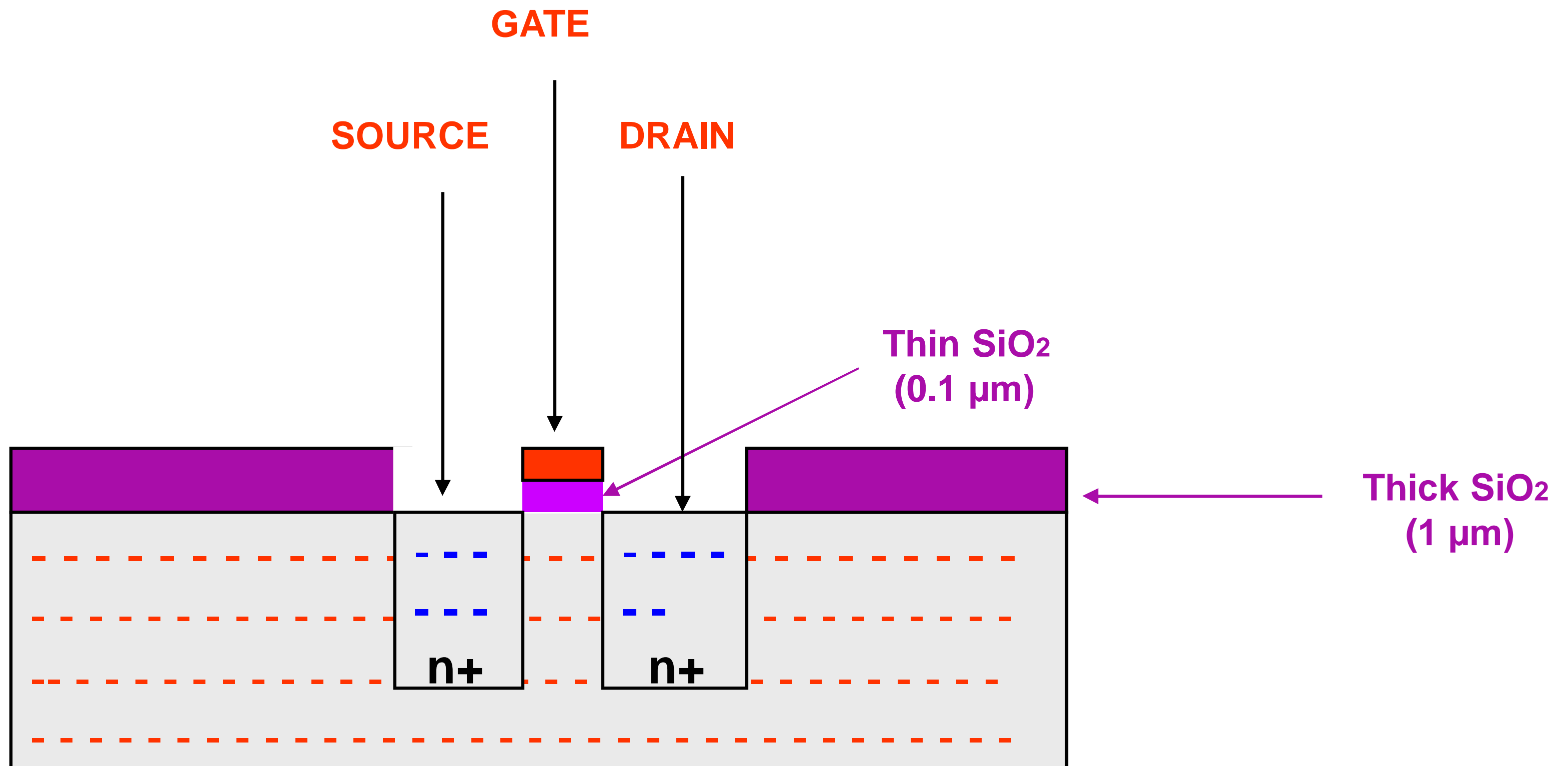


Fig. (14) n^+ Doping to form SOURCE and DRAIN by using diffusion

N-MOS Fabrication Process

Step - Metallization

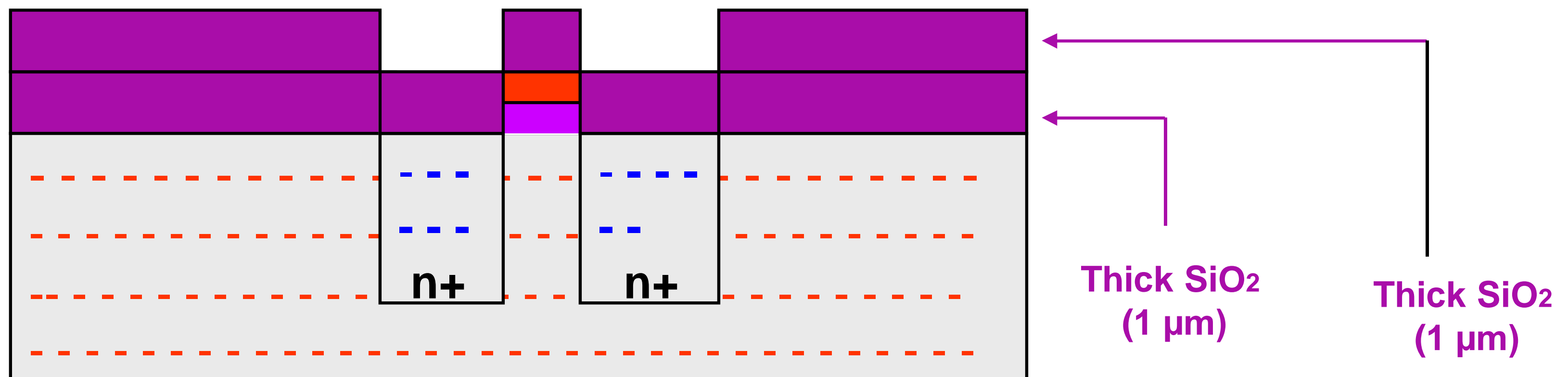


Fig. (15) A thick layer of SiO2 (1 μm) is again grown.

N-MOS Fabrication Process

Step - Metallization

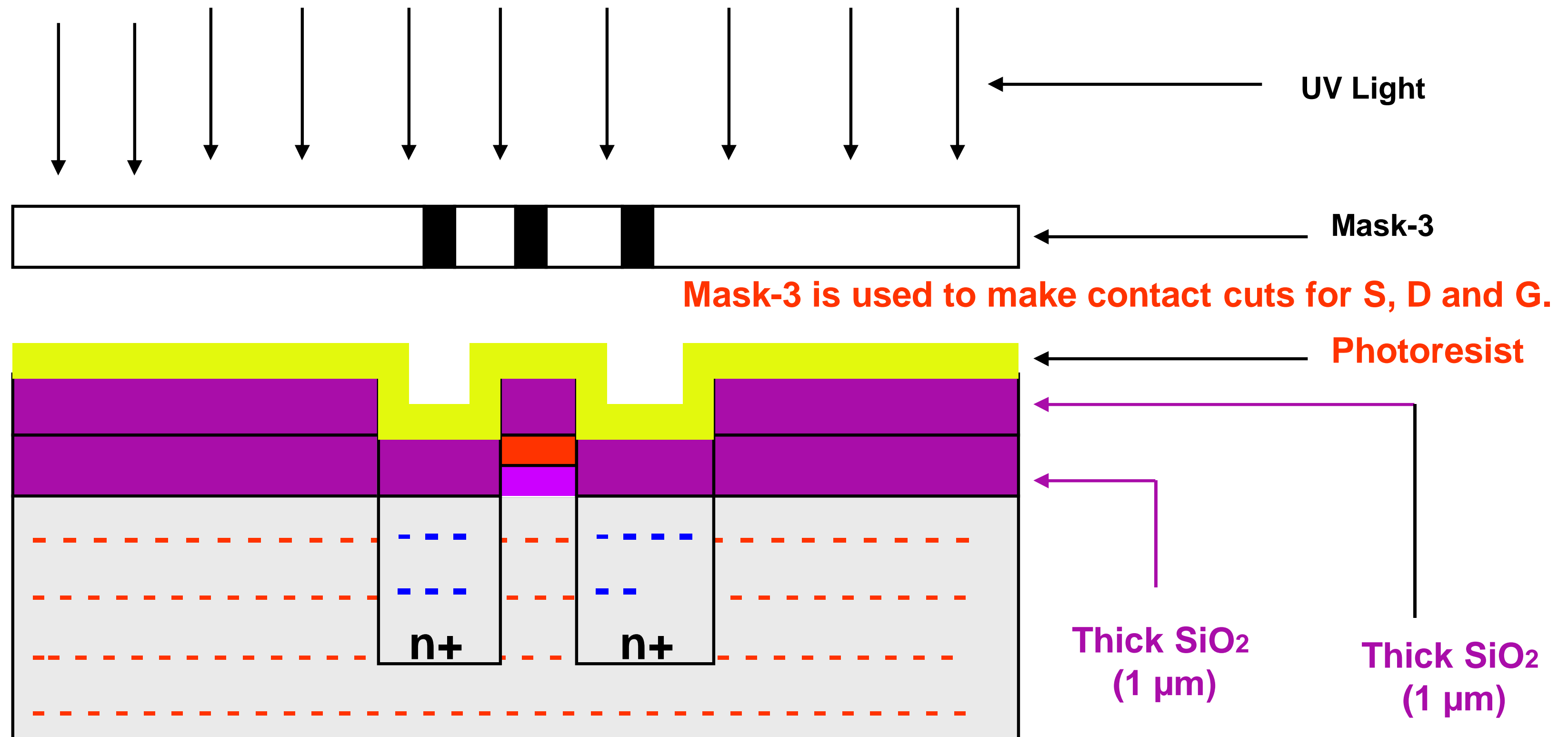


Fig. (16) Photoresist is grown over thick SiO_2. Selected areas of the poly GATE and SOURCE and DRAIN are exposed where contact cuts are to be made

N-MOS Fabrication Process

Step - Metallization

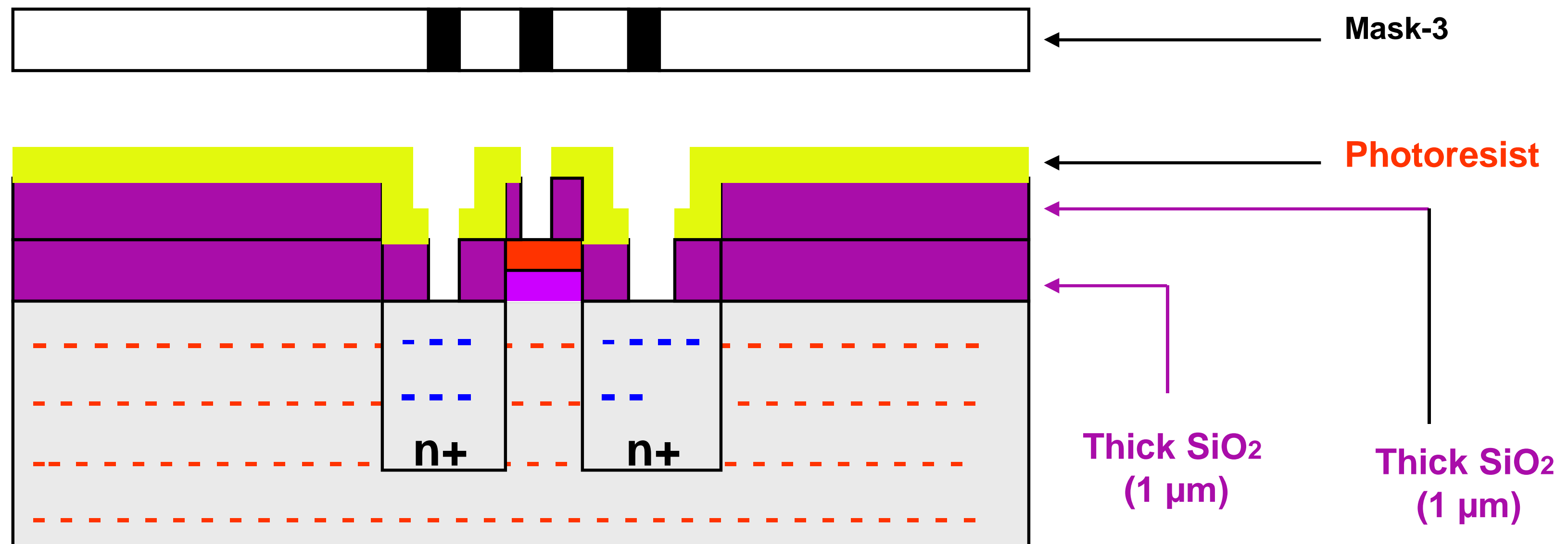


Fig. (17) The region of photoresist which is not exposed by UV light will become soft. This effective photoresist and SiO_2 below it are etched away.

N-MOS Fabrication Process

Step - Metallization

Mask-3

Photoresist

n+

n+

Thick SiO_2 (1 μm)

Thick SiO_2 (1 μm)

Fig. (18) The contact cuts are formed for S, D and G (hardened photoresist is stripped away).

N-MOS Fabrication Process
Step - Metallization

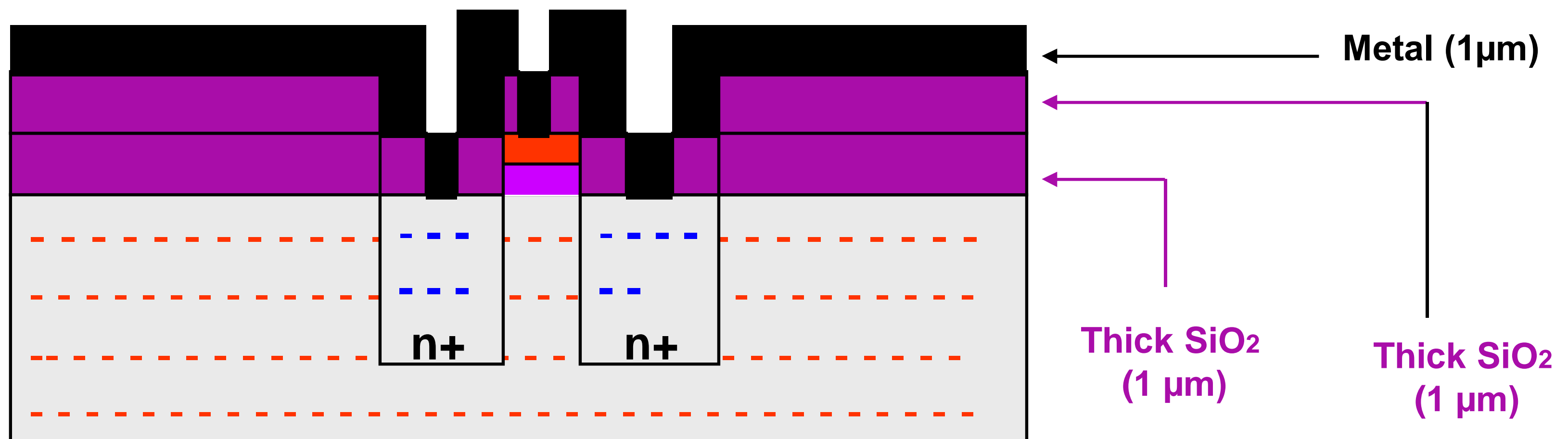


Fig. (19) Metal (aluminium) is deposited over the surface of whole chip (1 µm thickness).

N-MOS Fabrication Process

Step - Metallization

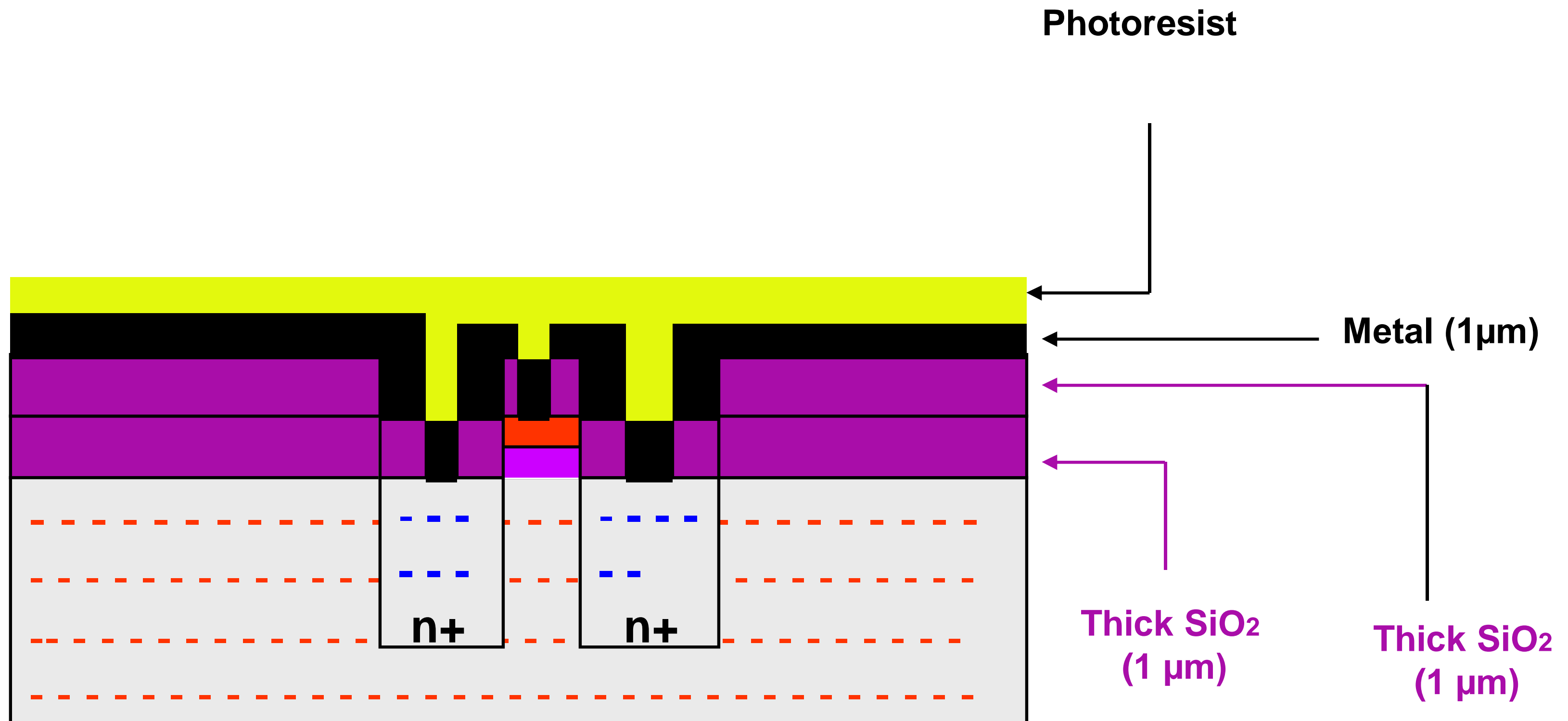
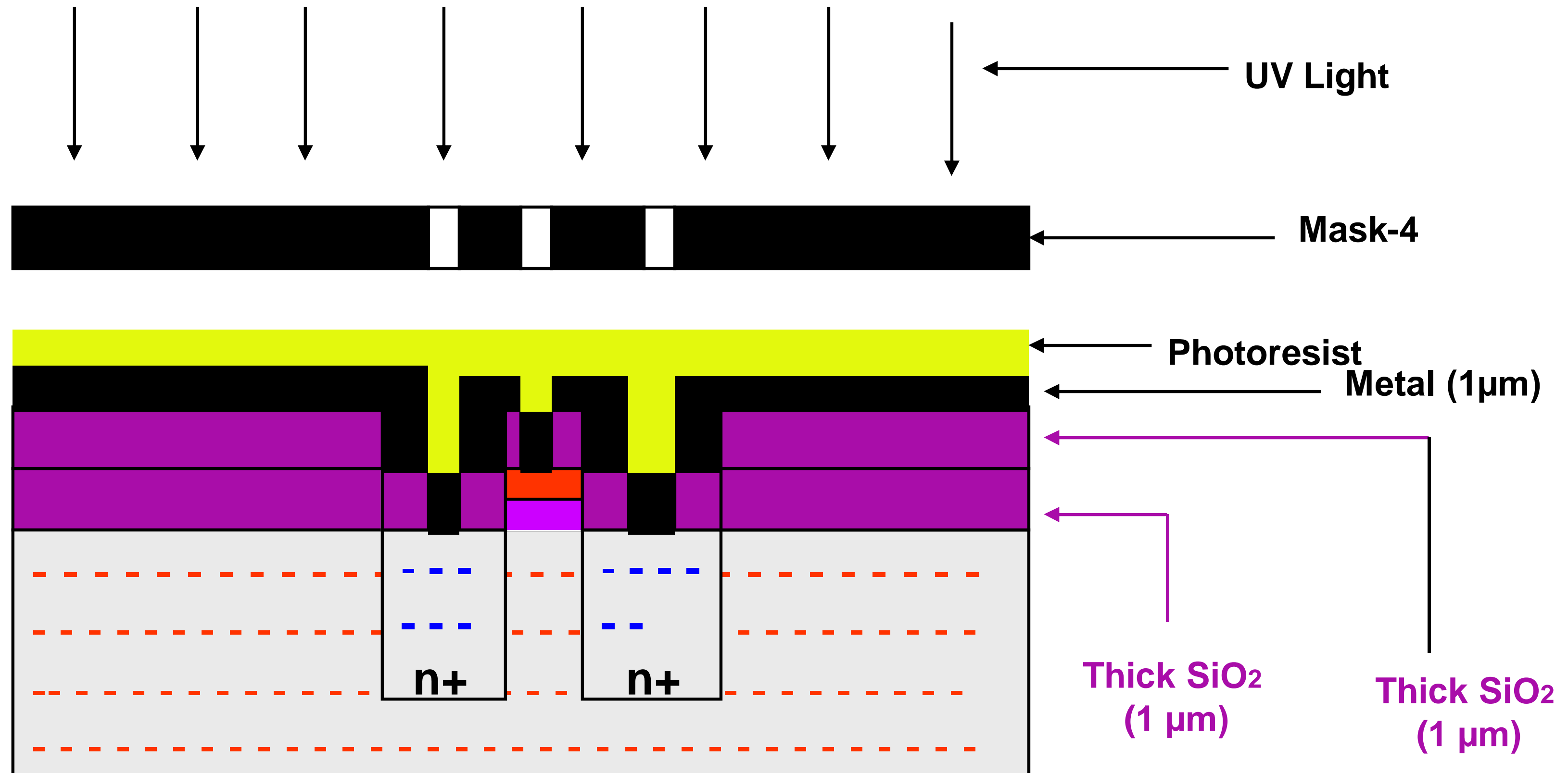


Fig. (20) Photoresist is deposited over the metal.

N-MOS Fabrication Process

Step - Metallization



Mask-4 is used to deposit metal in contact cuts of S, D and G.

Fig. (21) UV Light is passed through Mask-4 (with a aim of removing all metal other than metal in contact-cuts).

N-MOS Fabrication Process

Step - Metallization

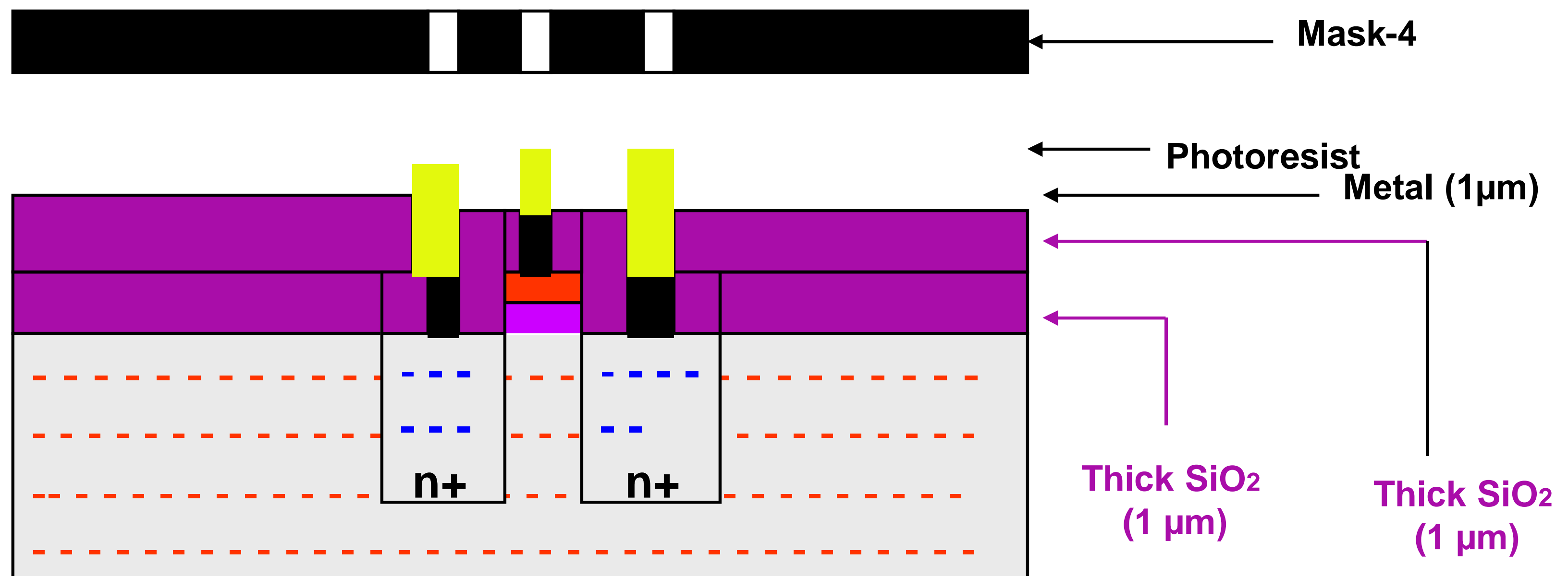


Fig. (22) Photoresist and metal which is not exposed to UV light are etched away.

N-MOS Fabrication Process

Step - Metallization

SOURCE

GATE

DRAIN

n+

n+

Fig. (23) Final n-MOS Transistor