VLSI DESIGN

Ideal MOSFET Current–Voltage Characteristics—NMOS Device

The **threshold voltage of the n-channel MOSFET, denoted as *VTn, is defined as the*** applied gate voltage needed to create an inversion charge. In simple terms, we can think of the threshold voltage as the gate voltage required to “turn on” the transistor. For the n-channel enhancement-mode MOSFET, the threshold voltage is positive because a positive gate voltage is required to create the inversion charge.

If the gate voltage is less than the threshold voltage, the current in the device is essentially zero. If the gate voltage is greater than the threshold voltage, a drain-to-source current is generated as the drain-to-source voltage is applied.

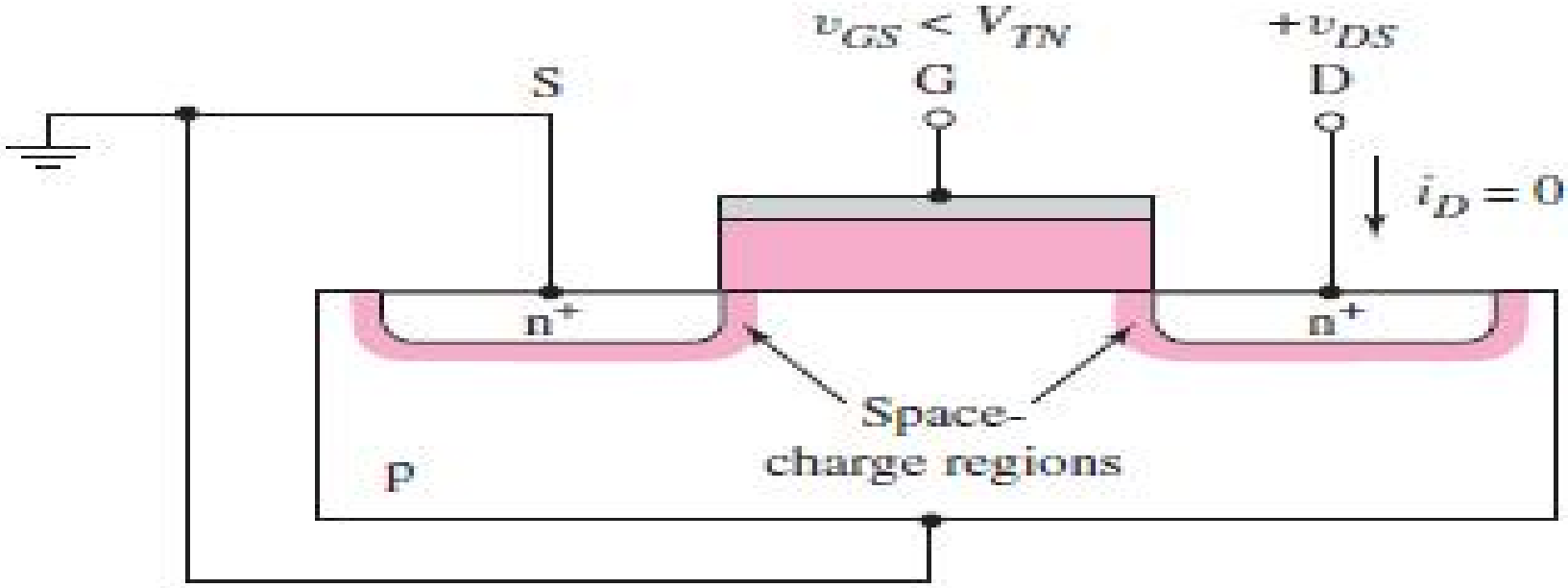

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Figure shows an n-channel enhancement-mode MOSFET with the source and substrate terminals connected to ground. The gate-to-source voltage is less than the threshold voltage, and there is a small drain-to-source voltage. With this bias configuration, there is no electron inversion layer, the drain-to-substrate pn junction is reverse biased, and the drain current is zero.

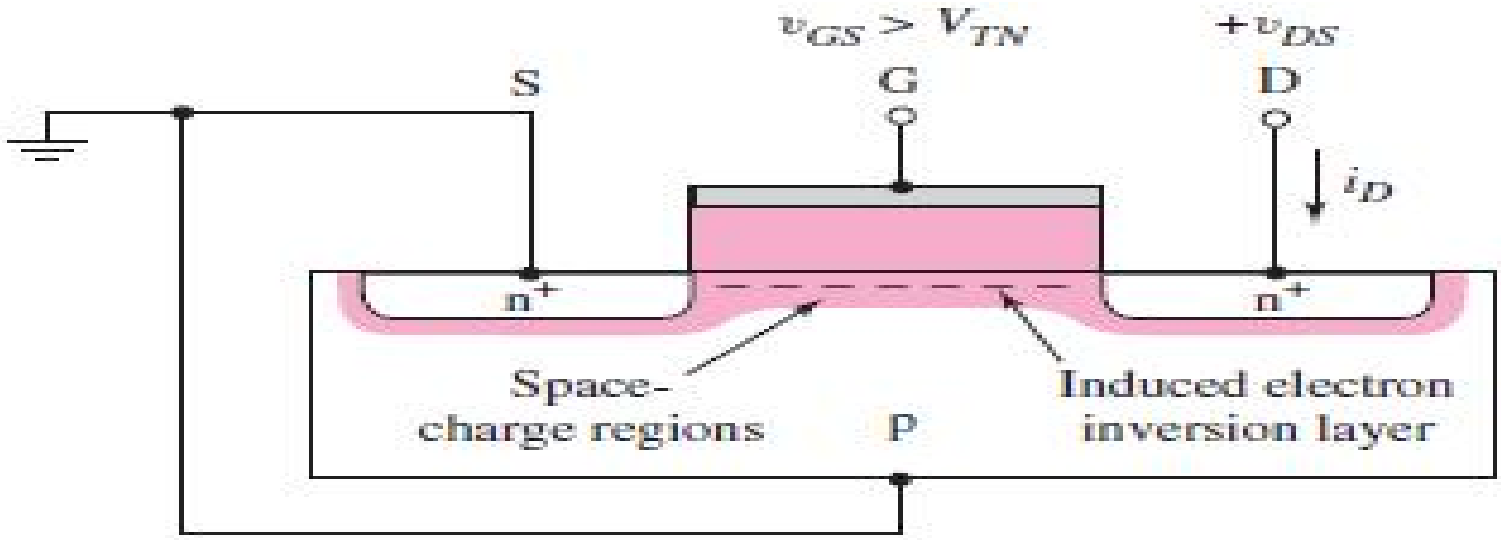

Figure shows the same MOSFET with an applied gate voltage greater than the threshold voltage. In this situation, an electron inversion layer is created and, when a small drain voltage is applied, electrons in the inversion layer flow from the source to the positive drain terminal.

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The *iD versus vDS characteristics for small values of vDS are shown in Figure.* When *vGS < VT N , the drain current is zero. When vGS is greater than VT N,* the channel inversion charge is formed and the drain current increases with *vDS.*

Then, with a larger gate voltage, a larger inversion charge density is created, and the

drain current is greater for a given value of *vDS.*

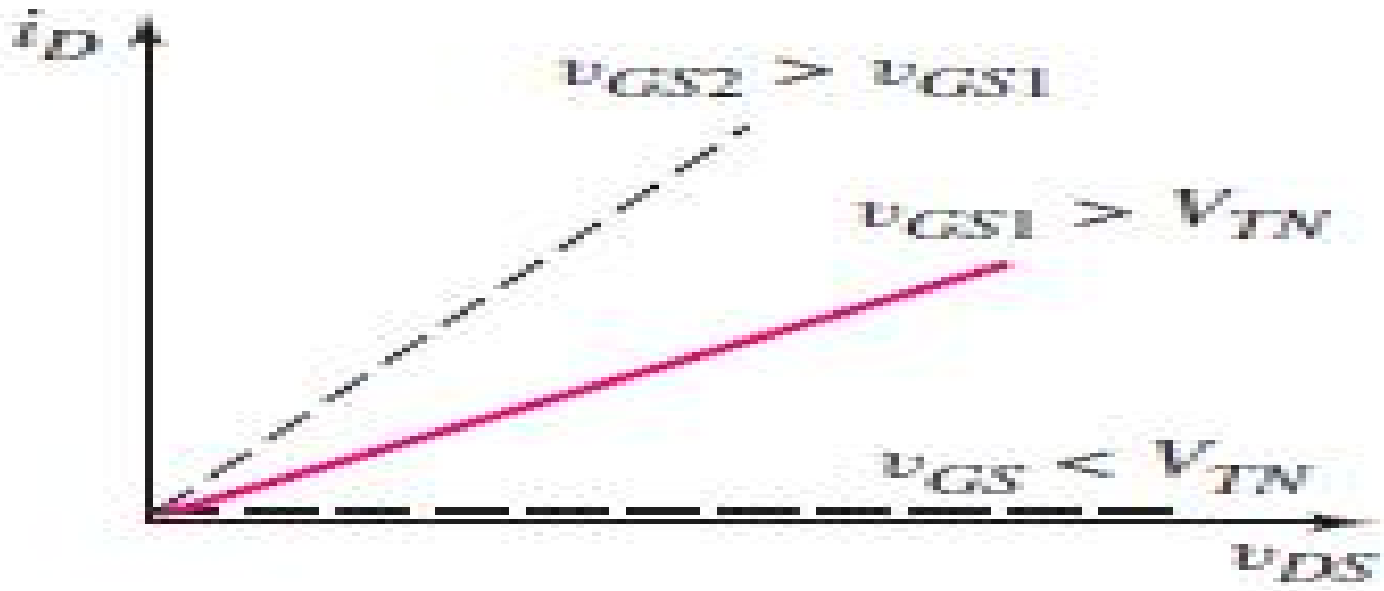

Figure 3.8 Plot of i_D versus v_{DS} characteristic for small values of v_{DS} at three v_{GS} voltages