VLSI IMPORTANT QUESTIONS

1. Draw the stick and circuit diagram of 2-input NAND gate using CMOS and n-MOS technology
2. Draw the stick and circuit diagram of 2-input NOR gate using CMOS and n-MOS technology
3. We have multiple instances in RTL (Register Transfer Language), do you do anything special during synthesis stage?
4. What is Channel length Modulation?
5. What is body effect?
6. What is latch up in CMOS design and ways to prevent it?
7. Difference between mealy and moore state machine?
8. What is CMOS Technology?
9. Give the advantages of CMOS IC.
10. What are four generations of Integration Circuits?
11. Why NMOS technology is preferred more than PMOS technology?
12. What are the different layers in MOS transistor?
13. What is Enhancement mode transistor?
14. What are the steps involved in manufacturing of IC?
15. What is meant by Epitaxy?
16. What are the processes involved in photo lithography?
17. What are the advantages and disadvantages of SOI process?
18. What are the various etching processes used in SOI process?
19. What is BiCMOS Technology?
20. What are the basic processing steps involved in BiCMOS process?
21. What is meant by interconnect? What are the types are of interconnect?
22. What is Stick diagram?
23. What are the uses of Stick diagram?
24. Compare between CMOS and bipolar technologies.
25. Define Threshold voltage in CMOS
26. What is Latch – up?
27. What is demarcation line?
28. What are the two types of Layout design rules?
29. What is Lay-out design rule?
30. What are LVS and DRL tools?
31. What are the cells available in primitive library?
32. Draw the characteristics graph of enhancement mode of n-MOS.
33. What are the three modes in an enhancement MOS transistor?
34. How an Inversion layer is formed in MOS Transistor?
35. What are the different regions that can be defined in n-MOS depending upon the voltages applied?
36. What is the formula for power dissipation for CMOS Inverter?
37. What is pull-down device?
38. How reliability of a VLSI circuit is related to its power dissipation?
39. How environment is affected by the power dissipation of VLSI circuits?
40. What are the commonly used conducting layers used in IC fabrication?
41. Show the basic structure of a MOS transistor.
42. What is the latch up problem that arises in bulk CMOS technology? How is it overcome?
43. Distinguish between the bulk CMOS technology with the SoI technology fabrications.
44. What are the benefits of SOI technology relative to conventional bulk CMOS technology?
45. What are the basic assumptions of the fluid model?
46. Explain the function of a MOS transistor in the saturation mode using fluid model.
47. Explain the function of a MOS transistor in the non saturation mode using the fluid model.
48. Explain the three modes of operation of a MOS transistors.
49. Explain the linear region of the I-V characteristic of an nMOS transistor using the fluid model.
50. What is the threshold voltage of a MOS transistor? How it varies with the body bias?

51. What is channel length modulation effect? How the voltage current characteristics are affected because of this effect?
52. What is body effect? How does it influences the threshold voltage of a MOS transistor?
53. What is transconductance of a MOS transistor? Explain its role in the operation of the transistor.
54. Explain the behaviour of a nMOS transistor as a switch.
55. Explain the behaviour of a pMOS transistor as a switch.
56. How one nMOS and one pMOS transistor are combined to behave like an ideal switch.
57. The input of a lightly loaded transmission gate is slowly changes from HIGH level to LOW level. How the currents through the two transistors vary?
58. How its ON-resistance of a transmission gate changes as the input varies from 0 V to Vdd, when the output has a light capacitive load.
59. Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics.
60. What is noise margin? Find out the noise margin from the actual characteristics of the inverter.
61. Compare the characteristics of the different types of MOS inverters in terms of noise margin and power dissipation.
62. What is the inversion voltage of an inverter? Find out the inversion voltage of a CMOS inverter.
63. How the inversion voltage is affected by the relative sizes of the nMOS and pMOS transistors of the CMOS inverter?
64. Find out the noise margin of a CMOS inverter.
65. How the noise margin is affected by voltage scaling?
66. What is the lower limit of supply voltage of a CMOS inverter. What happens if the supply voltage is further reduced?
67. What is sheet resistance? Find out the expression of the resistance of rectangular sheet in terms of sheet resistance.
68. Find out the capacitance of a MOS capacitor.
69. Find out the expression of delay time of a CMOS inverter.
70. What are the various ways to reduce the delay time of a CMOS inverter?
71. Explain the commonly used technique to estimate the delay time of a CMOS inverter.
72. Justify the reason for not recommending more than 4 pass transistors to use in series in realizing logic circuits.
73. Draw the schematic diagram of an inverting super-buffer and explain its operation.
74. Give the schematic diagram of a Bi-CMOS inverter. Explain its operation.
75. Compare the switching characteristics of a BiCMOS inverter with respect to that for static CMOS for different fan out conditions.
76. Prove that the delay of a series of pass transistors can be reduced from quardratic dependence to linear dependence on the number of transistors in series by inserting buffers at suitable intervals.
77. How the transfer characteristic of a CMOS NAND gate is affected with increase in fan-in?
78. How the transfer characteristic of a CMOS NOR gate is affected with increase in fan-in?
79. How switching characteristic of a CMOS NAND gate is affected with increase in fan-in?
80. How switching characteristic of a CMOS NOR gate is affected with increase in fan-in?
81. How noise margin of a CMOS NAND/NOR gate is affected with increase in fan-in?
82. For a complex/compound CMOS logic gate, how do you realize the pull-up and the pull-down networks?
83. Give the two possible topologies AND-OR-INVERT AND-ORINVERT (AOI) and OR-AND-INVERT (OAI) to realize CMOS logic gate. Explain with an example.
84. Give the AOI and OAI realizations for the sum and carry functions of a full adder.
85. How do you realize pseudo nMOS logic circuits. Compare its advantage and disadvantages with respect to standard static CMOS circuits.
86. In what way relay logic circuits differ from pass transistor logic circuits? Why the output of a pass transistor circuit is not used as a control signal for the next stage?
87. What are the advantages and limitations of pass transistor logic circuits? How the limitations are overcome?
88. Why is it necessary to insert a buffer after not more than four pass transistors in cascade?
89. Why is it necessary to have swing restoration logic in pass transistor logic circuits? Explain its operation.

90. What is the ‘sneak path’ problem of pass transistor logic circuits? How sneak path is avoided in Universal Logic Module (ULM) based realization of pass transistor network. Illustrate with an example.
91. What are the key characteristics of MOS dynamic circuits?
92. Explain the basic operation of a 2-phase dynamic circuit?
93. How 2-phase clocks can be generated using inverters?
94. What makes dynamic CMOS circuits faster than static CMOS circuits?
95. Compare the sources of power dissipation between static CMOS and dynamic CMOS circuits?
96. What is charge leakage problem of dynamic CMOS circuits?How is it overcome?
97. What is charge sharing problem? How can it be overcome?
98. Explain the clock skew problem of dynamic CMOS circuits?
99. How clock skew problem is overcome in in domino CMOS circuits?
100. How charge sharing leads to power dissipation?