Microcontroller and Embedded Systems

MOV and other inst.

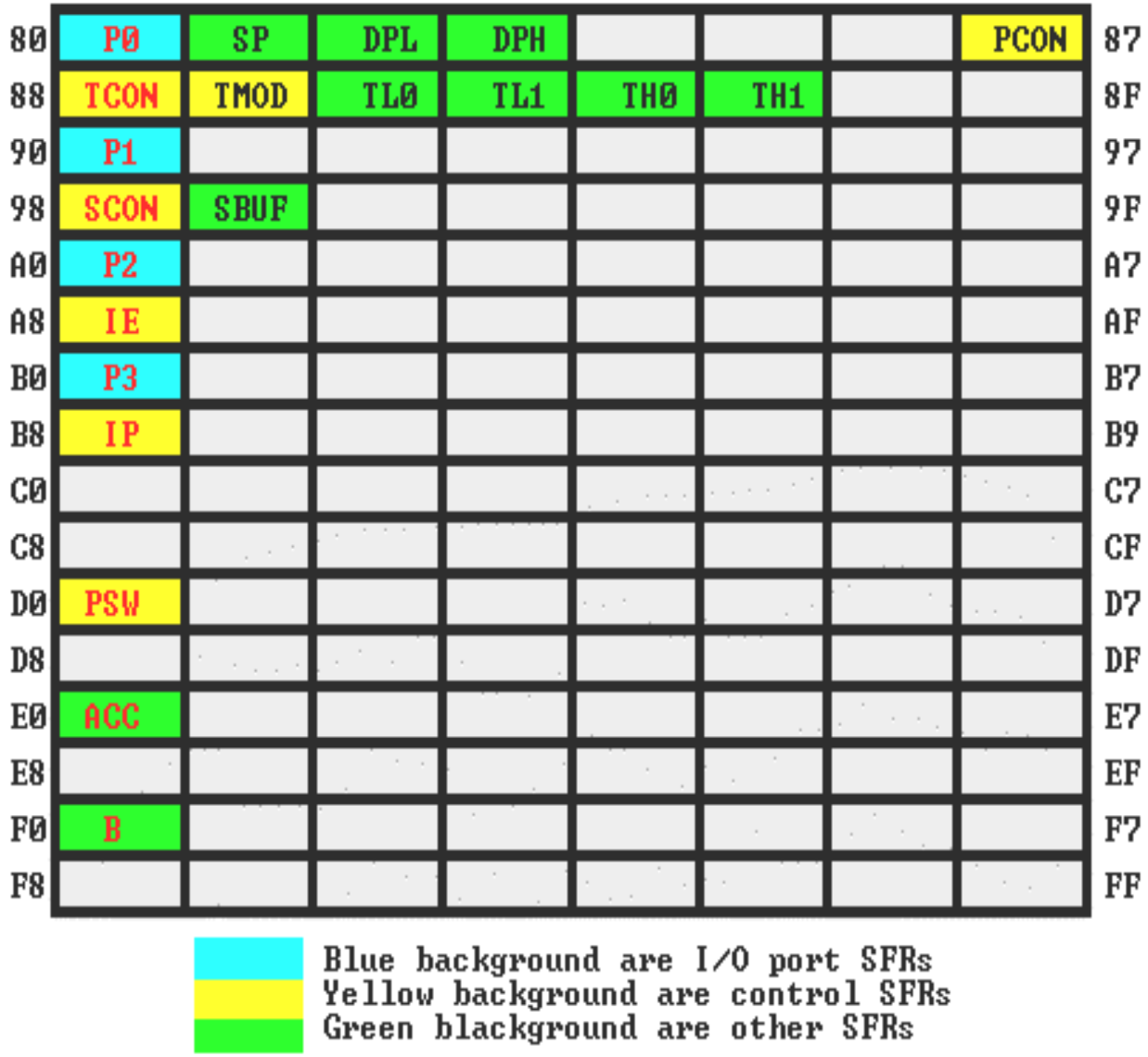
- **MOV A,R3** ;Move the value of R3 into the accumulator
- **MOV R5,A** ;Store the resulting value temporarily in R5
- **MOV A,R1** ;Move the value of R1 into the accumulator
- **MOV A, #55H**
- **(MOV A, #FFH)**
- **MOV A, #0FFH**

ADD and other inst.

- **ADD A, source**
- **ADD A,R2** ;Add the value of R2
- MOV A, #25H
- ADD A,#34H

SFRs(Special Function Registers)

Internal RAM is from address 00h through 7Fh whereas SFR registers exist in the address range of 80h through FFh.



Special Function Registers

- SFRs contain memory locations that are used for special tasks.
- SFR occupies RAM from **0x80 to 0xFF**, (but some areas are empty!) They are 8 bits wide.
- Ex.

➢ **A register** or accumulator is used for most ALU operations & external moves

➢ **B** used for multiplication & division and can also be used for general purpose storage

➢ **PSW Program Status Word** is a bit addressable register.

SPECIAL FUNCTION REGISTERS

ACC	ACCUMULATOR	0E0H
B	B REGISTER	0F0H
SP	PROGRAM STATUS WORD	0D0H
PSW	STACK POINTER	81H
DPTR	DATA POINTER 2 BYTES	
DPL	LOW BYTE	82H
DPH	HIGH BYTE	83H
P0	PORT 0	80H
P1	PORT 1	90H
P2	PORT 2	0A0H
P3	PORT3	0B0H

CONTD
...

IP	INTERRUPT PRIORITY CONTROL	0B8H
IE	INTRRUPT ENABLECONTROL	0A8H
TMOD	TIMER/COUNTER MODE CONTROL	89H
TCON	TIMER COUNTER CONTROL	88H
T2CON	TIMER/COUNTER 2 CONTROL	0C8H
TH0	TIMER/COUNTER 0 HIGH BYTE	8CH
TL0	TIMER/COUNTER 0 LOW BYTE	8AH
TH1	TIMER/COUNTER 1 HIGH BYTE	8DH
TL1	TIMER/COUNTER 1 LOW BYTE	8BH
TH2	TIMER/COUNTER 2 HIGH BYTE	0CDH
TL2	TIMER/COUNTER 2 LOW BYTE	0CCH

RCAP 2H	T/C 2 CAPTURE REG. HIGH BYTE	0CBH
RCAP2L	T/C 2 CAPTURE REG. LOW BYTE	0CAH
SCON	SERIAL CONTROL	98H
SBUF	SERIAL DATA BUFFER	99H
PCON	POWER CONTROL	87H

PC or program counter. This is not directly addressable, nor does it have a memory location.
It is not part of SFR.

DPTR or data pointer. DPL and DPH.

DPTR doesn't have a single internal address.

This is used to furnish memory addresses for internal and external code access and external data access.

SFRs

SFRs which are also bit addressable

A, B, IP, IE, TCON, SCON, PSW, P0, P1, P2, P3

Other SFRs

TMOD, THO, TLO, TH1, TL1, SBUF, PCON, SP, DPTR

PROGRAM STATUS WORD- BIT ADDRESSABLE

CY	AC	F0*	RS1	RS0	OV	-*	P

- CY-CAARY FLAG
- AC AUXILLARY CARRY FLAG
- F0 –GENERAL PURPOSE FLAG
- RS1- REGISTER BANK SELECTOR BIT
- RS0- REGISTER BANK SELECTOR BIT
- OV- OVERFLOW FLAG
- - USER DEFINABLE FLAG
- P- PARITY FLAG

SELECTION OF REGISTER BANK

RS1	RS0	REGISTER BANK
0	0	0
0	1	1
1	0	2
1	1	3

Interrupts

Interrupts are just *special subroutines that may (or may* not) be called explicitly.

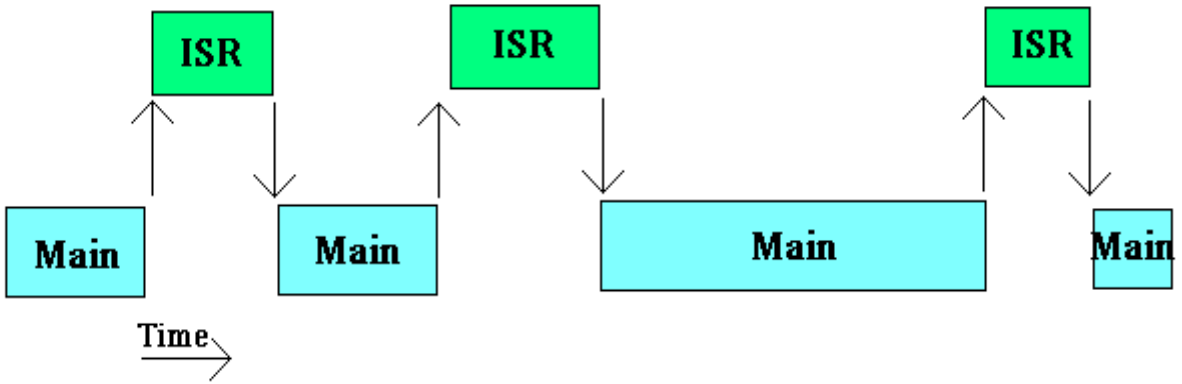
If conditions are “right”, when an interrupt occurs, then the processor will stop what it is doing, and jump to a specific place in memory (decided by the Intel 8051 designers) hooked by that particular interrupt.

It is up to the programmer to make sure that you supply a sensible further course of action. This is called the interrupt handler routine or *interrupt service routine , ISR.*

Interrupt :

Program execution without intrrupts :

Program execution with intrrupts :



ISR : Intrrupt Service Routin