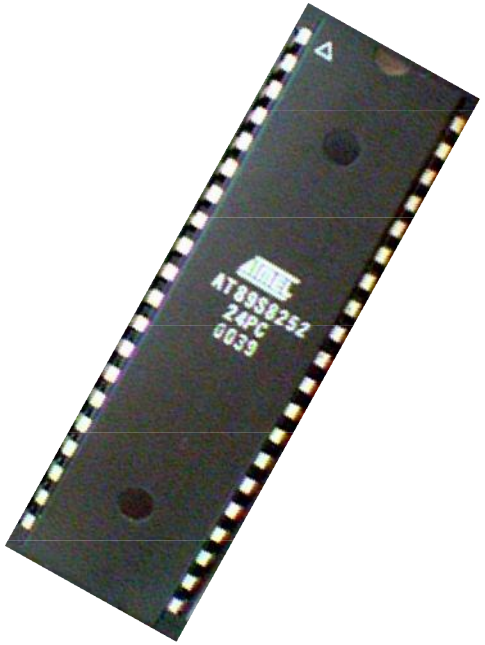
Microcontroller and Embedded Systems

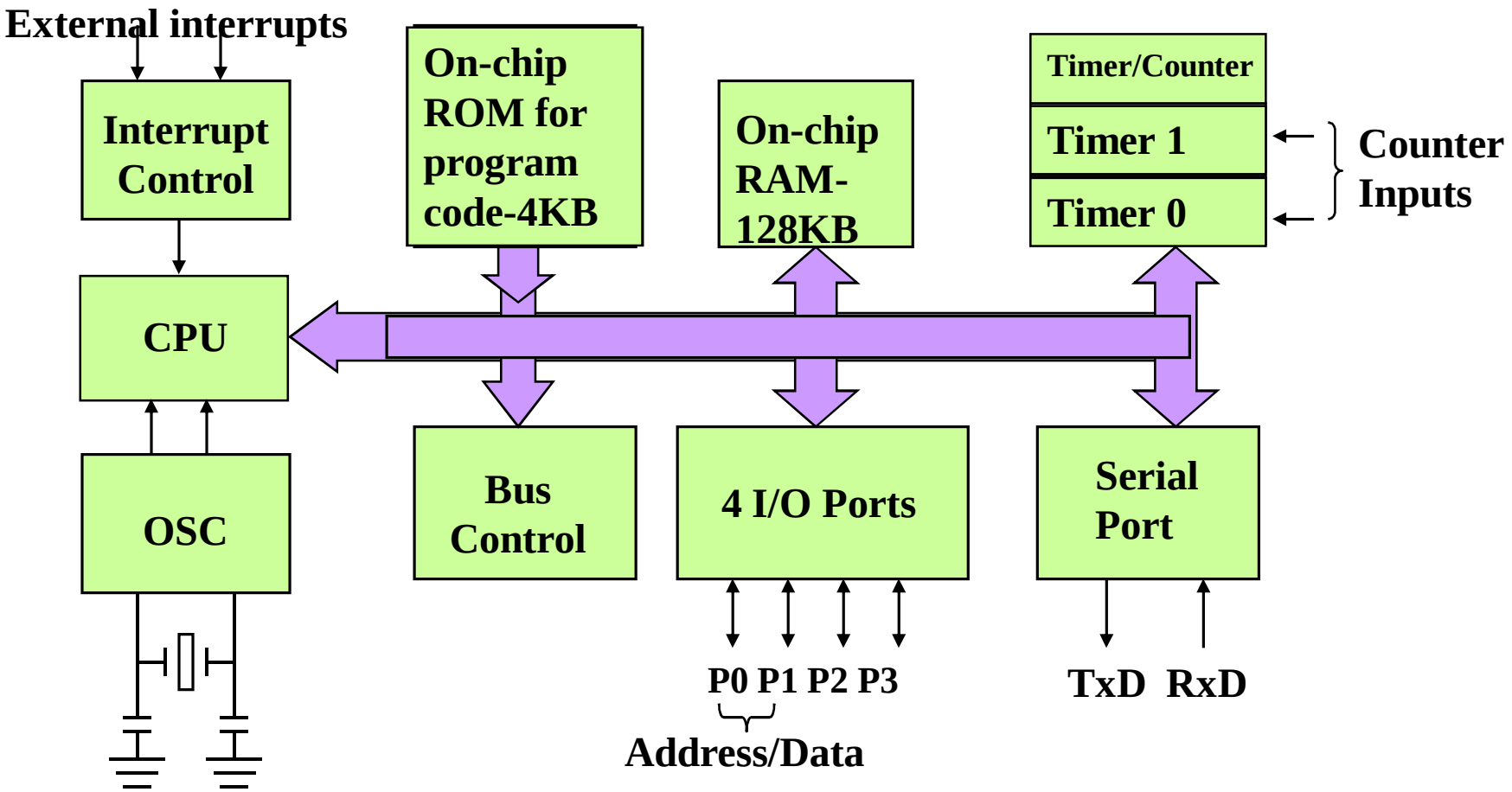
Microcontroller 8051



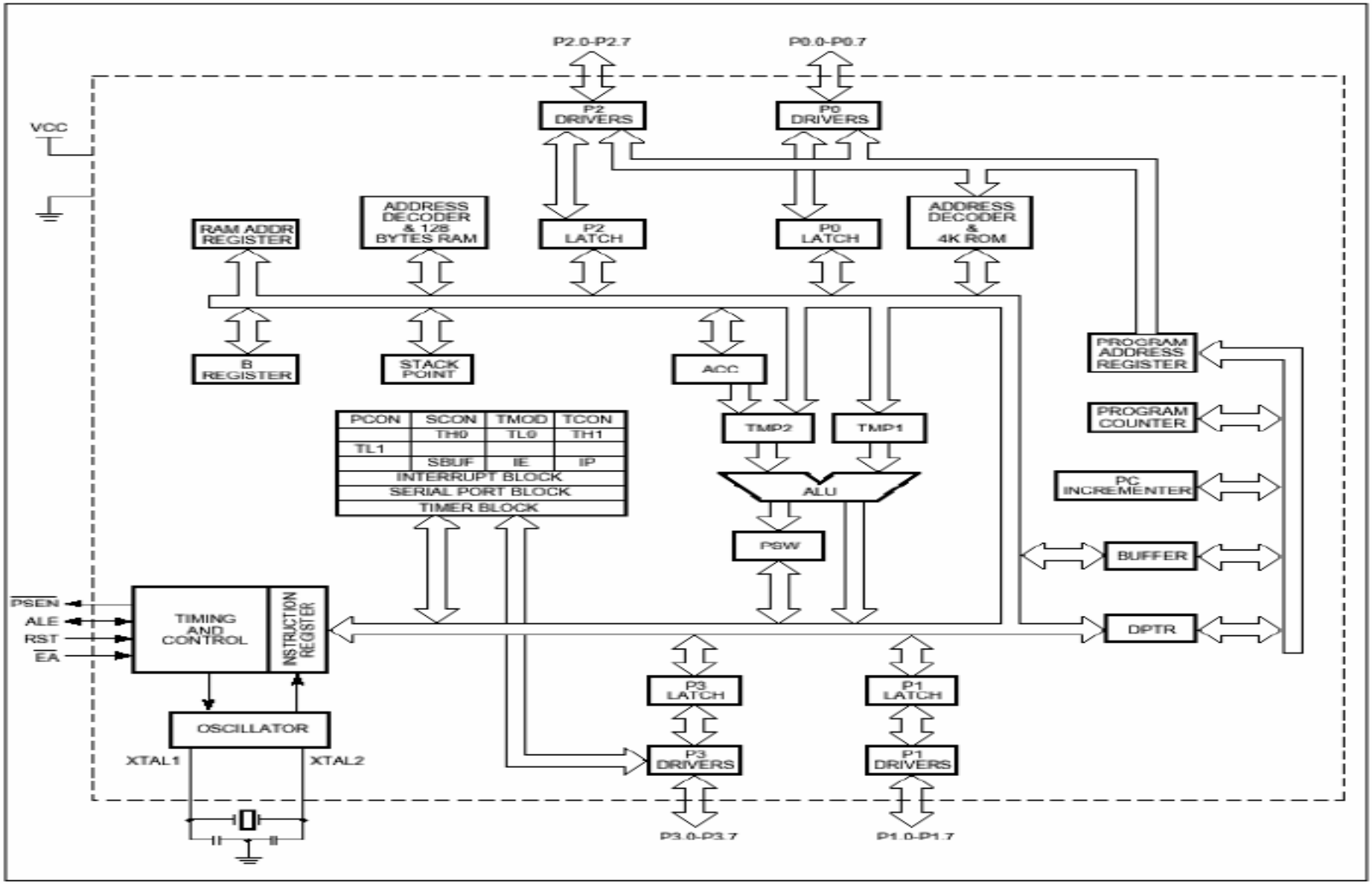
FEATURES OF 8051

- **8- bit microcontroller**
- Operating frequency is **11.0592 MHz**.
- Separate program memory and data memory (**Harvard**).
- Separate 64K program and 64K data memory.
- **4k of on chip EPROM for program memory.**
- **128 bytes RAM (in built)**
- **32 bi-directional and individually addressable I/O lines.**
- **Two nos. of 16-bit timer/counter T0 and T1.**
- Full duplex **UART.**
- On-chip clock oscillator
- **Interrupts from six sources, 2 external and 4 internal.**
- **255** instructions.
- **Bit processing** capability.
- **16-bi**t add bus multiplexed with P0 and P2, data bus mux P0

Block Diagram



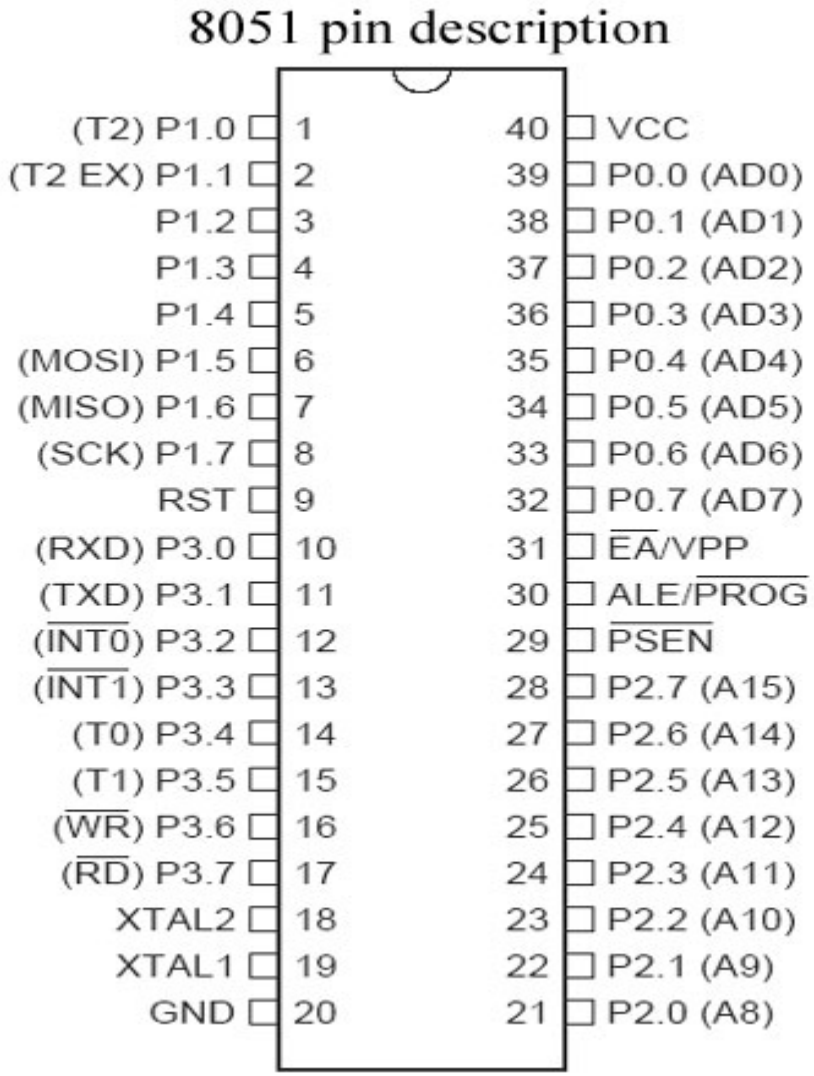
ARCHITECTURE OF 8051



- 8051 Architecture
- 32 I/O pins arranged as four 8 bit ports (P0 – P3)
- 2 16-bit timer/counters: T0 and T1
- Full duplex serial data receiver/transmitter: SBUF
- Control registers: TCON, TMOD, SCON, PCON, IP
- and IE
- 2 external and 4 internal interrupt sources
- Oscillator and clock circuits

8051 PIN DESCRIPTION

- **8051 other family members:**
  - 8751 (has EPROM)
  - 8951 (has EEPROM)



8051 PIN DESCRIPTION contd.

- Vcc → +5 v ,125 mA, max power diss 1W.
- Vss→ Gnd.
- XTAL2 →o/p of the cryt osc. Ckt is connected. 30pf disc capacitors, when 12MHz quartz cryt is used. In case of external clock , clock is connected to XTAL2.
- XTAL1 → i/p of cryt osc. Ckt is connected. In case of external clock, it is connected to Gnd.
- Port 0 → bidi, serve as low order address and data bus for external memory.
- Port 1 →bidi 8 bit I/O port.
- Port 2 → bidi 8 bit I/O port, and high order address bus.
- Port 3 → bidi 8 bit I/O port and serial i/p ,serial o/p, external int

8051 PIN DESCRIPTION contd.

P3 Bit	Function	Pin
P3.0	RxD	10
P3.1	TxD	11
P3.2	$\overline{\text{INT0}}$	12
P3.3	$\overline{\text{INT1}}$	13
P3.4	T0	14
P3.5	T1	15
P3.6	$\overline{\text{WR}}$	16
P3.7	$\overline{\text{RD}}$	17

8051 PIN DESCRIPTION contd.

P0	P1	P2	P3	Port Bit
P0.0	P1.0	P2.0	P3.0	D0
P0.1	P1.1	P2.1	P3.1	D1
P0.2	P1.2	P2.2	P3.2	D2
P0.3	P1.3	P2.3	P3.3	D3
P0.4	P1.4	P2.4	P3.4	D4
P0.5	P1.5	P2.5	P3.5	D5
P0.6	P1.6	P2.6	P3.6	D6
P0.7	P1.7	P2.7	P3.7	D7

Port Operations

- To read and write from port:

MOV A, P0 or

MOV A,80h

(This copies data from port 0 pins to register A).

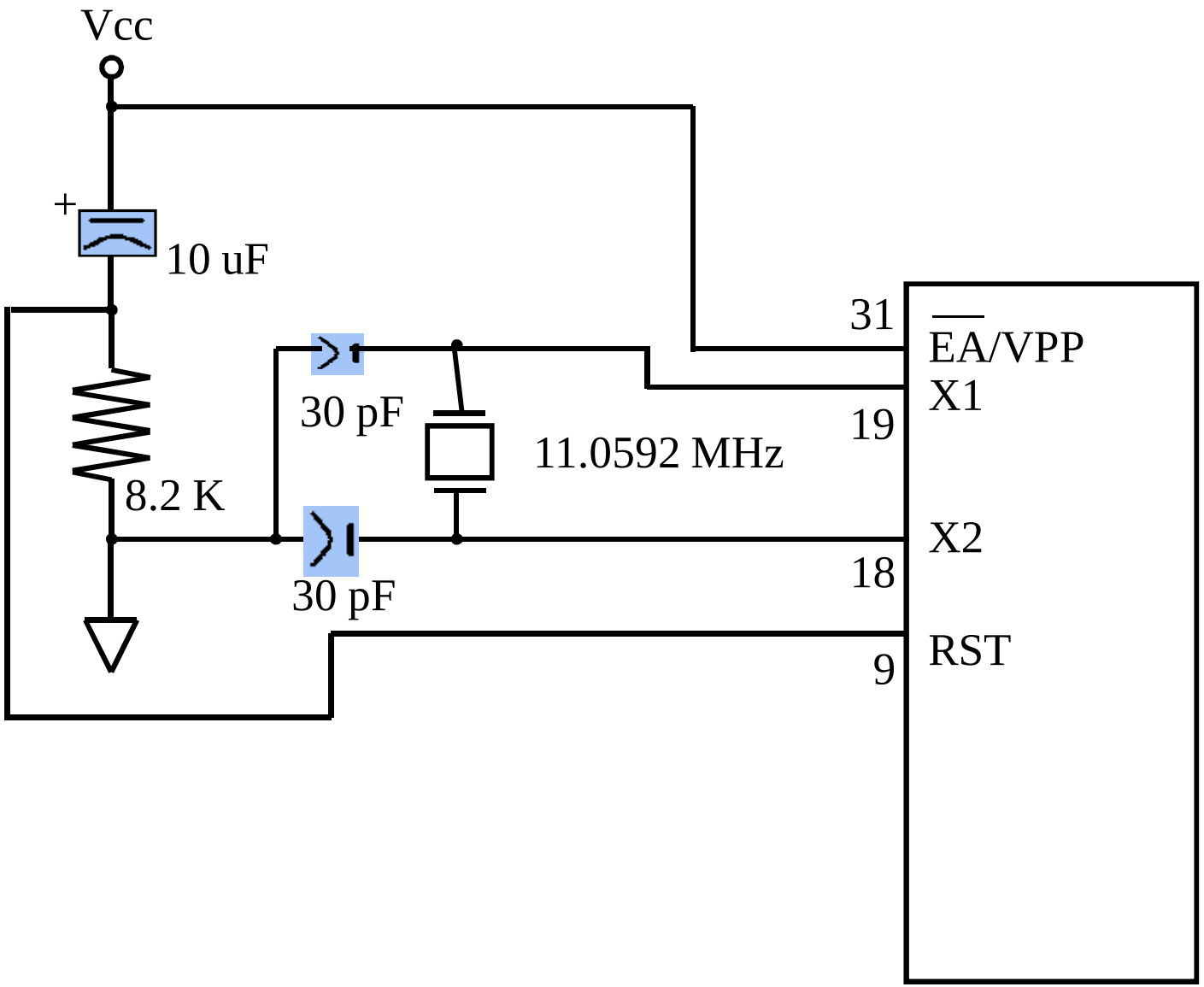
MOV P1, #0a5h or

MOV 90h,#0a5h

(This moves a constant number into port1).

- Moving data to a port changes the port latch,
- moving data from a port gets data from the port pins.

Figure (b). Power-On RESET Circuit



8051 PIN DESCRIPTION contd.

- RST → (reset ckt.) as shown in fig. for resetting 8051, RST pin is made high for 2 m/c. Table below lists SFR's and reset values

PC	0000H
ACC,B,PSW	00H
SP	07

Register	Reset Value (Binary)
P0	11111111
P1	11111111
P2	11111111
P3	11111111