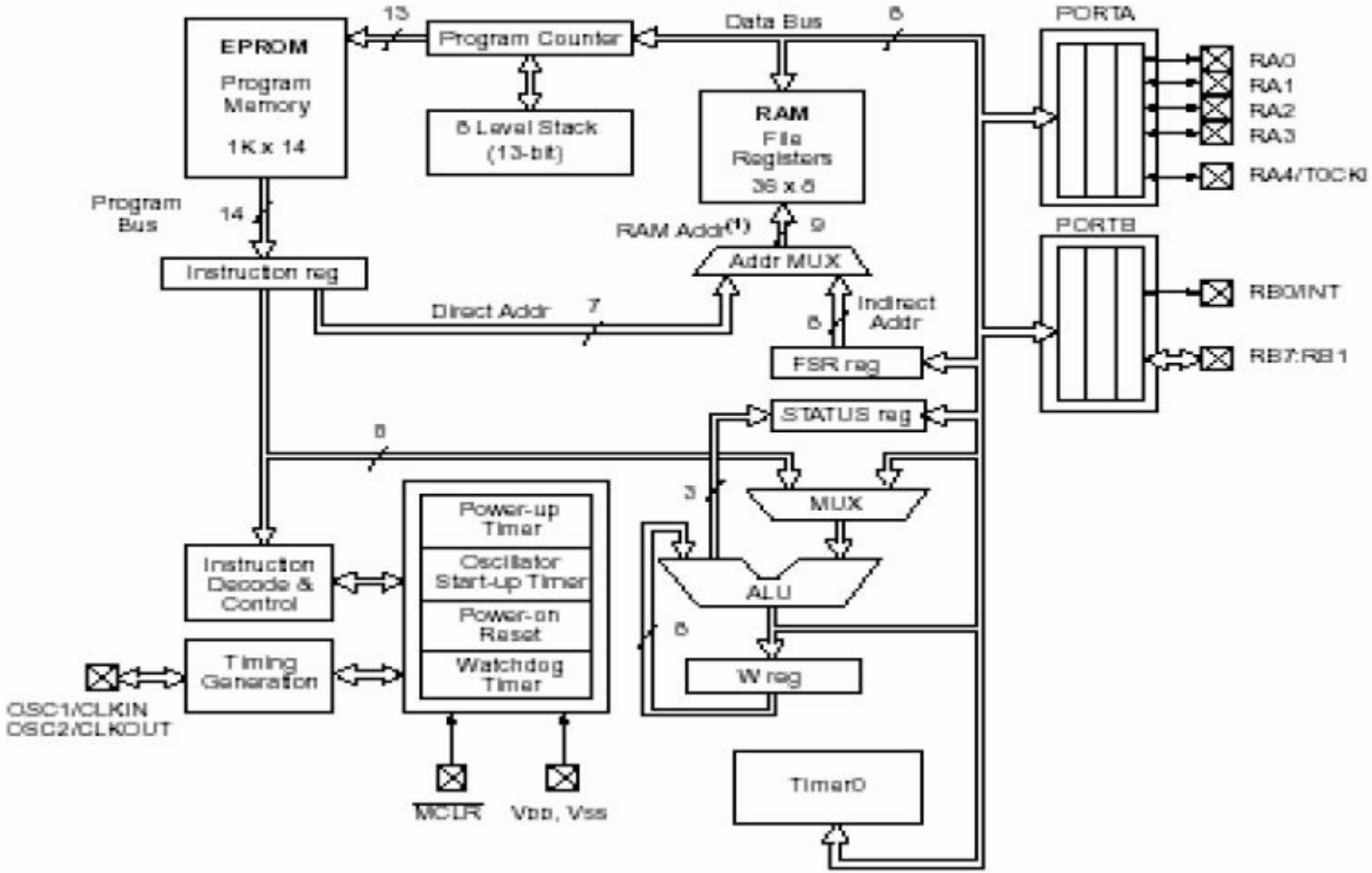
PIC Architecture

PIC Internal Architecture



PIC Architecture

- ALU

  Size is 8 bit

  Performs operations with temporary working register and (W register) and any register file.

- W register

  8 bit wide. It contains one of source operands during execution of instruction and may serve as the destination for the result of operation.

  Used only for ALU operations.

Architecture Continued…

- STATUS Register

7	6	5	4	3	2	1	0
0	0	RP0	$\overline{T0}$	$\overline{PD}$	Z	DC	C

C = Carry Bit

DC = Digits Carry (Same as AC)

- $\overline{Z}$ = Zero
- $\overline{TO}$ = Reset status bit (Time out bit)
- $\overline{PD}$ = Reset status bit (Power down)

These bits are used along with SLEEP mode. After coming out from SLEEP processor checks these bits to determine which kind of event is responsible for bringing out of SLEEP mode.

- RP0 = Register Bank Select bit.If 0 selects bank 0 otherwise bank 1.

Architecture Contd..

- FSR Register (File Selection Register)

  FSR is a pointer used for indirect memory addressing in the whole register file. In indirect addressing mode one has to write address byte in FSR and then use INDF (Indirect thro FSR).INDF is used in instruction.

Architecture Contd..

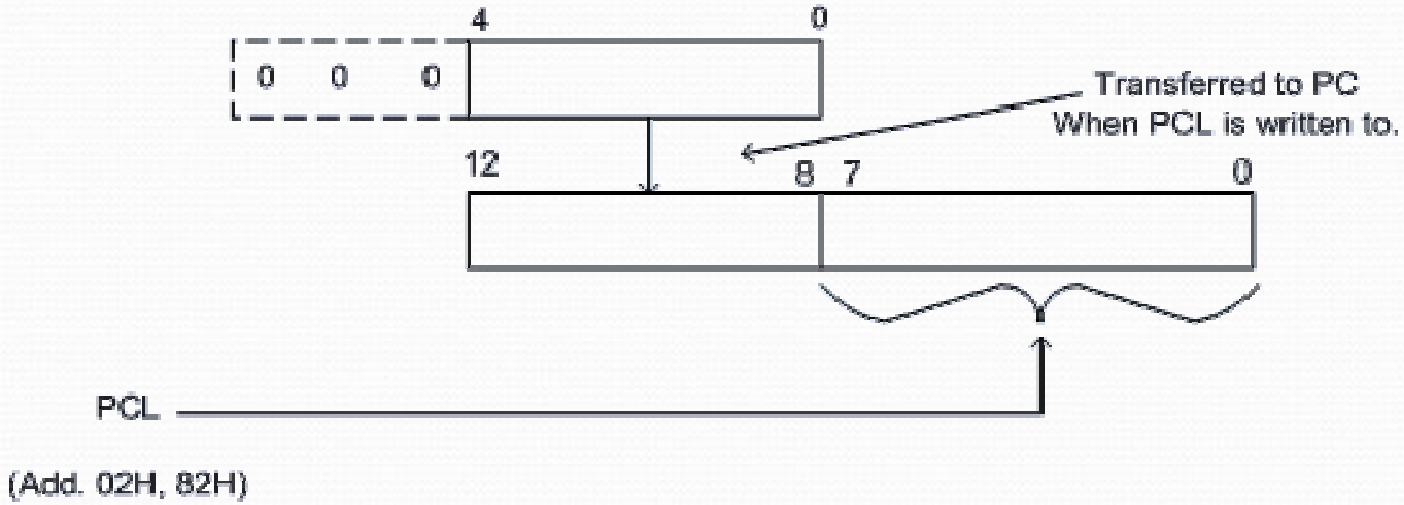
- PCLATH (PC Latch)
- Can be independently read or written like any other register.
- It's different from PC and is separate entity.
- It is 5 bits.This is added with PCL (Program Counter Lower) so as to get 13 bit address.

PCL Register

(Program Counter Low Byte, address = 02H, 82H)
PCL is actually the lower 8-bits of the 13-bit program counter. This is a both readable and writable register.

PCLATH Register

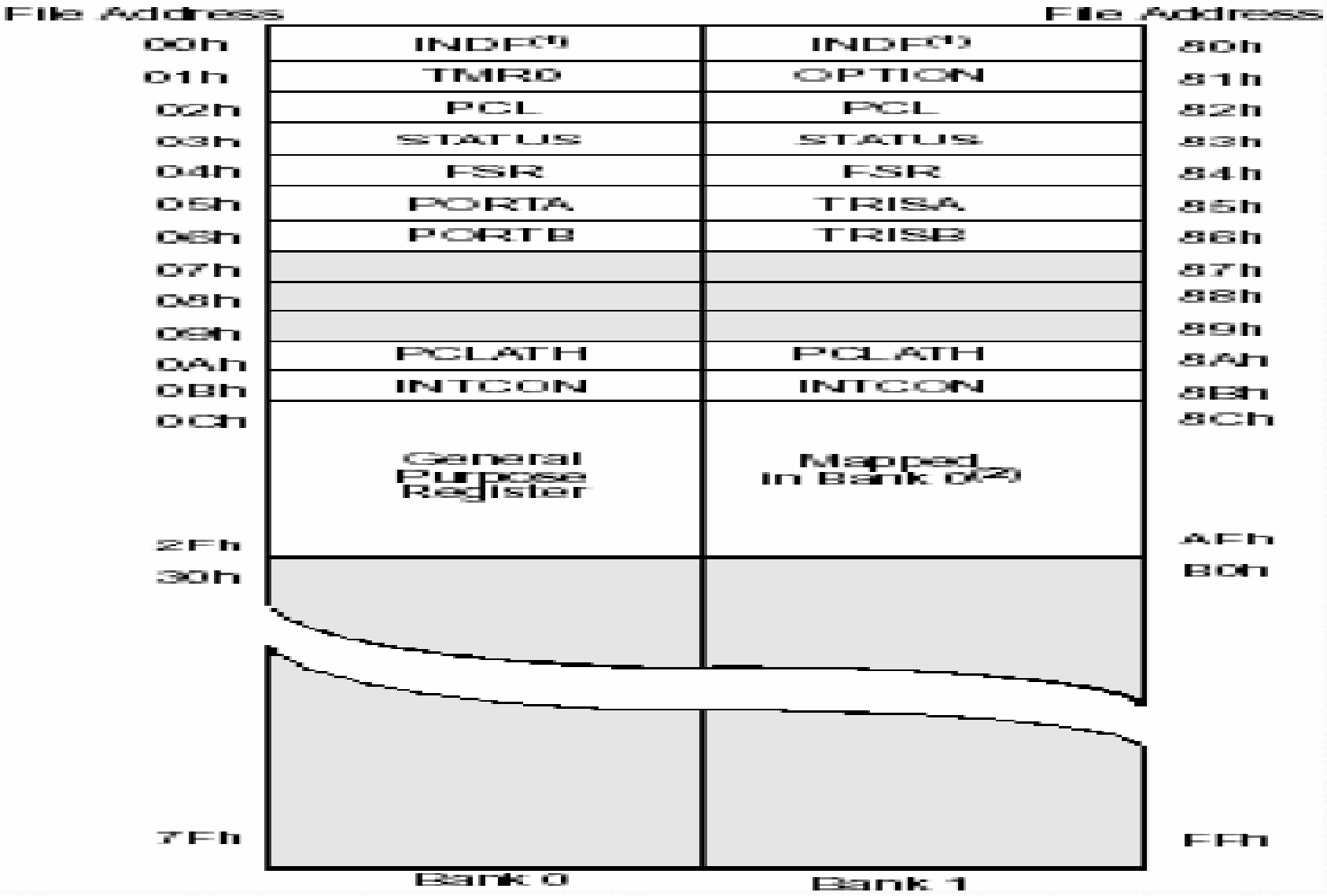
(Program Counter Latch, address = 0AH, 8AH)
PCLATH is a 8-bit register which can be used to decide the upper 5bits of the program counter. PCLATH is not the upper 5bits of the program counter. PCLATH can be read from or written to without affecting the program counter. The upper 3bits of PCLATH remain zero and they serve no purpose. When PCL is written to, the lower 5bits of PCLATH are automatically loaded to the upper 5 bits of the program counter, as shown in the figure.



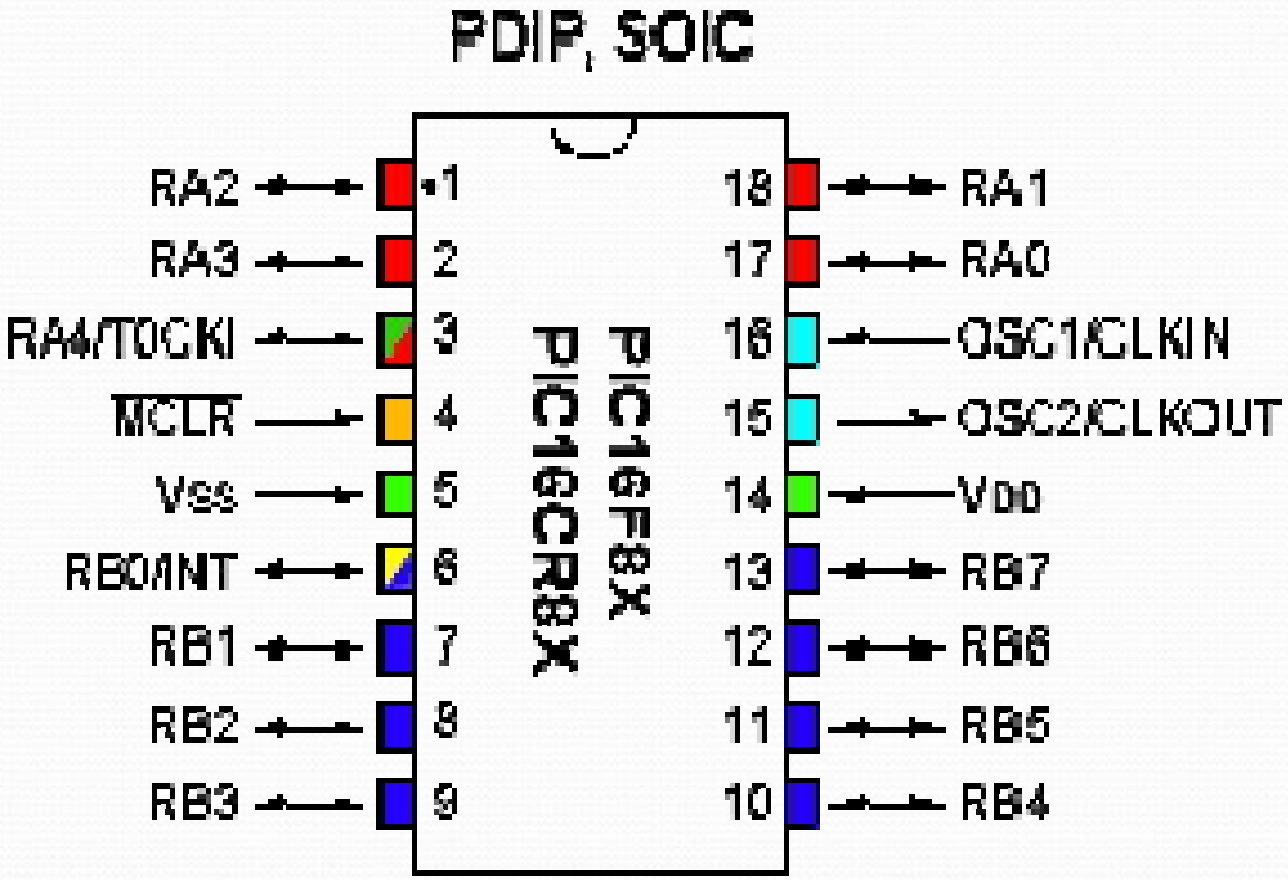
Program Counter Stack

An independent 8-level stack is used for the program counter. As the program counter is 13bit, the stack is organized as 8x13bit registers. When an interrupt occurs, the program counter is pushed onto the stack. When the interrupt is being serviced, other interrupts remain disabled. Hence, other 7 registers of the stack can be used for subroutine calls within an interrupt service routine or within the mainline program.

Register File Map



Port Structure and Pin Configuration of PIC 16C8X



PIC 16C8X DESCRIPITION

Port A

RA0 to RA4 (5 lines)(Address 05)

RA4 has alternate function. TRISA(85H)

is SFR used to configure these lines individually as either inputs or outputs.Setting bit in TRIS will configure as input and 0 will configure as output.

Port B

RB0 to RB7(8 lines).TRISB

It has weak internal pull up which is to be

Enabled.

PIC 16C8X DESCRIPITION

Pin Name	DIP/SOIC Number	Description
OSC1/CLKIN	16	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR	4	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
RA0	17	PORTA is a bi-directional I/O port.
RA1	18	
RA2	1	

RA3	2	
RA4/T0CKI	3	This Pin can also be selected to be the clock input to the TMR0 timer/counter.
RB0/INT	6	PORTB is a bi-directional I/O port. RB0/INT can also be selected as an external interrupt pin.
RB1	7	
RB2	8	
RB3	9	
RB4	10	
RB5	11	
RB6	12	
RB7	13	
VSS	5	Ground reference for logic and I/O pins.
VDD	14	Positive supply for logic and I/O pins.