

# Microcontroller and Embedded Systems

# Classification of Microcontrolles

- ***Processor Architecture***

- i) Harvard architecture ii) Princeton architecture

- ***Memory***

- i) DATA ii) PROGRAM

- ***Types of memory***

- i) NONE ii) PROM iii) EPROM iv) EEPROM v) Flash

- ***Instructions***

- i) CISC ii) RISC

# PROCESSOR ARCHITECTURE

- HARVARD VERSUS PRINCETON: HARVARD UNIVERSITY AND PRINCETON UNIVERSITIES OF USA HAS GIVEN THE COMPUTER ARCHITECTURE .
- CISC OR RISC ( Complex Instruction set Computers OR Reduced Instruct Set Computers)

# HARVARD VERSUS PRINCETON

## HARVARD

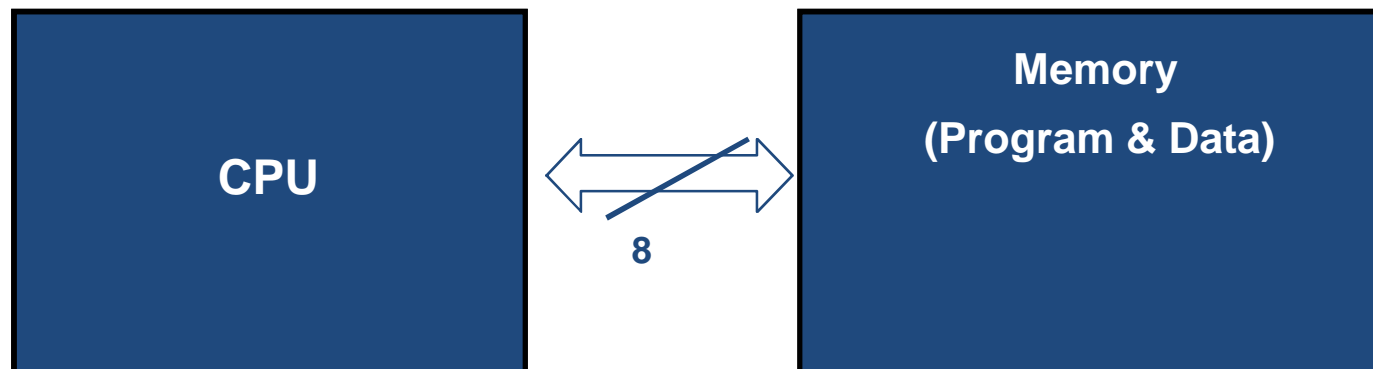
1. It uses separate memory banks for program storage, the processor stack and variable RAM.
2. Previously ignored till 1970 but later it is more popular.
3. Executes instructions in fewer instruction cycle due to Instruction Parallelism.
4. It can carryout the instruction while the next instruction is being fetched from memory and hence helps instructions to take the same no. of cycles for easier timing of loops and critical code.

## PRINCETON

1. It uses the common memory for storing the control program as well as variables and other data structures.
2. It was more popular earlier because it simplifies the microcontroller chip design because only one memory is accessed.
3. Executes instructions in more cycles.
4. it requires separate cycles to execute and fetch the instruction.

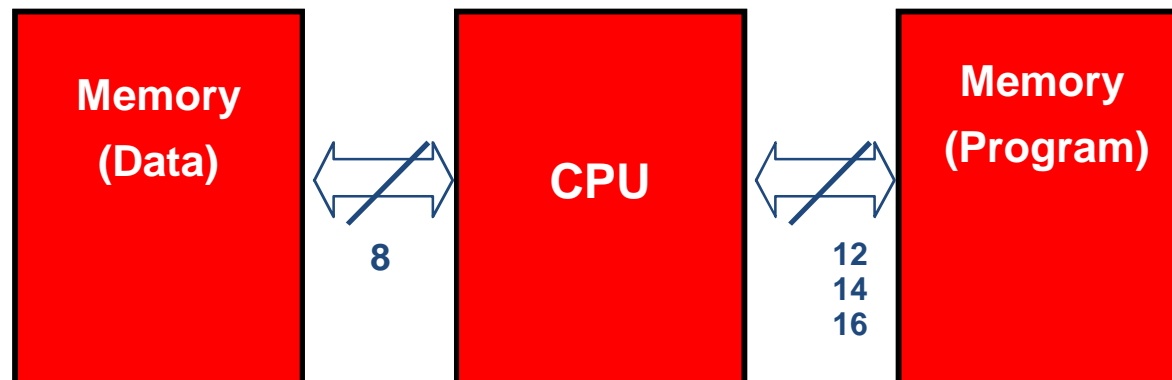
# Von-Neuman/Princeton Architecture

- Used in: 80X86 (PCs), 8051, 68HC11, etc.)
- **Only one** bus between CPU and memory
- RAM and program memory share the same bus and the same memory, and so must have the same bit width
- **Bottleneck:** Getting instructions interferes with accessing RAM



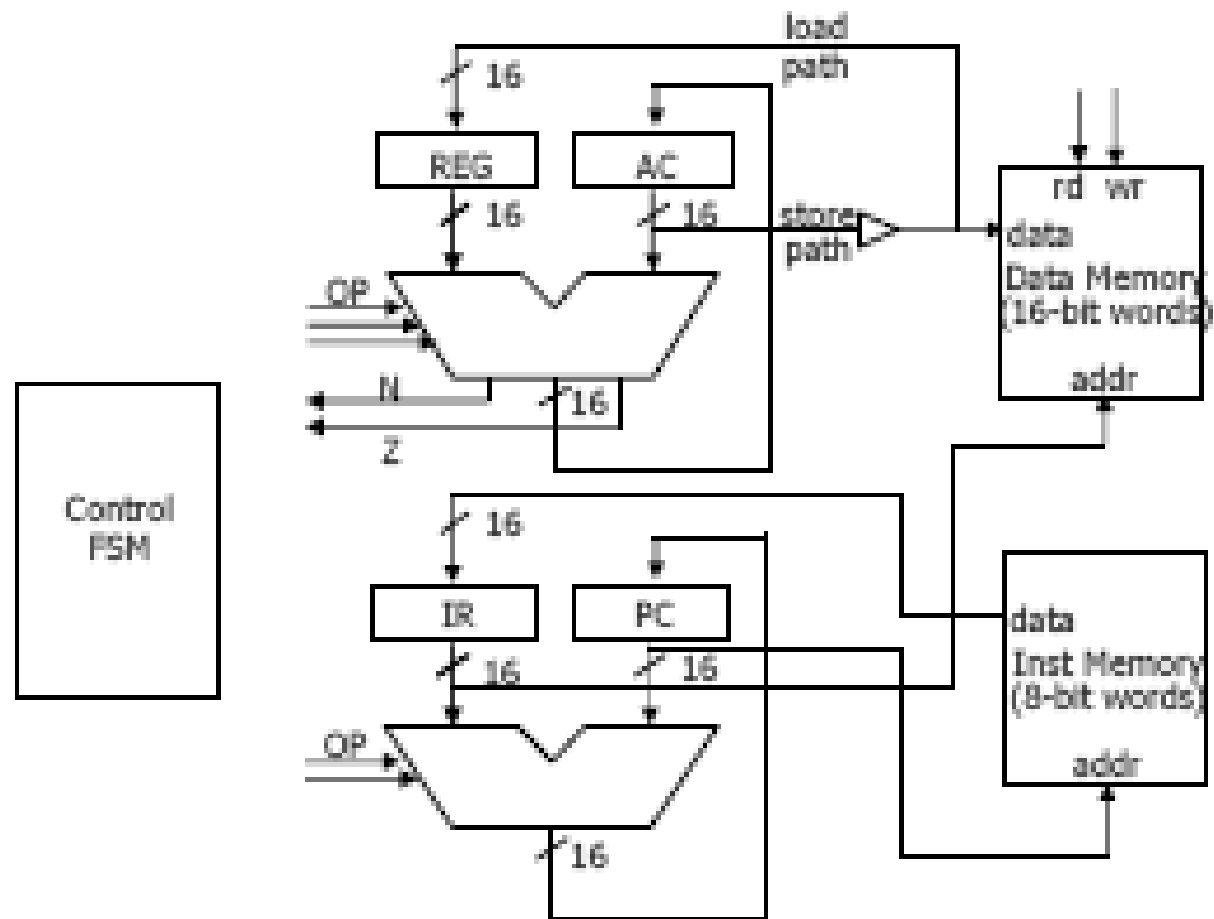
# PICs use the Harvard Architecture

- Used mostly in RISC CPUs (we'll get there)
- **Separate** program bus and data bus: can be different widths!
- For example, PICs use:
  - Data memory (RAM): a small number of 8bit registers
  - Program memory (ROM): 12bit, 14bit or 16bit wide (in EPROM, FLASH, or ROM)



# Block diagram of processor (Harvard)

- Register transfer view of Harvard architecture
  - Separate busses for instruction memory and data memory



# Block diagram of processor (Princeton)

- Register transfer view of Princeton architecture
  - Single unified bus for instructions, data, and I/O

