PC Peripherals for Technicians

Interfaces: Parallel Port

The Parallel Port

OBJECTIVES: At the end of this section, the student will be able to do the following:

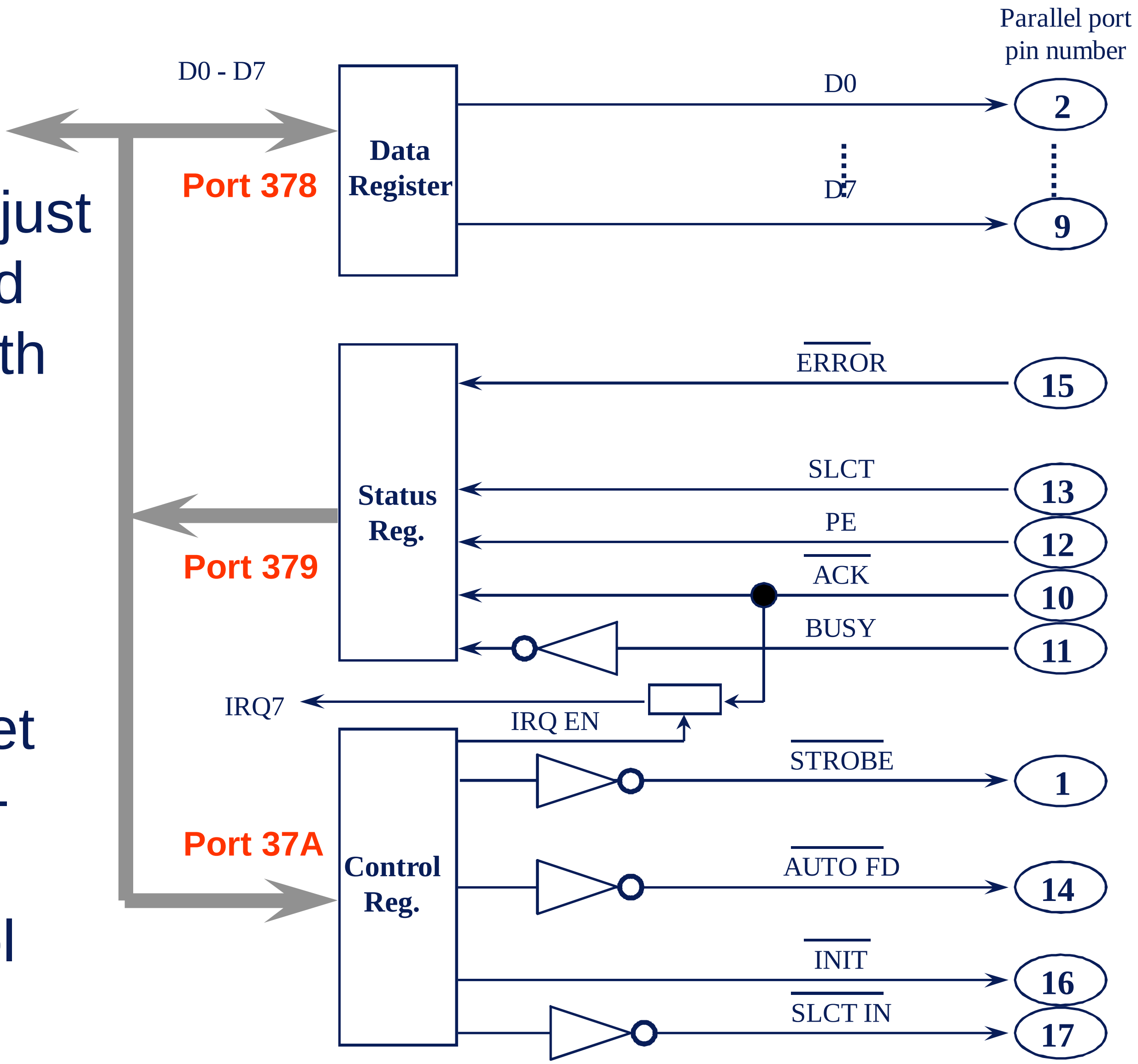
- Describe the functions of the Standard Parallel Port.
- Discuss Parallel Port I/O addresses.
- Describe the Standard Parallel Port registers and connector input/output signals.
- Explain the use of loopbacks for testing the SPP.
- Discuss Parallel Port BIOS support.
- Discuss the IEEE-1284 standard and the EPP/ECP Bi-directional modes.

Standard Parallel Port Overview

- The PC parallel port is specifically designed to attach printers with a parallel port interface, but it can be used as a general input/output port for any device or application that matches its input/output capabilities.
  - The parallel port in the original IBM PC is sometimes called the SPP, for **S**tandard **P**arallel **P**ort
    - » Other names used are AT-type or ISA-compatible.
  - The port in the original PC was based on an existing Centronics printer interface & had no written standard beyond the diagrams and documentation for the IBM PC.
  - The SPP transfers 8 bits at once to a peripheral, using a protocol similar to that used by the ***Centronics*** interface.
    - » ***Centronics*** was a printer manufacturer that ceased to exist many years ago.

Standard Parallel Port Overview

- The parallel port contains no intelligence and is just a set of latches and buffers together with some address decoding circuitry.
- Software outputs instructions that explicitly set & reset bits in the latches--these are used to generate all control signals.



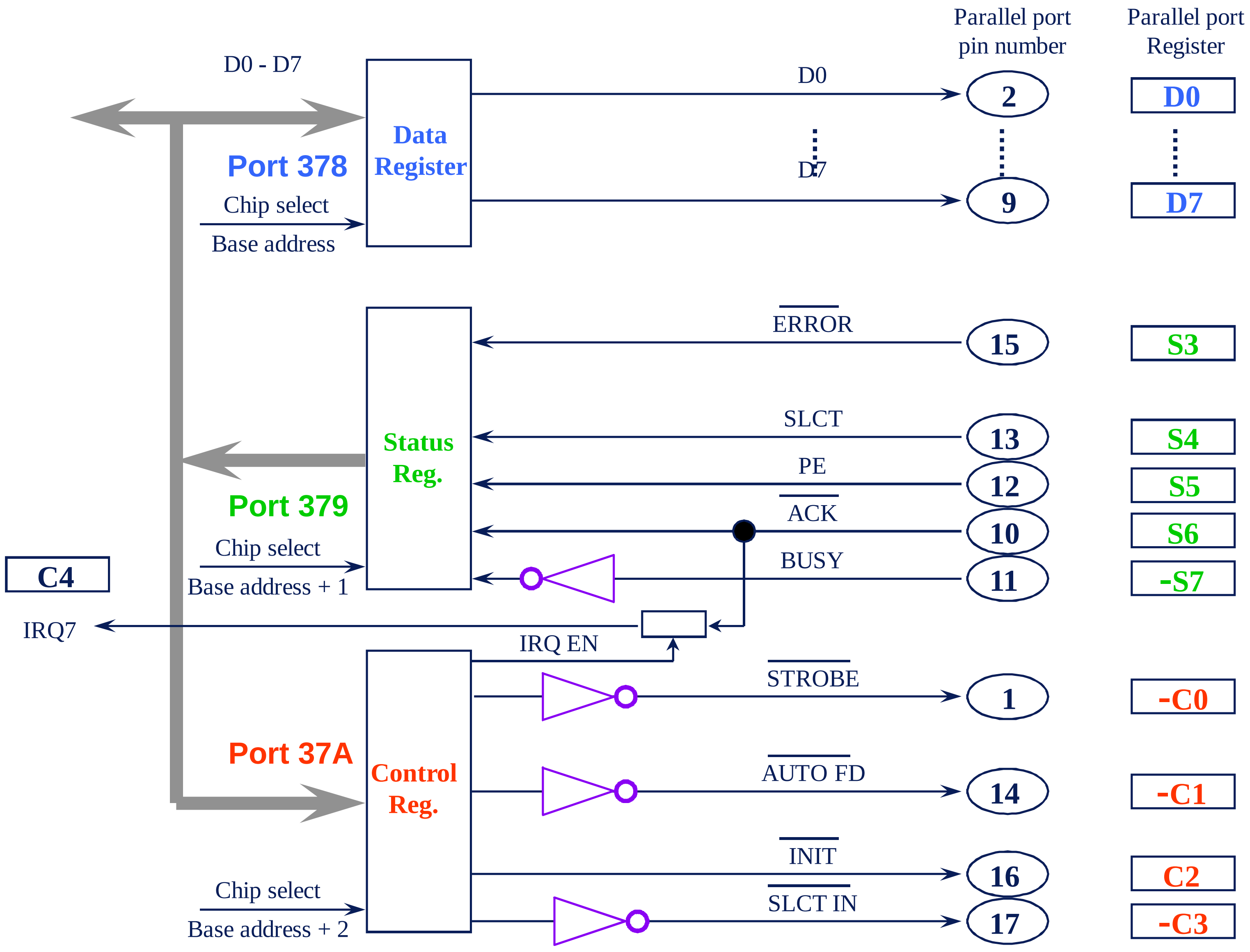
Parallel Port Addresses & Names

- The standard parallel port uses three contiguous addresses, usually in one of these ranges:
  - » **378h, 379h, 37Ah**
  - » 278h, 279h, 27Ah
  - » 3BCh, 3BDh, 3BEh
    - > For ports implemented on Monochrome Video Cards.
  - ➢ **On newer systems the parallel port base address is most often at 378h, but all three addresses are reserved for parallel ports.**
- Addresses:
  - ➢ The 1st address (e.g. 378h) is the port's base address, also called the Data register or just the port address.
  - ➢ The 2nd address (e.g. 379h) is the port's Status register
  - ➢ The 3rd address (e.g. 37Ah) is the Control register.

Parallel Port Addresses & Names

- During POST, the BIOS checks for parallel printer ports by writing data at base addresses 0x3BC, 0x378, and 0x278, reading the same address, and deciding that there is a port installed if it compares.
  - The BIOS stores the base addresses (2 bytes) of any parallel ports that are found in consecutive locations in a table starting at main memory address 0x408.
    - The first entry in the BIOS table at 0x408 becomes LPT1, the 2nd LPT2, and the 3rd LPT3 (if there are that many).
      - **LPT1 parallel port base address is most often 0x378.**
      - **0000:0408 78 03 (0378h stored in little endian format)**
    - Some software ignores this table, but it is used by the BIOS itself (e.g. - INT 17, Printer I/O) and by DOS.
      - The DOS device "PRN" is a software alias--by default LPT1. (The DOS MODE command changes the PRN alias).

Std Parallel Port Registers & Pinout



Std Parallel Port Registers & Pinout

	Bits	7	6	5	4	3	2	1	0
Base (e.g 378h)	Data	X	X	X	X	X	X	X	X
Base+1 (e.g 379h)	Status	-X	X	X	X	X			
Base+2 (e.g 37Ah)	Control					-X	X	-X	-X

- Base Address = 278, 378, or 3BC Hex
  - **i.e. Base = 378 Hex DATA PORT**
  - **i.e. Base+1 = 379 Hex STATUS PORT**
  - **i.e. Base+2 = 37A Hex CONTROL PORT**
- NOTE: S7, C0, C1 & C3 are inverted **(-X)**.
  - i.e. Parallel Port pin 11 high (Busy) will set S7=0
  - i.e. C0=1 causes Parallel Port pin 1 (Strobe#) to go Low

Std Parallel Port Registers & Pinout

- The parallel port responds to five I/O instructions:
  - Two output registers (Data & Control):
    - **The output instructions transfer data into two latches (Data & Control Registers) whose outputs are presented on the pins of a 25-pin D-type female connector.**
    - Output to 278/378/3BC Hex (Data Reg): Captures data from the data bus and presents on the respective pins.
    - Output to 27A/37A/3BE Hex (Control Reg): The latch captures the least significant bits of the data bus.

	Bits	7	6	5	4	3	2	1	0
Base (e.g 378h)	Data	X	X	X	X	X	X	X	X
Base+1 (e.g 379h)	Status	-X	X	X	X	X			
Base+2 (e.g 37Ah)	Control					-X	X	-X	-X

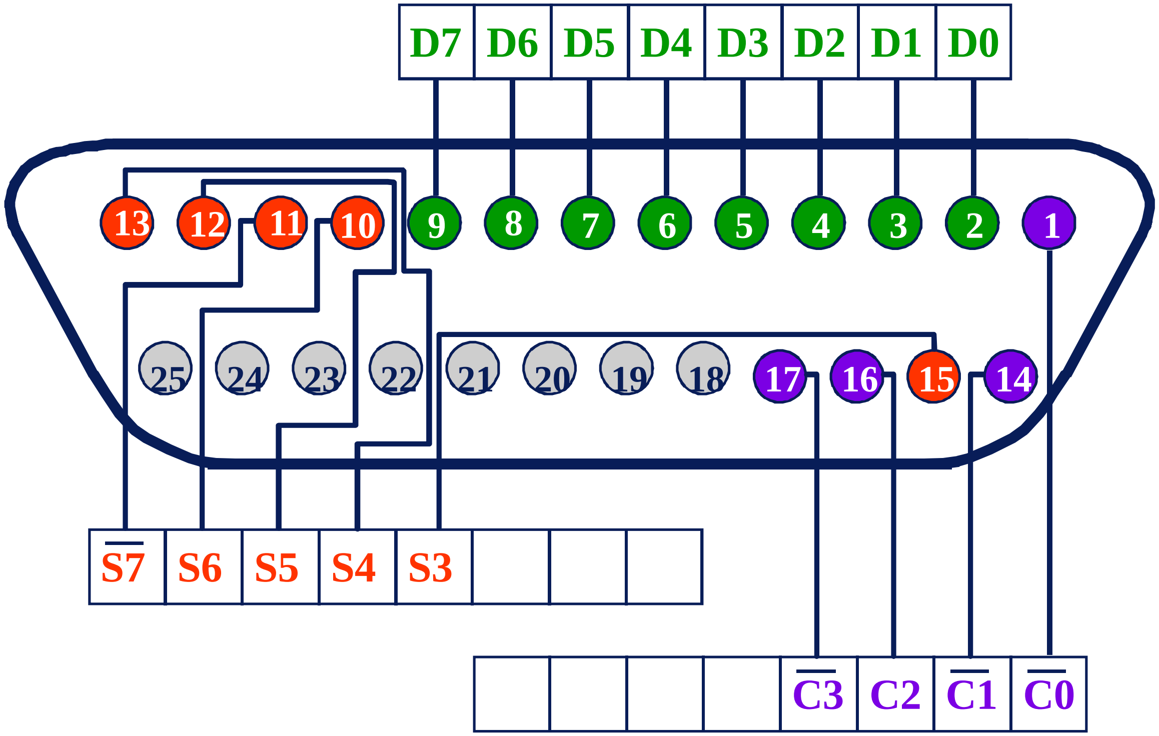
Std Parallel Port Registers & Pinout

- The parallel port responds to five I/O instructions: (cont)
  - Three input registers (Status, Data, & Control)
    - Input from 279/379/3BD Hex (Status Reg) READ ONLY: Reads the real-time status of a group of pins on the connector.
  - READS BACK the contents of the two latches:
    - Input from 278/378/3BC Hex (Data Reg): This command presents the processor with data present on the pins.
    - Input from 27A/37A/3BE Hex (Control Reg): Data on pins 1,14,16,17 and the IRQ bit to be read by CPU.

	Bits	7	6	5	4	3	2	1	0
Base (e.g 378h)	Data	X	X	X	X	X	X	X	X
Base+1 (e.g 379h)	Status	-X	X	X	X	X			
Base+2 (e.g 37Ah)	Control					-X	X	-X	-X

Parallel Port Signal Description

- I/O signals available through a 25-pin, D-type female connector.
  - Connector protrudes through the rear panel of the system.
- In IBM compatible PC, the Centronics parallel port uses a 25-pin connector in place of the original 36-pin form.
  - Sharing ground leads saved space & cost on early PC's
  - Cable length should not exceed 5 meters.



Designed as a printer port, and many of the signal names (PaperEnd, AutoLineFeed) reflect that use.

Parallel Port Signal Description

- Pin 2-9: Data 0 - Data 7 (Data Reg bit 7:0)
  - » Sends data BYTES **to** the external device on these lines.
  - » Note: These are Bi-directional on later designs and an extra bit (C5) is implemented in the Control Register.
- Pin 1: STROBE# (Data strobe - Ctrl Reg bit C0-)
  - » Control Line output that when set low (> 0.5 uS) by software (e.g writing 1 to bit C0-) causes the external device (e.g. printer) to latch the data byte on pins 2-9 (WRITE SIGNAL).
  - » Data is sent to the printer when STROBE# is asserted.
- Pin 14: AUTO FD# (Auto Feed - Ctrl Reg bit C1-)
  - » Control Line output that when set low causes the printer to advance the paper 1 line for each Carriage Return (0Dh).
    - > **Most printers give a choice on whether it just returns the printhead to beginning of line or also advances the paper.**

Parallel Port Signal Description

- Pin 16: INIT# (Initialize - Ctrl Reg bit C2+)
  - » Control Line output that when set low (> 50 uS) by software causes the printer to be initialized and placed on-line (~reset command --Clears the printers buffers).
- Pin 17: SLCTIN# (Select Printer- Ctrl Reg bit C3-)
  - » Control Line output that when set low by software causes the printer to be selected by the host computer.
  - » Many printers fix this signal internally to ground or provide a DIP switch so that the printer is always selected.
- Pin 11: Busy (Status Reg bit S7-)
  - » Status Line input set high when external device is busy and cannot accept data (stops flow of data to printer).
    - > **Don’t send any more data!**

Parallel Port Signal Description

- Pin 10: ACK# (Acknowledge - Status Reg bit S6+)
  - Status Line input set low (~0.5 uS) when external device has properly received a data byte & is ready for more data.
  - If bit C4 =1 (IRQ Enable), will interrupt CPU when ACK# transitions 1 to 0. (Used with interrupt-driven device drivers)
- Pin 12: PE (Paper End - Status Reg bit S5+)
  - Status Line input set high when external device has an “out of paper” or similar condition.
- Pin 13: SLCT (Select - Status Reg bit S4+)
  - Status Line input set high when external device has been selected (i.e. is “on-line” or ready to receive data).
- Pin 15: Error# (Status Reg bit S3-)
  - Status Line input set low when external device has encountered an error condition (e.g. printhead jammed).

Parallel Port Signal Description

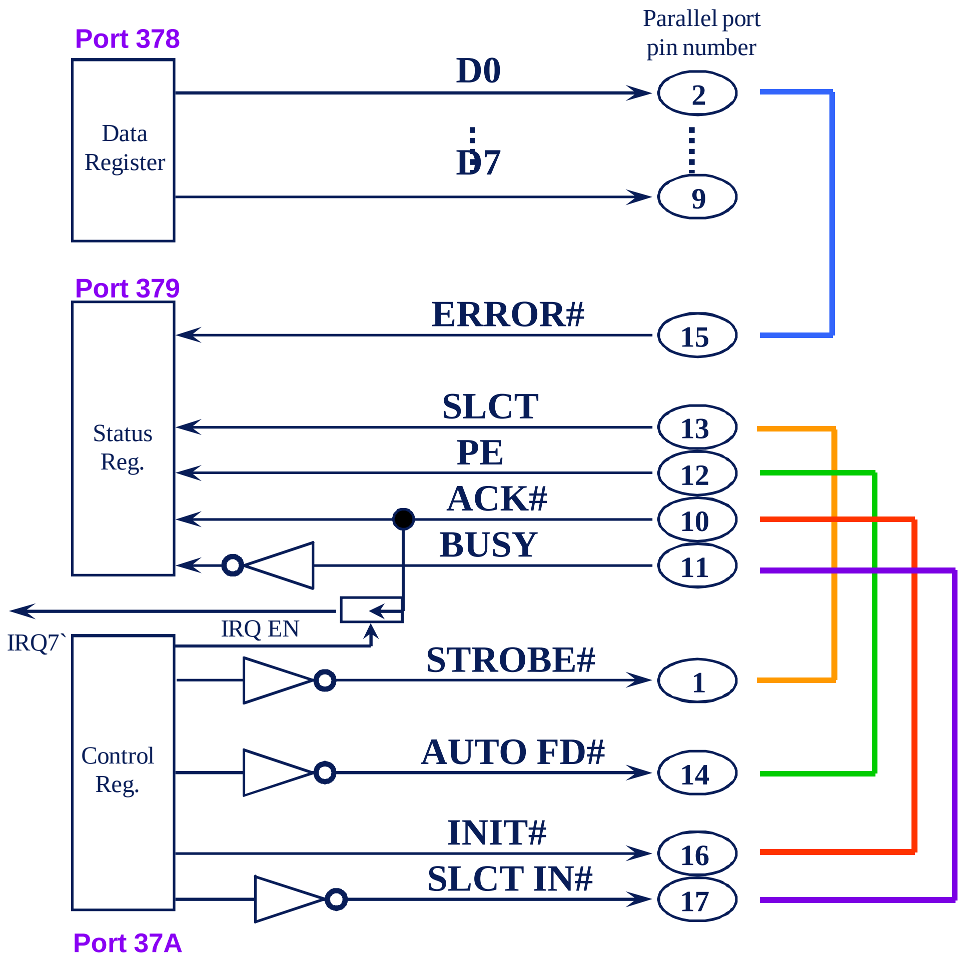
- "Compatibility mode" data transfer to a printer is limited to 40-300 Kbps due to the multiple I/O cycles required for software handshaking.
  - Write data to Data Register (e.g. 378h)
  - Read Status (e.g. 379h) to check printer not busy (-S7 = 1).
    - **e.g. - Check for BUSY Pin 11 = 0 (-S7=1).**
  - If not busy, write to Control Register (e.g 37Ah) to assert the STROBE# line (Pin 1 = 0).
    - **e.g. - Write "1" to Control Reg bit -C0 (STROBE#).**
  - Wait approx. 5 microseconds, then write to Control Register (e.g 37Ah) to deassert the STROBE# line (Pin 1 = 1).
    - **e.g. Write "0" to Control Reg bit -C0 (STROBE#).**
  - **Note: EPP & ECP ports increase throughput by using hardware instead of software to check Busy & Strobe.**

Parallel Port Loopbacks & Testing

- A PASSIVE LOOPBACK CONNECTOR is a connector on which some of the output pins have been wire connected to some of the input pins so that when placed on the board's parallel port connector, data sent out is received back by the same port.
  - Note: Some tests also require an active loopback (has an ASIC that interfaces a DRAM chip to the parallel port) and can operate in the parallel port's compatible, PS/2, EPP and ECP modes.
    - **The circuit has two parts, the IFICS ID and memory.**
      - **The memory section is used for writing and reading data in selected modes.**
      - **These tests transfer a block of data to DRAM and reads it back in each supported mode of operation.**

Parallel Port Loopbacks & Testing

A common parallel loopback is a male 25-pin D-sub connector with the following pins wired together:



PRTD0 (pin 2) - (pin 15) ERROR#:

- Reg D0 to S3

STROBE# (pin 1) - (pin 13) SLCT:

- Reg -C0 to S4

AUTOFD#(pin 14) - (pin 12) PE:

- Reg -C1 to S5

INIT# (pin 16) - (pin 10) ACK#:

- Reg C2 to S6

SLCTIN# (pin 17) - (pin 11) BUSY:

- Reg -C3 to -S7

Parallel Port Loopbacks & Testing

- If write 01 to 378h & 0C to 37Ah, then read FF at port 379
  - 0000 0001 and 0000 1100 -> 1111 1111
- If write 00 to 378h & 03 to 37Ah , then read 07 at port 379
  - 0000 0000 and 0000 0011 -> 0000 0111

		7	6	5	4	3	2	1	0
Port 378	**Data**	X	X	X	X	X	X	X	X
Port 379	**Status**	-X	X	X	X	X	-	-	-
Port 37A	**Control**	-	-	-	-	-X	X	-X	-X

PRTD0 (pin 2) - (pin 15) ERROR: Reg D0 to S3

STROBE (pin 1) - (pin 13) SLCT: Reg -C0 to S4

AUTOFD (pin 14) - (pin 12) PE: Reg -C1 to S5

INIT (pin 16) - (pin 10) ACK: Reg C2 to S6

SLCTIN (pin 17) - (pin 11) BUSY: Reg -C3 to -S7

Parallel Port Loopbacks & Testing

- A more thorough loopback connector can test all 17 input & output lines of the port at the same time.
  - An example of such a loopback would have the following pins wired together:
    - **PRTD0 (pin 2) - (pin 1) STROBE***
    - **PRTD1 (pin 3) - (pin 10) ACK***
    - **PRTD2 (pin 4) - (pin 11) BUSY**
    - **PRTD3 (pin 5) - (pin 12) PE**
    - **PRTD4 (pin 6) - (pin 13) SLCT**
    - **PRTD5 (pin 7) - (pin 14) AUTOFD***
    - **PRTD6 (pin 8) - (pin 15) ERROR* and (pin 17) SLCTIN***
    - **PRTD7 (pin 9) - (pin 16) INIT***

Parallel Port Loopbacks & Testing

- The IFICS loopback is a small PC board attached to the LPT (printer) port of the UUT.
  - The IFICS cable/board assembly is a factory test assembly containing active components and jumpers.
- The purpose of the IFICS Loopback is to identify the station ID.
  - Test software will read jumper information and report it.
  - The jumpers are set to unique addresses within the same server.
    - » IFICS ID setting: There are 8 bit settings, each bit is either a high or a low. The default is a high if a jumper is not used.
  - Note: The IFICS loopback connector is required for the Display IFICS Loopback Value utility.

Parallel Port - Security keys

- Security keys, or dongles, are a form of copy protection that often uses the parallel port.
  - ➢Some software (usually expensive, specialized applications) includes a security key that you must plug into the parallel port in order to run the software.
  - ➢This key is a small device with a male D-sub connector on one end, and a female D-sub on the other end (to connect the printer) which may contain active devices.
  - ➢The software communicates with the key, which contains a code that the software recognizes and the key usually doesn’t use any conventional handshaking signals.
    - » The copy protection software writes various patterns to the data lines without ever pulsing the Strobe# line so the printer should ignore the data passed through.

Parallel Port BIOS Support

- Parallel port support by the ROM BIOS is limited.
  - Call INT 17h with AH=0 to print a character.
    - **AL= Character, DX = Printer to be used (0-2)**
    - **BIOS maintains a time-out counter for each printer port.**
      - Times out if the character cannot be written.
  - Call INT 17h with AH=1 to initialize the printer.
    - **Writes 0Ch to the Ctrl Reg - Asserts SLCT_IN# & INIT#**
    - **Reads the Status Registers.**
  - Call INT 17h with AH=2 to get printer port status.
    - **e.g. Error (Parallel pin 15 - ERROR*)**
    - **e.g. Printer selected/on-line (Parallel pin 13 - SLCT)**

Parallel Port BIOS Support

- IRQ7 (LPT1) or IRQ5 (LPT2): May be generated to indicate when the printer becomes ready.
  - Many printers do not generate this interrupt, and it's usually not enabled.
  - Historically there is no ROM BIOS support for hardware interrupt-driven parallel support operation, but some O/Ss & Parallel Port transfer programs use it.
    - Note that the 8259 PIC itself generates an interrupt corresponding to IRQ7 for spurious/phantom Interrupts.
      - The PIC returns the Type code for IRQ7 (Type 0Fh) if a noise spike or error caused the interrupt (IRQ input did not stay high until after the first INTA cycle).
      - IRQ7 ISR should check if bit 7 is set in the PIC In Service Reg to see if it is real interrupt or a phantom interrupt.
      - If a phantom interrupt, the ISR just executes a return.

Enhanced Ports - IEEE 1284 Standard

- The *"IEEE Std. 1284-1994 Standard Signaling Method for a Bi-directional Parallel Peripheral Interface for Personal Computers"* is fully backward compatible with all existing parallel port peripherals and printers.
  - *IEEE Std. 1284* provides for high speed bi-directional communication between the PC and an external peripheral that can communicate 50-100 times faster that the original parallel port.
  - The 1284 standard defines 5 modes of data transfer (Compatibly, Nibble, Byte, EPP, & ECP)
    - Each mode provides a method of transferring data in either the forward direction (PC to peripheral), reverse direction (peripheral to PC) or Bi-directional data transfer (half duplex).

Enhanced Ports - IEEE 1284 Standard

- **IEEE 1284 modes - Forward direction only:**
  - **1) Compatibility Mode:** "Centronics" or standard mode
    - » **It is commonly called the "Centronics" mode and is the method utilized with the SPP (Standard Parallel Port).**
    - » **This mode defines the protocol used by most PCs to transfer data to a printer.**
      - > **This mode provides backward compatibility with the huge base of installed printers and peripherals.**
    - » **The bandwidth capabilities of the port (~150K bytes per second) is sufficient for communicating with dot matrix and many older laser printers, but is a limitation when communicating with removable disk drives, the newest generation of laser printers, etc.**

Enhanced Ports - IEEE 1284 Standard

- **IEEE 1284 modes - Reverse direction only**:
  - **2) Nibble Mode:**.
    - **Transfers 4 bits at a time (a nibble) using <u>Status Lines</u> for data.**
      - **Busy (D3,D7); PE (D2,D6); Select (D1,D5); Error (D0,D4)**
      - **To send an entire byte to the PC, 2 cycles are required using the Nibble mode.**
    - **The Nibble mode is the most common way to get reverse channel data from a printer or peripheral.**
      - **Transfer rates ~ 50K bytes per second (SLOWEST).**
    - **The bits are not conveniently packed into the byte defined in the Status Register, so software must manipulate the bits.**

Enhanced Ports - IEEE 1284 Standard

- **IEEE 1284 modes - Bi-directional**
  - **3) Byte Mode:** 8 bits at a time using data lines.
    - **Added the capability to disable the drivers used for driving the data lines, and allowed the data port to become an input read data port.**
      - **Control Reg Bit C5 added to determine direction. When C5=1, the data port is effectively an input port.**
    - **Enables a peripheral to send an entire byte <u>to the PC</u> in one data transfer cycle using 8 data lines, rather than the 2 cycles required using the Nibble mode.**
    - **Introduced on IBM PS/2 -- "PS/2-type" has come to refer to any parallel port that has a bi-directional data port but doesn't support EPP/ECP modes.**

Enhanced Ports - IEEE 1284 Standard

- **IEEE 1284 modes - Bi-directional**
  - **4) EPP: Enhanced Parallel Port** - used primarily by non-printer peripherals: CD ROM, tape drives, etc.
    - **Developed by Intel, Zenith, & Xircom in 1991.**
    - **Implemented with special hardware on the motherboard**
    - **EPP adds 5 regs at <u>base addr+ 3</u> through <u>base addr+7</u>.**
      - **The first 3 registers are exactly the same as the SPP Regs.**
      - **For a base address of 378h, EPP registers at 37Bh-37Fh**
        - **Base + 3 = Address Port; Base + 4 = Data Port**
    - **EPP mode allows multiple peripherals on the same port.**
      - **Tailored to support portable PC peripherals: hard disks, tape backup units, CD-ROM drives, network adapters, etc.**
      - **EPP is effectively an extension of the system bus.**

Enhanced Ports - IEEE 1284 Standard

- **IEEE 1284 modes - Bi-directional**
  - **4) EPP: Enhanced Parallel Port** - (Cont.)
    - **An EPP can switch directions quickly, and is efficient when used devices that transfer data in both directions.**
      - **The pins function according to the EPP protocol.**
    - **The ability to use a single instruction to transfer data enables EPP mode to transfer data at ISA bus speeds.**
      - **Transfer rates from 500K to 2M bytes per second.**
      - **The handshaking for EPP is performed by hardware so that data is transferred in a single I/O cycle.**
      - Originally slower software handshaking was used for parallel ports (read busy bit , write strobe bit, etc)
    - **EPP mode may use interrupts.**
    - **An EPP can also emulate an SPP.**

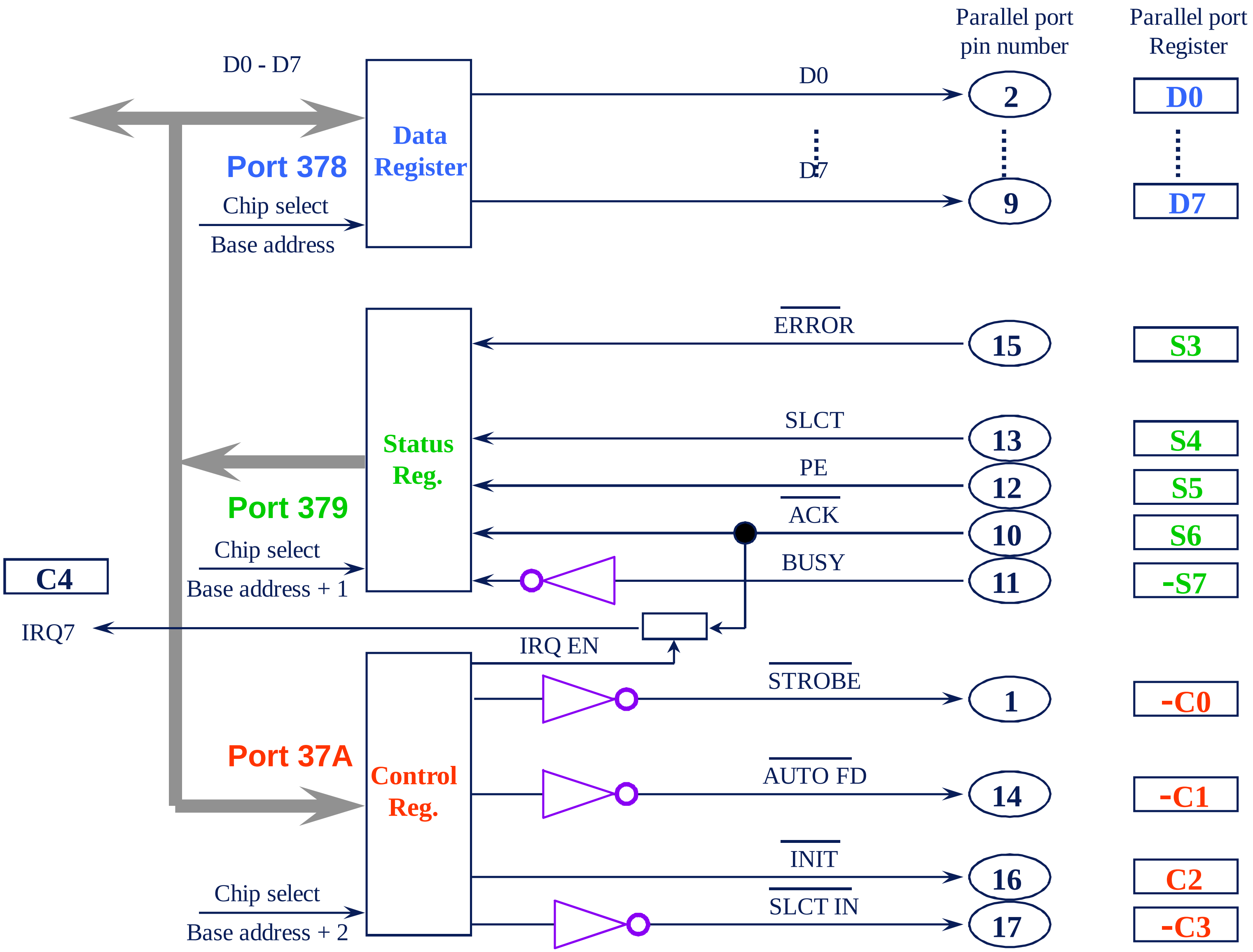
Enhanced Ports - IEEE 1284 Standard

- **IEEE 1284 modes - Bi-directional:**
  - **5) ECP: Extended Capability Port** - used primarily by the new generation of printers/scanners and other peripherals that transfer large bi-directional data blocks.
    - **Developed by Microsoft & HP in 1992.**
    - **Special hardware implements ECP on the motherboard.**
      - **The ECP is backwards compatible to the SPP and EPP**
    - **The first 3 registers are the same as the SPP Regs.**
    - **ECP adds 3 registers at base addr+400h through base addr+402h (uses A10 address line).**
      - **For base address 378h, ECP registers are at 778h-77Ah.**
      - **"Aliasing" expands the number of registers available, and still maintains compatibility with older ISA cards that only decode 10 address bits (A0-A9).**

Enhanced Ports - IEEE 1284 Standard

- **IEEE 1284 modes - Bi-directional:**
  - **5) ECP: Extended Capability Port** - (Cont.)
    - » **The ECP is bi-directional, can transfer data at ISA-bus speeds, has buffers, and supports DMA transfers.**
      - > **ECP is meant to be driven by DMA rather than use explicit I/O instructions like EPP (e.g. DMA Channel 3)**
      - > **ECP handshake is controlled by hardware not software.**
      - > **ECP mode may use interrupts (e.g. IRQ 7).**
    - » **ECP “channel addressing” accesses multiple logical devices within a single physical device such as a fax/printer/modem.**
      - > **e.g.- Could receive data from the modem data device while the printer data channel is busy processing a print image.**
    - » **Other features of ECP are a 16-byte FIFO and real time data compression up to 64:1.**

REVIEW & SUMMARY



REVIEW & SUMMARY

- **Functions of Standard & Bi-directional Parallel Ports.**
  - ➢Contains no intelligence and is just a set of latches and buffers together with some address decoding circuitry.
  - ➢Software outputs instructions to set & reset bits in the latches--these are used to generate all control signals.
  - ➢The parallel port in the original IBM PC is sometimes called the SPP, for **S**tandard **P**arallel **P**ort.
- **Parallel Port I/O addresses.**
  - » 278h or 378h or 3BCh Base Addresses.
  - ➢The 1st address (e.g. 378h) is the port's base address, also called the Data register or just the port address.
  - ➢The 2nd address (e.g. 379h) is the port's Status register.
  - ➢The 3rd address (e.g. 37Ah) is the Control register.

REVIEW & SUMMARY

- **Standard Parallel Port registers & connector signals.**
  - Two output registers
    - Output to 278/378/3BC Hex (Data Reg)
    - Output to 27A/37A/3BE Hex (Control Reg)
  - Three input registers
    - Input from 279/379/3BD Hex (Status Reg) READ ONLY
    - Input from 278/378/3BC Hex (Data Reg) READ BACK
    - Input from 27A/37A/3BE Hex (Control Reg) READ BACK
  - I/O available through a 25-pin, D-type female connector.
- **The use of loopbacks for testing the SPP.**
  - Passive Loopback: Connector on which some output pins have been wire connected to some input pins.

REVIEW & SUMMARY

- **Parallel Port BIOS support.**
  - INT 17h: AH=0 to print a character; AH=1 to initialize the printer; AH=2 to get printer port status.
- **IEEE-1284 standard & EPP/ECP Bi-directional modes.**
  - Compatibility Mode: "Centronics" or standard mode.
  - Nibble Mode: 4 bits at a time using <u>status lines</u> for data.
  - Byte Mode: 8 bits at a time using <u>data lines</u>.
  - EPP: Enhanced Parallel Port - used primarily by non-printer peripherals: CD ROM, tape drives, etc.
  - ECP: Extended Capability Port - used primarily by the new generation of printers/scanners and other peripherals that transfer large bi-directional data blocks.