MOS Layer
MOS Layer

• MOS design is aimed at turning a specification into masks for processing silicon to meet the specification.

• We have seen that MOS circuits are formed on four basic layers-n-diffusion, p-diffusion, polysilicon, and metal, which are isolated from one another by thick or thin (thinox) silicon dioxide insulating layers.
Mask Layout (Print this presentation in colour if possible, otherwise highlight colours)

- Circuit coloured mask layer layout
- Coloured stick diagram mask representation
- Lambda and layout design rules
- Mask layout of nMOS and CMOS inverters
- Mask layout of CMOS circuits (examples)
- Reading & understanding mask layout (exercises)
nMOS transistor mask representation
Mask layout & coloured stick diagram notation

Silicon layers are typically colour coded as follows:

- Green: diffusion (device well, local interconnect)
- Red: polysilicon (gate electrode, interconnect)
- Dark red: metal (contact, interconnect)
- Black: contact windows
- Yellow: depletion implant
- Orange: P well (CMOS devices)

This colour representation is used during mask layer definition.

Translation from circuit format to a mask layout (and vice-versa) is relatively straightforward.
A transistor is formed when device well is crossed by polysilicon. Device well oxide: thin gate oxide

- Metal contacting polysilicon
- Metal contacting diffusion
- Metal crossing polysilicon (no contact, electrically isolated with thick oxide and so can carry separate voltages)
- Metal contacting diffusion (no contact, electrically isolated with thick oxide)

Legend:
- Green: diffusion
- Red: polysilicon
- Brown: metal
- Gray: contact windows
- Yellow: depletion implant
- Orange: P well
A transistor is formed when device well is crossed by polysilicon. Device well oxide: thin gate oxide

Enhancement mode transistor ($V_{th} \approx 0.2V_{dd}$)

Depletion mode transistor (extra well implant to provide $V_{th} \approx -0.6V_{dd}$)
CMOS Inverter Mask Layout (using Microwind)

Use file>colors>white background
CMOS AN2 (2 i/p AND gate) Mask Layout

diffusion
polysilicon
metal
contact windows
depletion implant
P well
Layout Design rules & Lambda ($\lambda$)

**Lambda ($\lambda$):** distance by which a geometrical feature or any one layer may stay from any other geometrical feature on the same layer or any other layer. All processing factors are included plus a safety margin.

$\lambda$ used to prevent IC manufacturing problems due to mask misalignment or exposure & development variations on every feature, which otherwise could lead to:
- over-diffusion
- over-etching
- inadvertent transistor creation etc

$\lambda$ is the minimum dimension which can be accurately re-produced on the silicon wafer for a particular technology.
Layout Design rules & Lambda (\(\lambda\))

Minimum photolithographic dimension (width, not separation) is \(2\lambda\).
Hence, the minimum channel length dimension is \(2\lambda\).
Where a 0.25\(\mu\)m gate length is quoted, \(\lambda\) is 0.125 microns (\(\mu\)m).

Minimum distance rules between device layers, e.g.,
- polysilicon \(\leftrightarrow\) metal
- metal \(\leftrightarrow\) metal
- diffusion \(\leftrightarrow\) diffusion and
- minimum layer overlaps
are used during layout

Layout design rule checker (DRC) automatically verifies that no design rules have been broken

*Note however, the use of Lambda is not optimal but supports* design reuse
Lambda based design: half of technology since 1985. As technology changes with smaller dimensions, a simple change in the value of \( \lambda \) can be used to produce a new mask set.

Hcmos6 technology: \( \lambda = 0.2 \mu m \)
Hcmos8 technology: \( \lambda = 0.1 \mu m \)

All device mask dimensions are based on multiples of \( \lambda \), e.g., polysilicon minimum width = 2\( \lambda \). Minimum metal to metal spacing = 3\( \lambda \).
Basic design rules

- Minimize spared diffusion
- Use minimum poly width (2λ)

- 1 contact = 1mA
- Multiply contacts

2mA
Basic design rules

- Width of pMOS should be twice the width of nMOS
- Same N and P alters symmetry
- \( L_{min} \)
- \( W_{pmos} = 2 \cdot W_{nmos} \)
nMOS transistor mask representation (See stick diagram next slide) for comparison

drain

gate

source

diffusion (active region)

polysilicon

metal

Contact holes
nMOS transistor coloured stick diagram representation

- polysilicon
- metal
- Contact holes
- diffusion (active region)

Legend:
- green: diffusion
- red: polysilicon
- dark red: metal
- grey: contact windows
- yellow: depletion implant
- brown: P well
For reference: an nMOS Inverter coloured stick diagram

*Note the depletion mode device*

$V_{dd} = 5V$

$V_{gs}^{pu} = 0$ (always)

$V_{in}$

$V_{out}$

$V_{th}^{pu} \approx -3V$ ($T_{pu}$ always on since $V_{gs}=0$)

$T_{pu}$

$V_{th}^{pd} \approx +1V$ (enhancement mode device, off at 0V)

$T_{pd}$

$V_{in}$
CMOS Inverter Mask Layout
CMOS Inverter Mask Layout

Simplify by deleting connections provided for interconnecting cell (additional pads and output metal rails)
CMOS Inverter coloured stick diagram
Stick diagram -> CMOS transistor circuit

In practice, first draw stick diagram for nMOS section and analyse (pMOS is dual of nMOS section)
Static CMOS NAND gate

1. Pull-down: Connect to ground if $A=1$ AND $B=1$

2. Pull-up: Connect to Vdd if $A=0$ OR $B=0$
Static CMOS NOR gate

1. Pull-down: Connect to ground if \( A=1 \) OR \( B=1 \)
2. Pull-up: Connect to \( \text{Vdd} \) if \( A=0 \) AND \( B=0 \)
Static CMOS Design Example Layout

Example: \( f = \overline{a \cdot b} + c \)
Layout 2 (Different layout style to previous but same function being implemented)

Example: $f = a \cdot b + c$
Steps in translating from layout to logic circuit

1. Try to simplify mask layout diagram by removal of extended metal and polysilicon lines

2. First draw coloured stick diagram for nMOS section and analyse
   All nMOS transistor nodes which connect to GND terminal are SOURCE nodes

3. Since the pMOS section is the dual of the nMOS section, draw the pMOS stick diagram and confirm the outcome of step 2.
   All pMOS transistor nodes which connect to Vdd terminal are pMOS SOURCE nodes
Exercise: Draw coloured stick diagram and logic circuit for this CMOS mask layout
Layout Design Rule

$\lambda = 1 \mu m$

### MINIMUM WIDTH AND SPACING RULES

<table>
<thead>
<tr>
<th>LAYER</th>
<th>TYPE OF RULE</th>
<th>VALUE</th>
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<tbody>
<tr>
<td>POLY</td>
<td>Minimum Width</td>
<td>2$\lambda$</td>
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<tr>
<td></td>
<td>Minimum Spacing</td>
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<tr>
<td>ACTIVE</td>
<td>Minimum Width</td>
<td>3$\lambda$</td>
</tr>
<tr>
<td></td>
<td>Minimum Spacing</td>
<td>3$\lambda$</td>
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<tr>
<td>NSELECT</td>
<td>Minimum Width</td>
<td>3$\lambda$</td>
</tr>
<tr>
<td></td>
<td>Minimum Spacing</td>
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<tr>
<td>PSELECT</td>
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<td></td>
<td>Minimum Spacing</td>
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</tr>
<tr>
<td>METAL1</td>
<td>Minimum Width</td>
<td>3$\lambda$</td>
</tr>
<tr>
<td></td>
<td>Minimum Spacing</td>
<td>3$\lambda$</td>
</tr>
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### MOSFET LAYOUT RULES

<table>
<thead>
<tr>
<th>RULE</th>
<th>MEANING</th>
<th>VALUE</th>
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<tbody>
<tr>
<td>POLY Overlap</td>
<td>Minimum extension over ACTIVE</td>
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</tr>
<tr>
<td>POLY-ACTIVE</td>
<td>Minimum Spacing</td>
<td>1$\lambda$</td>
</tr>
<tr>
<td>MOSFET Width</td>
<td>Minimum N+/P+ MOSFET W</td>
<td>3$\lambda$</td>
</tr>
<tr>
<td>ACTIVE CONTACT</td>
<td>Exact Size</td>
<td>2$\lambda \times 2\lambda$</td>
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<tr>
<td></td>
<td>Minimum Space to ACTIVE Edge</td>
<td>2$\lambda$</td>
</tr>
<tr>
<td>POLY CONTACT</td>
<td>Exact Size</td>
<td>2$\lambda \times 2\lambda$</td>
</tr>
<tr>
<td></td>
<td>Minimum Space to POLY Edge</td>
<td>2$\lambda$</td>
</tr>
</tbody>
</table>
Double metal single poly CMOS Process

**FIGURE B.1(D)** Rules for n-well (Orbit 1.2 μm CMOS process).