

**ECE Department**  
**Virtual Lab Experiments**

LINK: [www.vlab.co.in](http://www.vlab.co.in)

**Sem :IV ECE**

**Lab:Digital Electronics**

**Lab under Virtual Portal: Digital Electronics, IIT H**

<b>S.No</b>	<b>Experiment</b>	<b>Virtual Lab Link</b>
1	Verification of state tables of RS,JK and D flip flops using NAND & NOR gates.	<a href="http://deploy.virtual-labs.ac.in/labs/cse15/exp6/index.php">http://deploy.virtual-labs.ac.in/labs/cse15/exp6/index.php</a>
2	Implementation of 4*1 multiplexer using logic gates.	<a href="http://deploy.virtual-labs.ac.in/labs/cse15/exp2/index.php">http://deploy.virtual-labs.ac.in/labs/cse15/exp2/index.php</a>
3	Design and verify the 4 bit asynchronous counter.	<a href="http://deploy.virtual-labs.ac.in/labs/cse15/exp8/index.php?section=Theory">http://deploy.virtual-labs.ac.in/labs/cse15/exp8/index.php?section=Theory</a>
4	To design and verify operation of half adder and full adder.	<a href="http://deploy.virtual-labs.ac.in/labs/cse15/exp1/index.php">http://deploy.virtual-labs.ac.in/labs/cse15/exp1/index.php</a>
5	To design and verify operation of magnitude comparator.	<a href="http://deploy.virtual-labs.ac.in/labs/cse15/exp5/index.php">http://deploy.virtual-labs.ac.in/labs/cse15/exp5/index.php</a>