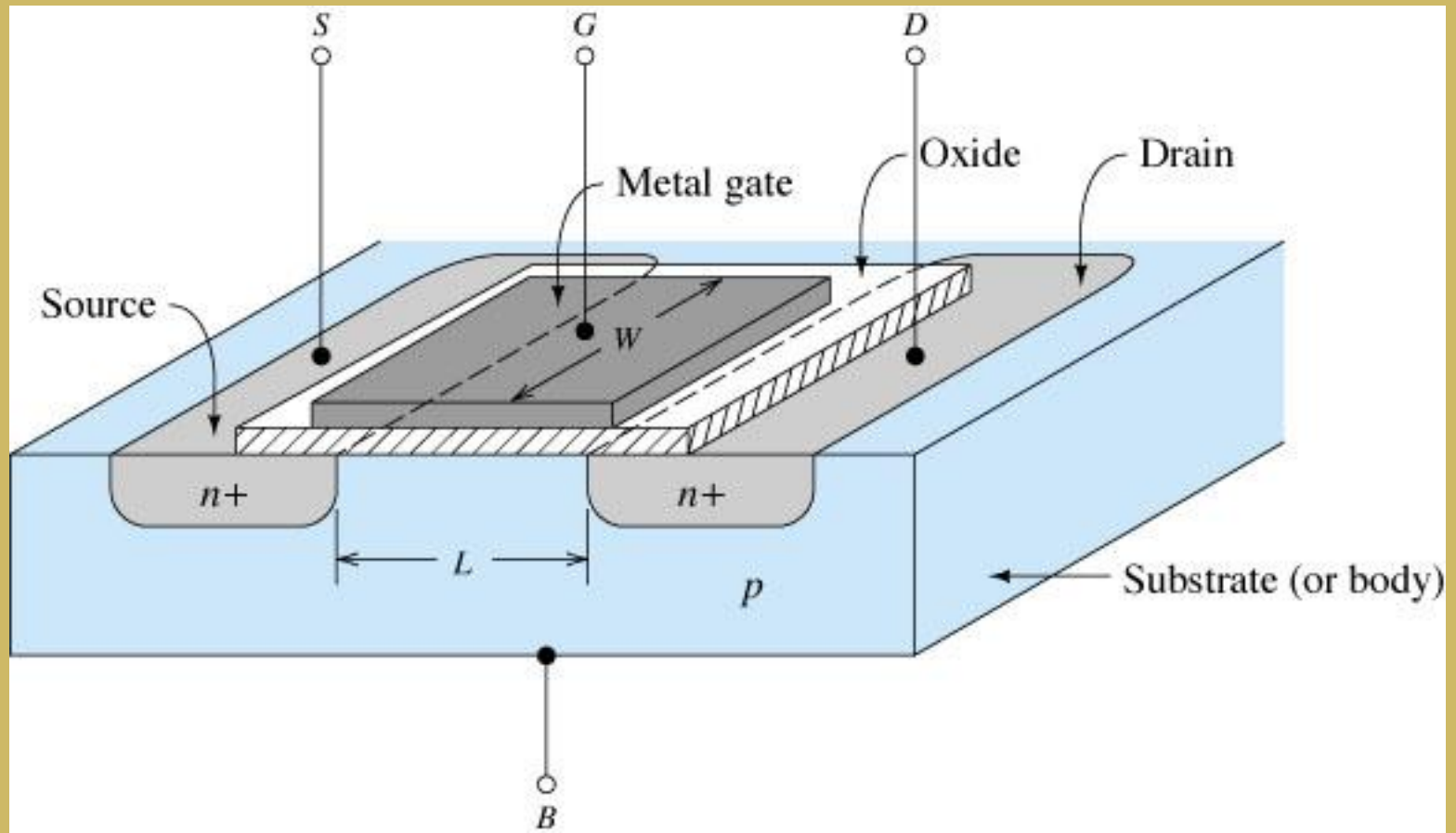


# **ANALOG ELECTRONICS**

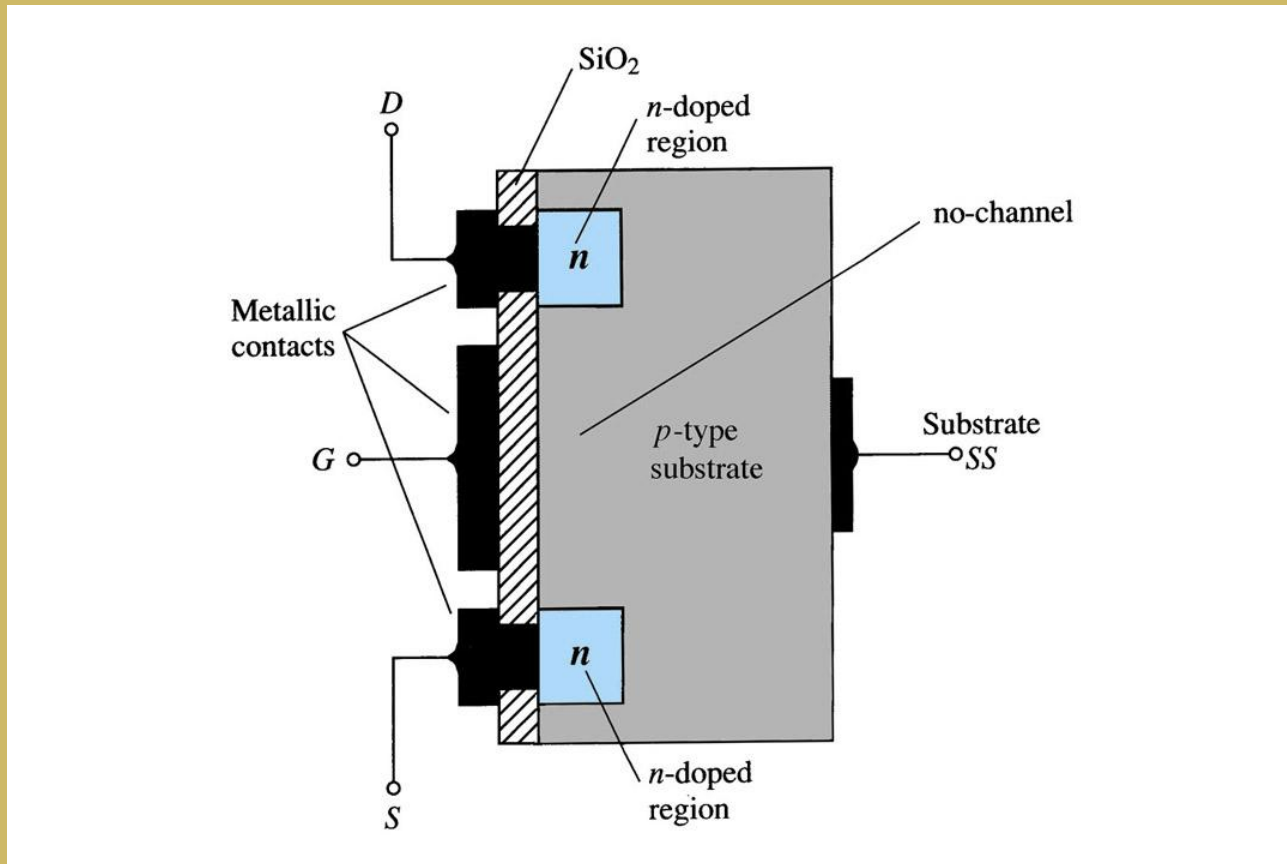
LECTURE NO. 10

# ENHANCEMENT MODE MOSFET'S

***n*-Channel E-MOSFET showing channel length  $L$  and channel width  $W$**



## Enhancement Mode MOSFET Construction



The Drain (D) and Source (S) connect to the two n-doped regions

These n-doped regions are not connected via an n-channel without an external voltage

The Gate (G) connects to the *p*-doped substrate via a thin insulating layer of  $\text{SiO}_2$

The n-doped material lies on a *p*-doped substrate that may have an additional terminal connection called SS

# Specification Sheet

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	25	Vdc
Drain-Gate Voltage	$V_{DG}$	30	Vdc
Gate-Source Voltage*	$V_{GS}$	30	Vdc
Drain Current	$I_D$	30	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300 1.7	mW mW/°C
Junction Temperature Range	$T_J$	175	°C
Storage Temperature Range	$T_{stg}$	-65 to +175	°C

\* Transient potentials of  $\pm 75$  Volt will not cause gate-oxide failure.

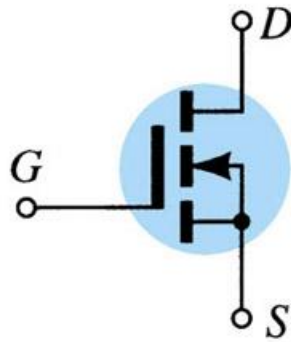
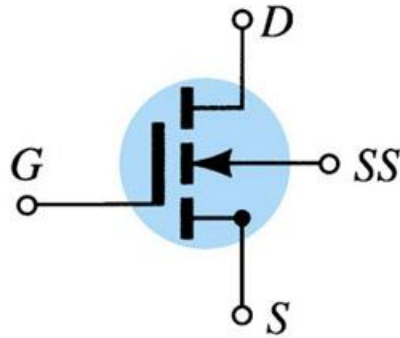
## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Drain-Source Breakdown Voltage ( $I_D = 10 \mu\text{A}$ , $V_{GS} = 0$ )	$V_{(BR)DSX}$	25	-	Vdc	
Zero-Gate-Voltage Drain Current ( $V_{DS} = 10 \text{V}$ , $V_{GS} = 0$ ) $T_A = 25^\circ\text{C}$ $T_A = 150^\circ\text{C}$	$I_{DSS}$	-	10 10	nAdc $\mu\text{Adc}$	
Gate Reverse Current ( $V_{GS} = \pm 15 \text{Vdc}$ , $V_{DS} = 0$ )	$I_{GSS}$	-	$\pm 10$	pAdc	
<b>ON CHARACTERISTICS</b>					
Gate Threshold Voltage ( $V_{DS} = 10 \text{V}$ , $I_D = 10 \mu\text{A}$ )	$V_{GS(TH)}$	1.0	5	Vdc	
Drain-Source On-Voltage ( $I_D = 2.0 \text{mA}$ , $V_{GS} = 10\text{V}$ )	$V_{DS(on)}$	-	1.0	V	
On-State Drain Current ( $V_{GS} = 10 \text{V}$ , $V_{DS} = 10 \text{V}$ )	$I_{D(on)}$	3.0	-	mAdc	
<b>SMALL-SIGNAL CHARACTERISTICS</b>					
Forward Transfer Admittance ( $V_{DS} = 10 \text{V}$ , $I_D = 2.0 \text{mA}$ , $f = 1.0 \text{kHz}$ )	$ y_{fs} $	1000	-	$\mu\text{mho}$	
Input Capacitance ( $V_{DS} = 10 \text{V}$ , $V_{GS} = 0$ , $f = 140 \text{kHz}$ )	$C_{iss}$	-	5.0	pF	
Reverse Transfer Capacitance ( $V_{DS} = 0$ , $V_{GS} = 0$ , $f = 140 \text{kHz}$ )	$C_{rs}$	-	1.3	pF	
Drain-Substrate Capacitance ( $V_{DGS(B)}$ = 10 V, $f = 140 \text{kHz}$ )	$C_{d(sub)}$	-	5.0	pF	
Drain-Source Resistance ( $V_{GS} = 10 \text{V}$ , $I_D = 0$ , $f = 1.0 \text{kHz}$ )	$r_{d(sos)}$	-	300	ohms	
<b>SWITCHING CHARACTERISTICS</b>					
Turn-On Delay (Fig. 5)	$I_D = 2.0 \text{mAdc}$ , $V_{DS} = 10 \text{Vdc}$ , ( $V_{GS} = 10 \text{Vdc}$ ) (See Figure 9; Times Circuit Determined)	$t_{d1}$	-	45	ns
Rise Time (Fig. 6)		$t_r$	-	65	ns
Turn-Off Delay (Fig. 7)		$t_{d2}$	-	60	ns
Fall Time (Fig. 8)		$t_f$	-	100	ns



## E-MOSFET Symbols

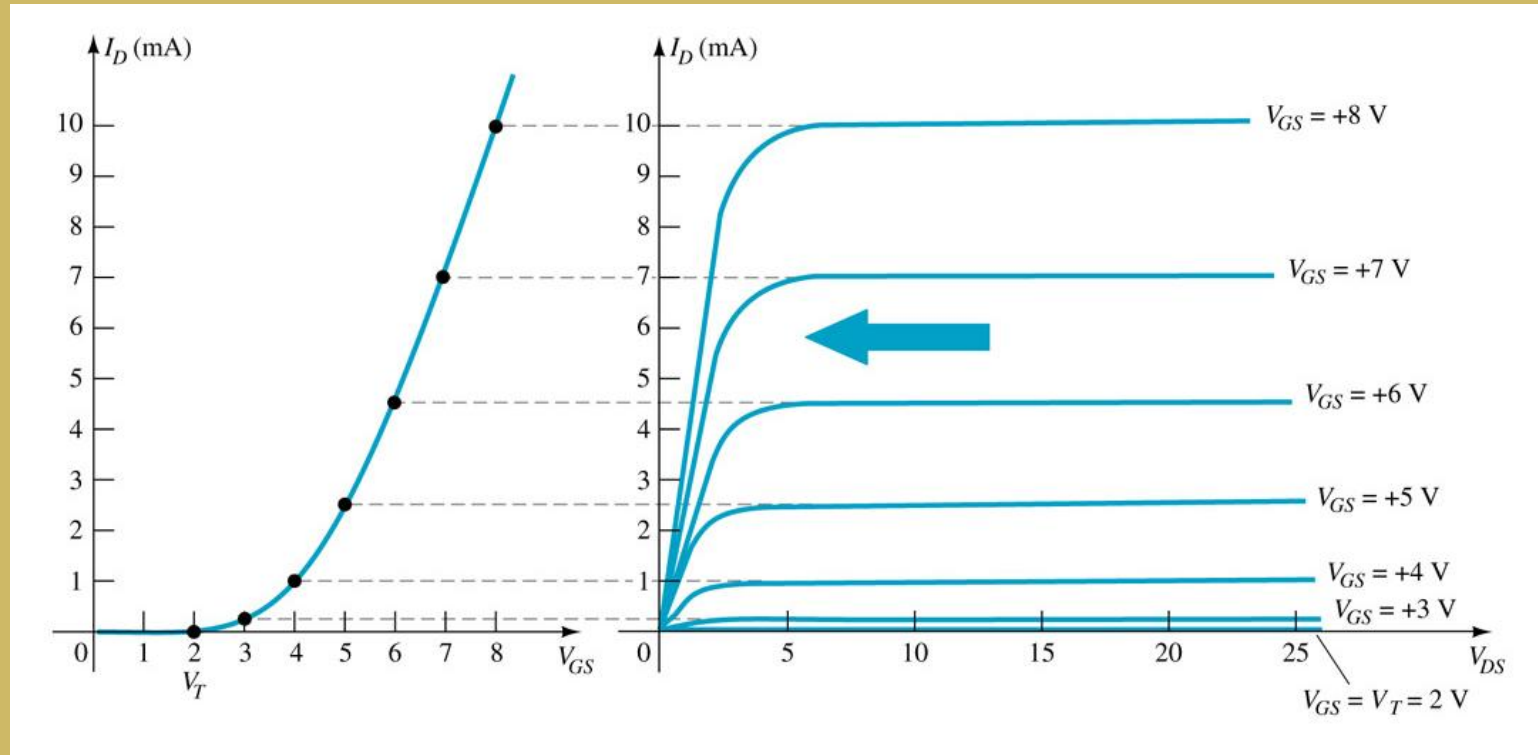
*n*-channel



(a)

## Basic Operation

The Enhancement mode MOSFET only operates in the enhancement mode.



$V_{GS}$  is always positive

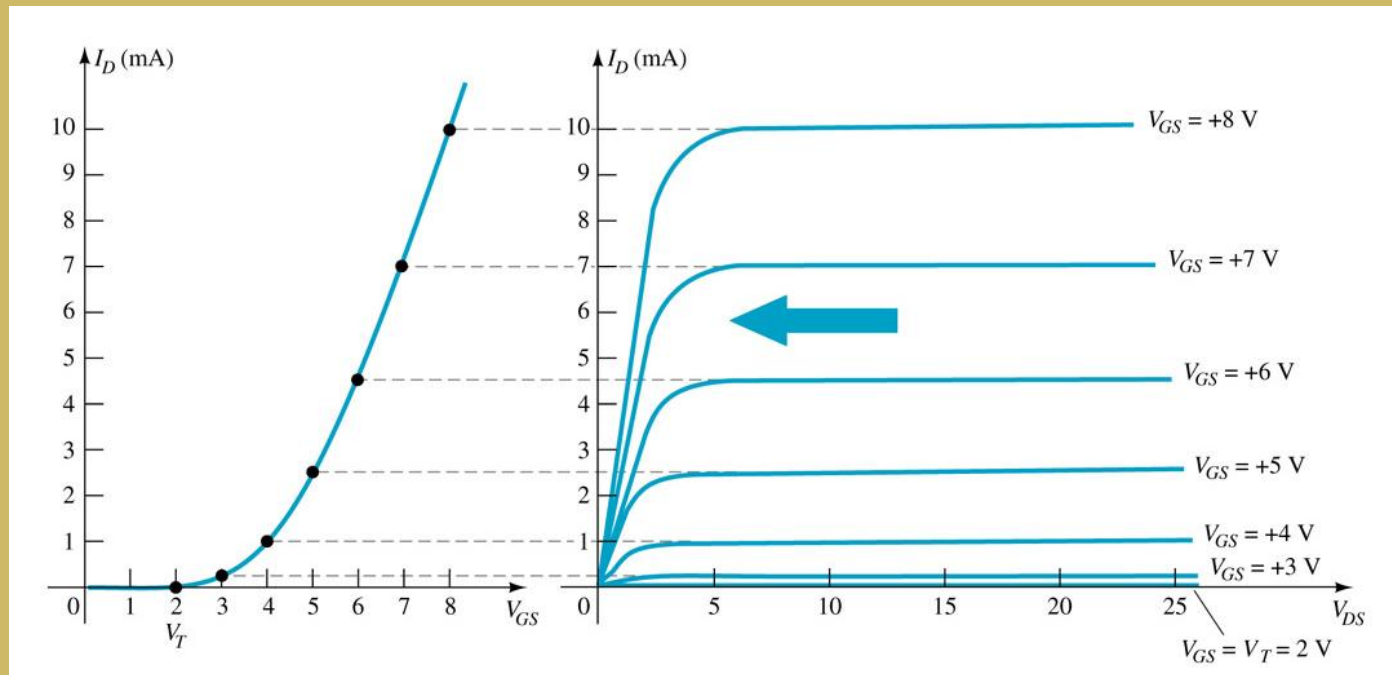
$I_{DSS} = 0$  when  $V_{GS} < V_T$

As  $V_{GS}$  increases above  $V_T$ ,  $I_D$  increases

If  $V_{GS}$  is kept constant and  $V_{DS}$  is increased, then  $I_D$  saturates ( $I_{DSS}$ )

The saturation level,  $V_{DSsat}$  is reached.

## Transfer Curve



To determine  $I_D$  given  $V_{GS}$ :  $I_D = k (V_{GS} - V_T)^2$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

where  $V_T$  = threshold voltage or voltage at which the MOSFET turns on.

$k$  = constant found in the specification sheet

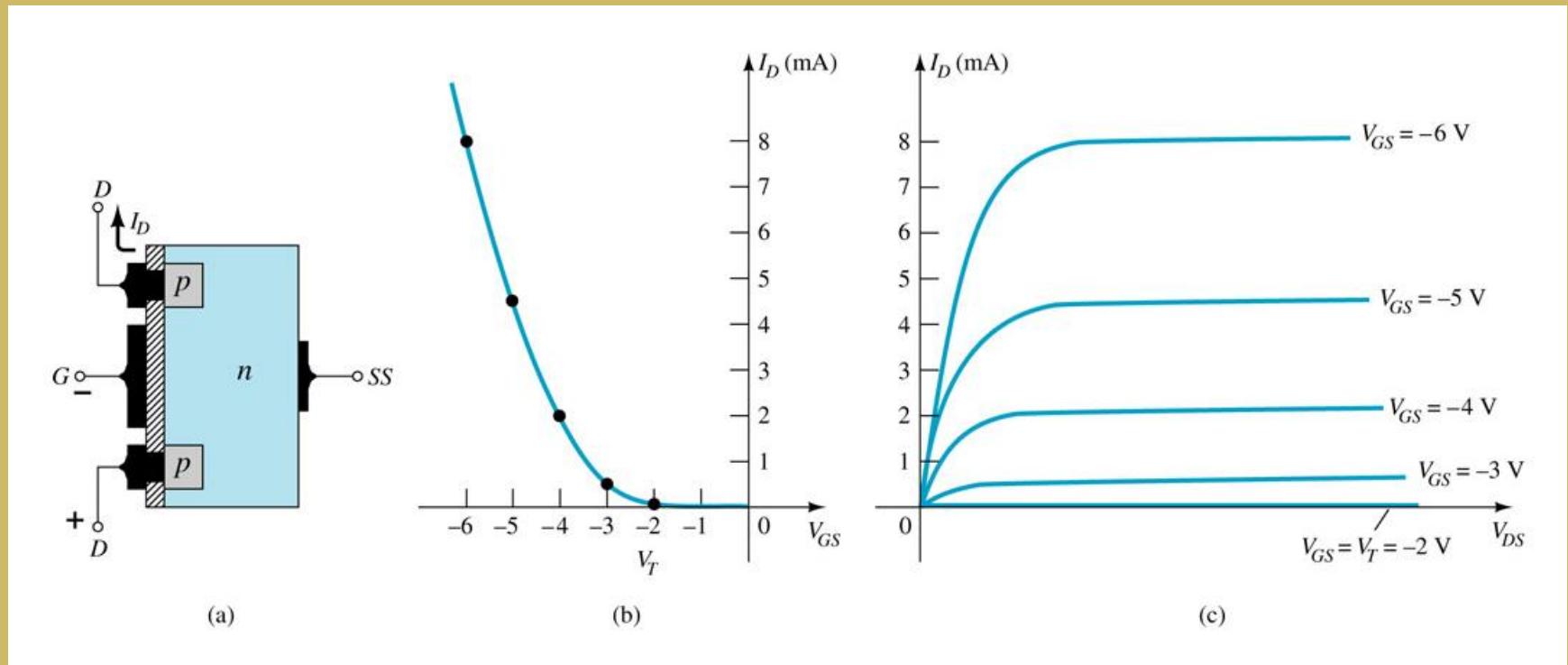
The PSpice determination of  $k$  is based on the geometry of the device:

$$k = \left( \frac{W}{L} \right) \left( \frac{KP}{2} \right) \quad \text{where } KP = \mu_n C_{ox}$$



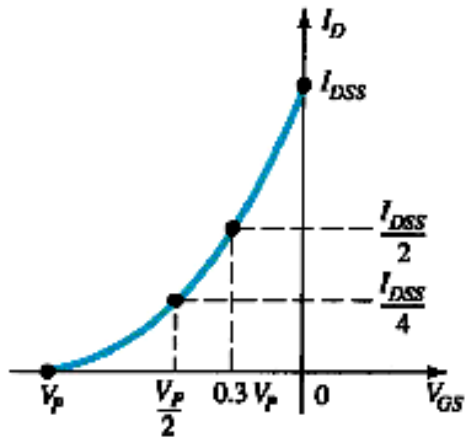
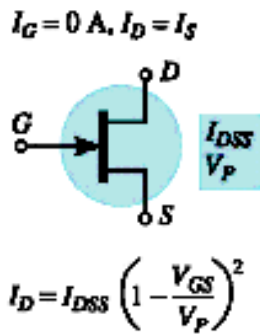
## p-Channel Enhancement Mode MOSFETs

The p-channel Enhancement mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.

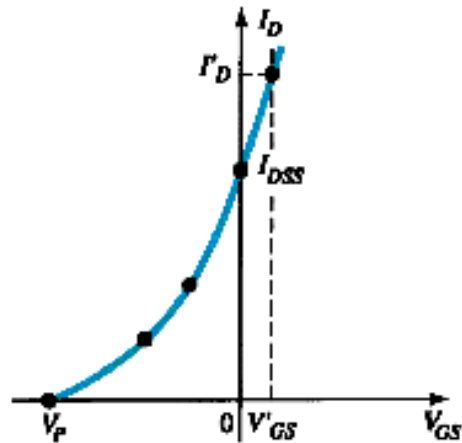
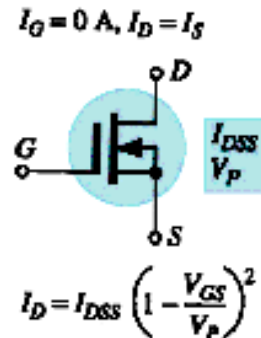


# Summary Table

## JFET



## D-MOSFET



## E-MOSFET

