Microprocessor & Interfacing
Lecture 26
8237 DMA Controller--1

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Contents

Introduction

- Direct memory access (DMA) is a process in which an external device takes over the control of system bus from the CPU.
- DMA used for high-speed data transfer from/to mass storage peripherals, e.g.
  - Hard disk drive,
  - Magnetic tape,
  - CD-ROM, and sometimes video controllers.

Cont..

- Example
  - A hard disk transfer rate of 5 M bytes per second, i.e. 1 byte transmission every 200 ns. To make such data transfer via the CPU is both undesirable and unnecessary.
- The basic idea of DMA is to transfer blocks of data directly between memory and peripherals. The data don't go through the microprocessor but the data bus is occupied.
- "Normal" transfer of one data byte takes up to 29 clock cycles.
- The DMA transfer requires only 5 clock cycles.
- Nowadays, DMA can transfer data as fast as 60 M byte per second. The transfer rate is limited by the speed of memory and peripheral devices.

Features

1. It provides various modes of DMA.
2. It provides on chip 4 independent channel. The no of channel can be increased by cascading.
3. Each channel can be used in auto initialize mode.
4. It can transfer data from memory to memory.
5. In memory to memory transfer single word can be written in all location of memory block.
6. Address of memory is either increment or decrement.
7. Clock frequency 3Mhz.
8. Data transfer rate 1.6 Mbps/sec.

Cont..

9. Directly expendable to any no of channel by cascading.
10. It provides EOP line that is used for terminate DMA operation. This signal can be generated by external h/w.
11. DMA can be requested by setting an appropriate bit of request register.
12. Independent control for DREQ and DACK. These signal can be initialized by active high or low.
13. It provides compressed timing to improve throughput. It can compress the transfer time to 2s.

Basic Process of DMA

- For 8088 in maximum mode:
  - The RQ/GT1 and RQ/GT0 pins are used to issue DMA request and receive acknowledge signals.
- Sequence of events of a typical DMA process

1) Peripheral asserts one of the request pins, e.g. RQ/GT1 or RQ/GT0 (RQ/GT0 has higher priority)
2) 8088 completes its current bus cycle and enters into a HOLD state
3) 8088 grants the right of bus control by asserting a grant signal via the same pin as the request signal.
4) DMA operation starts.
5) Upon completion of the DMA operation, the peripheral asserts the request/grant pin again to relinquish bus control.

Minimum Mode

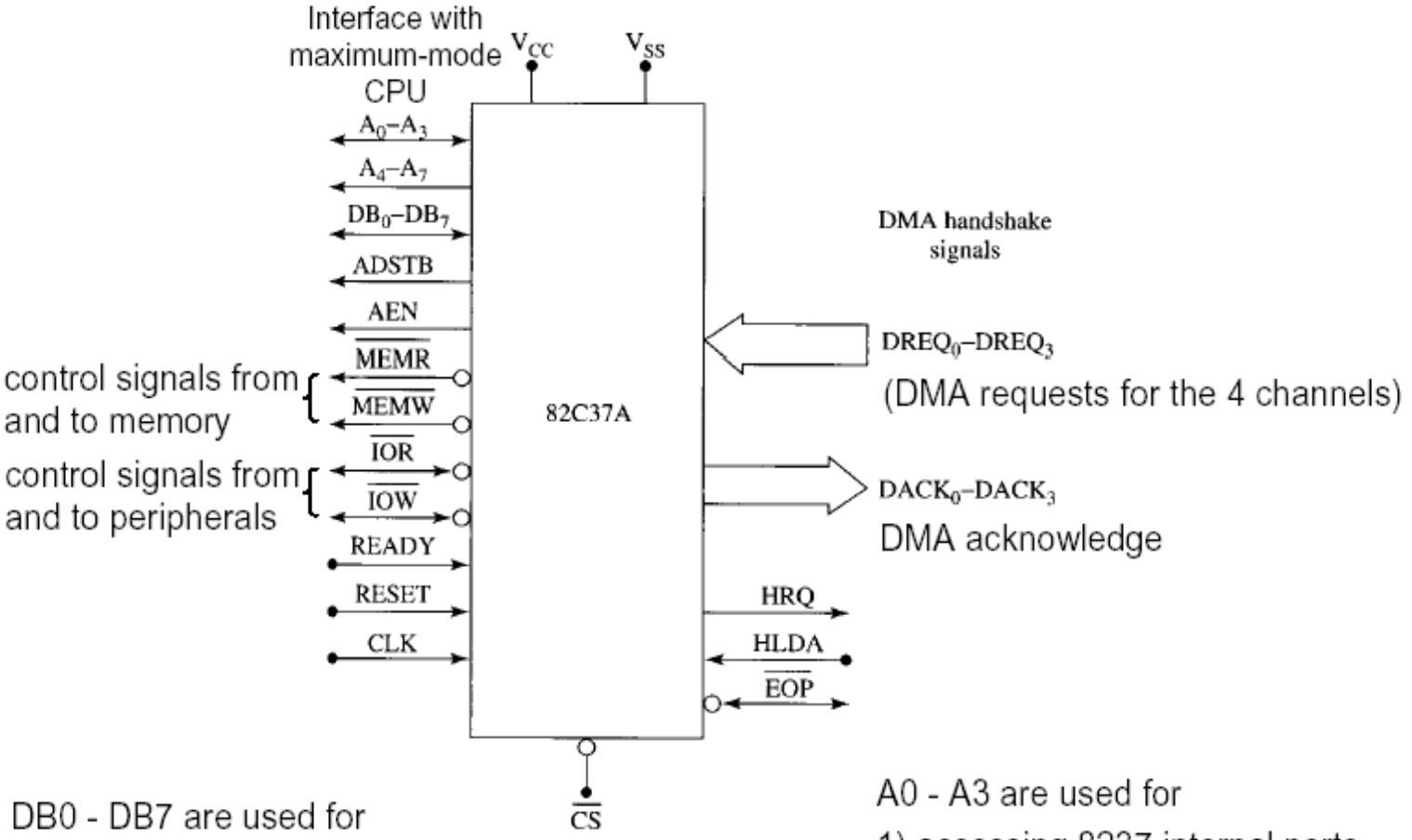
- For 8088 in minimum mode:
  - The HOLD and HLDA pins are used instead to receive and acknowledge the hold request respectively.
  - Normally the CPU has full control of the system bus.
  - In a DMA operation, the peripheral takes over bus control temporarily.

DMA Controller

- A DMA controller interfaces with several peripherals that may request DMA.
- The controller decides the priority of simultaneous DMA requests communicates with the peripheral and the CPU, and provides memory addresses for data transfer.
- DMA controller commonly used with 8088 is the 8237 programmable device.
- The 8237 is in fact a special-purpose microprocessor.
- Normally it appears as part of the system controller chip-sets.
- The 8237 is a 4-channel device.
- Each channel is dedicated to a specific peripheral device and capable of addressing 64 K bytes section of memory.

8237 DMA Controller

8237 DMA controller

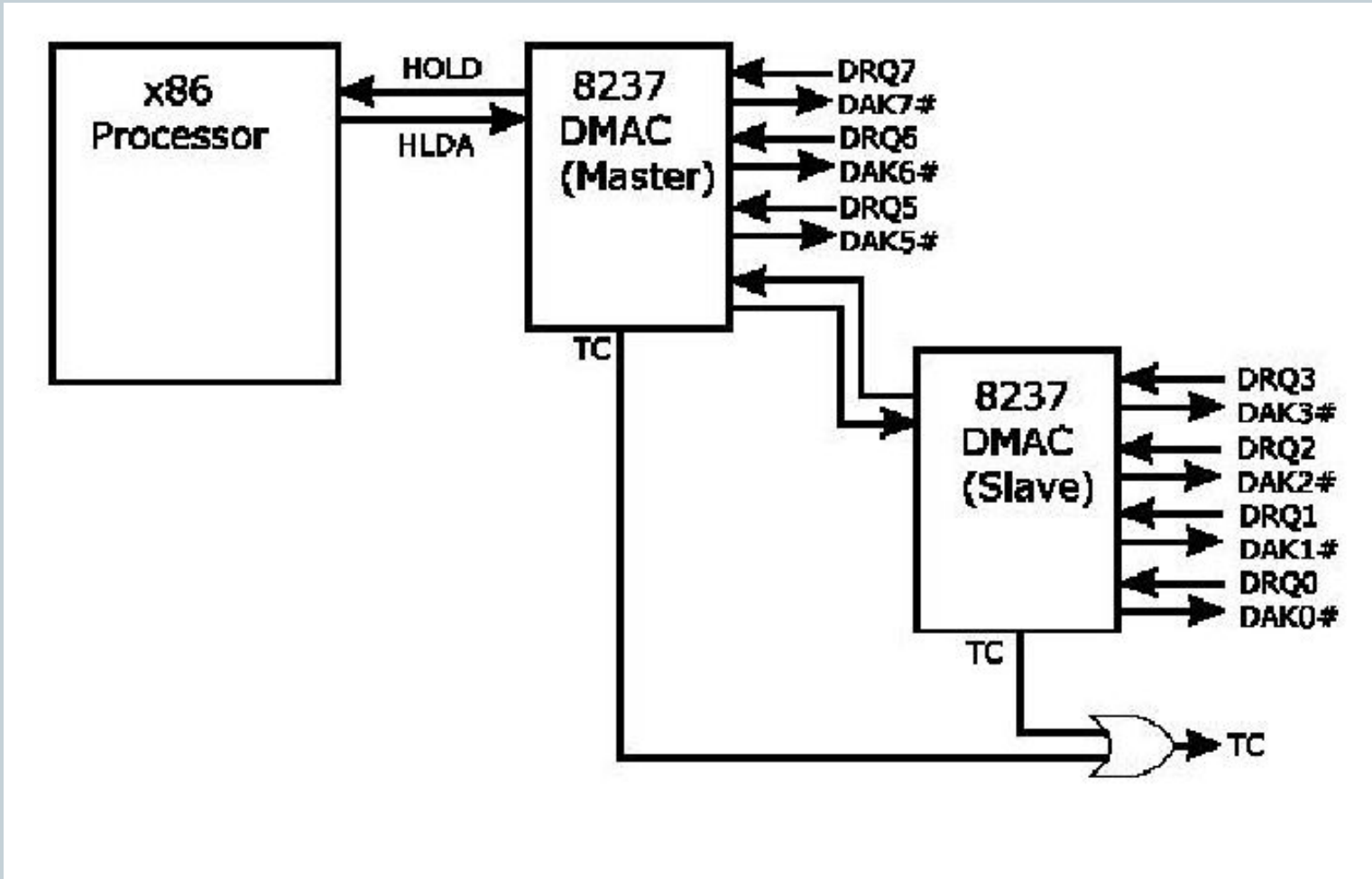


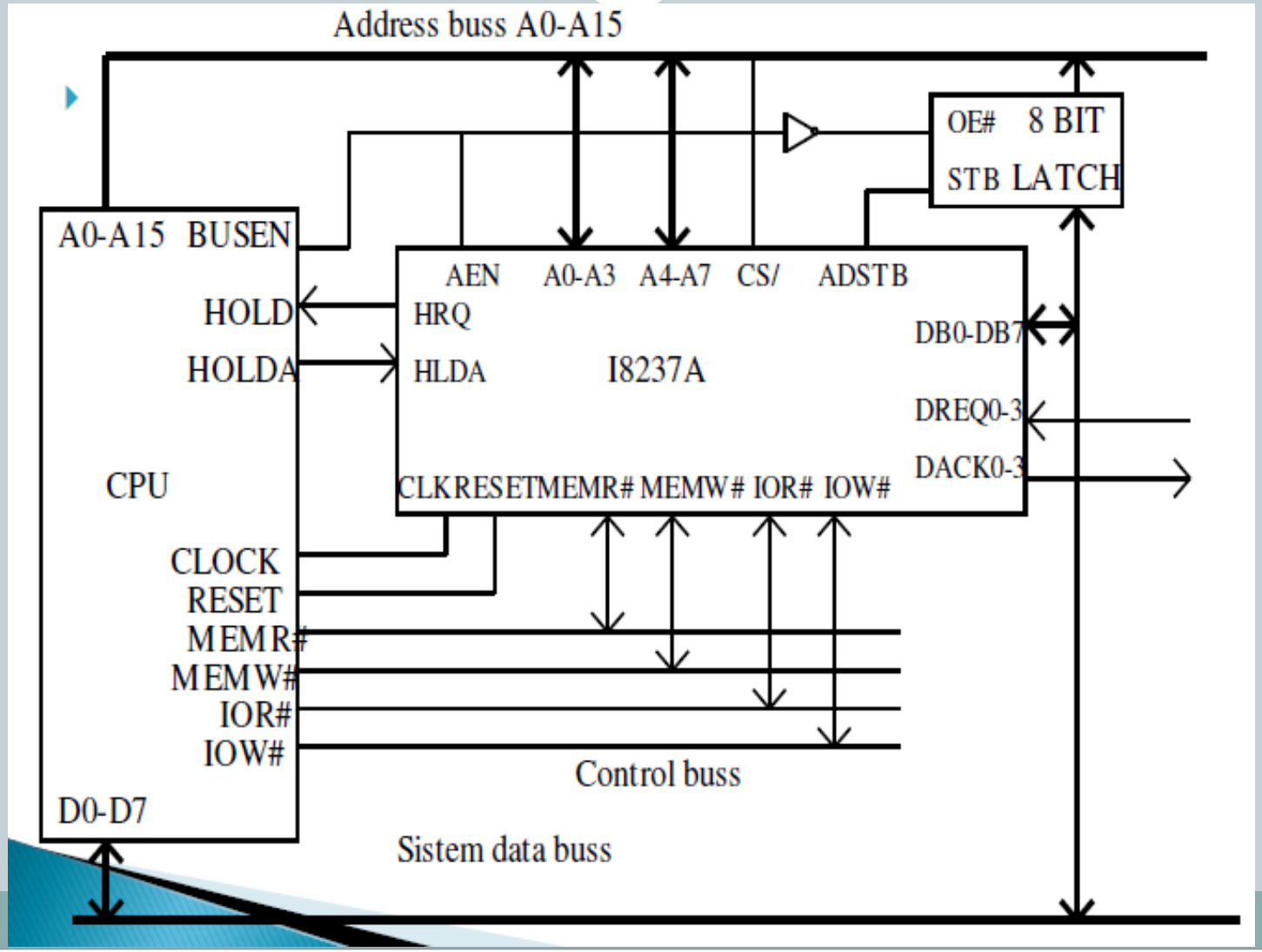
DB0 - DB7 are used for

1) transfer of data
2) 8237 programming

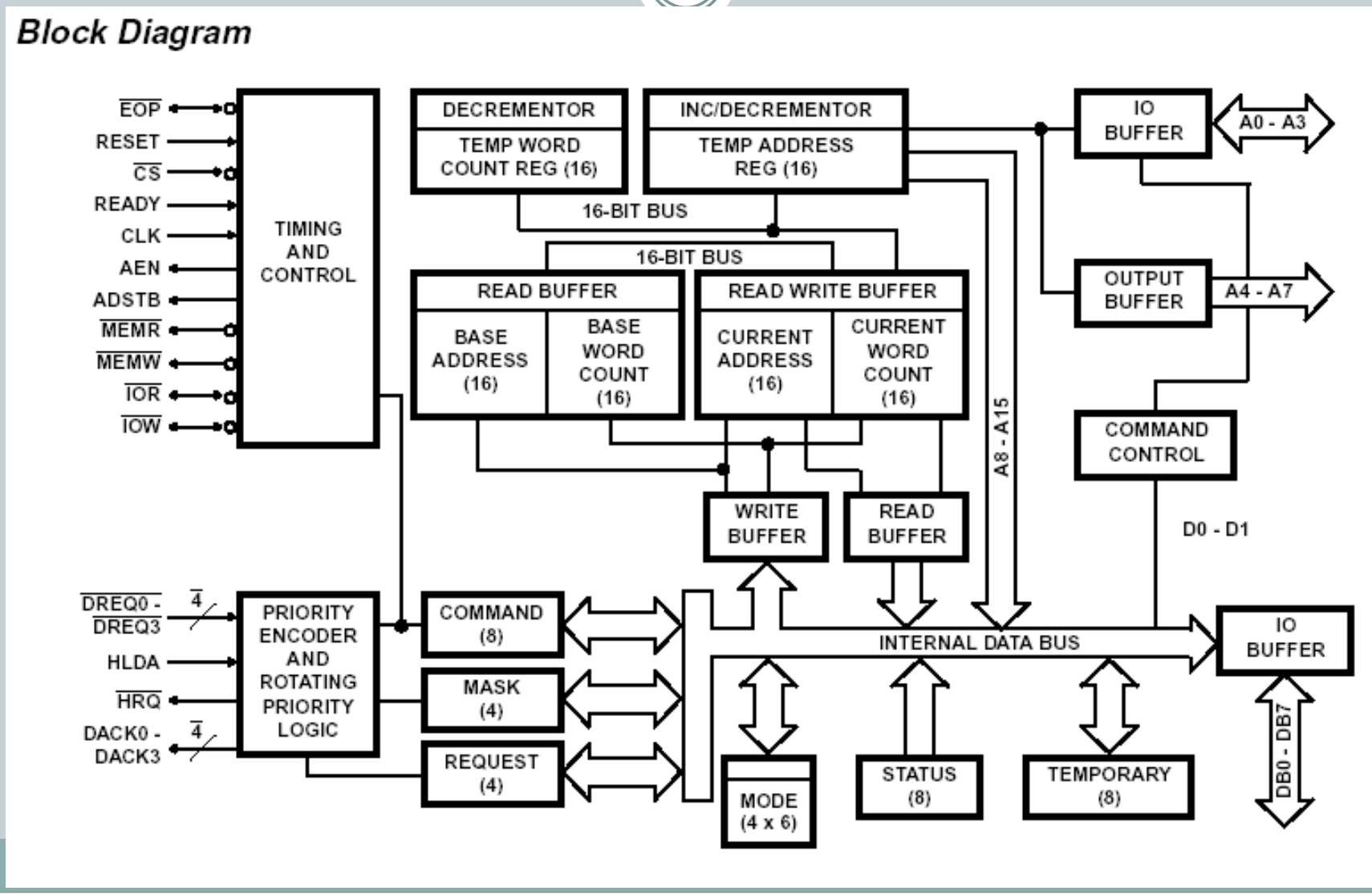
A0 - A3 are used for

1) accessing 8237 internal ports
2) carrying memory address in DMA read and write operations


x86
Processor
HOLD
HLDA
8237
DMAC
(Master)
DRQ7
DAK7#
DRQ6
DAK6#
DRQ5
DAK5#
TC
8237
DMAC
(Slave)
DRQ3
DAK3#
DRQ2
DAK2#
DRQ1
DAK1#
DRQ0
DAK0#
TC
TC


Address buss A0-A15
OE#
8 BIT
STB
LATCH
A0-A15
BUSEN
AEN
A0-A3
A4-A7
CS/
ADSTB
HOLD
HRQ
DB0-DB7
HOLDA
HLDA
I8237A
DREQ0-3
DACK0-3
CPU
CLK
RESET
MEMR#
MEMW#
IOR#
IOW#
CLOCK
RESET
MEMR#
MEMW#
IOR#
IOW#
Control buss
D0-D7
Sistem data buss

Block Diagram



- Figure shows internal block diagram of 8237A it consists block of:
- Control register and
- Internal register

Control Logic

- 8237A contain three basic block of control logic.

i. Timing and control Block: It generates internal timing and external control signal to the 8237A.

ii. Program command control Block: It decodes various command given to the 8237 by the microprocessor before servicing a DMA request. It also decodes the mode control word, which is used to select the type of DMA during the servicing.

iii. Internal registers: 8237 contain 344 bits of internal memory in the form of register.