Microprocessor & Interfacing
Lecture 25
Direct Memory Access--2

ECS DEPARTMENT
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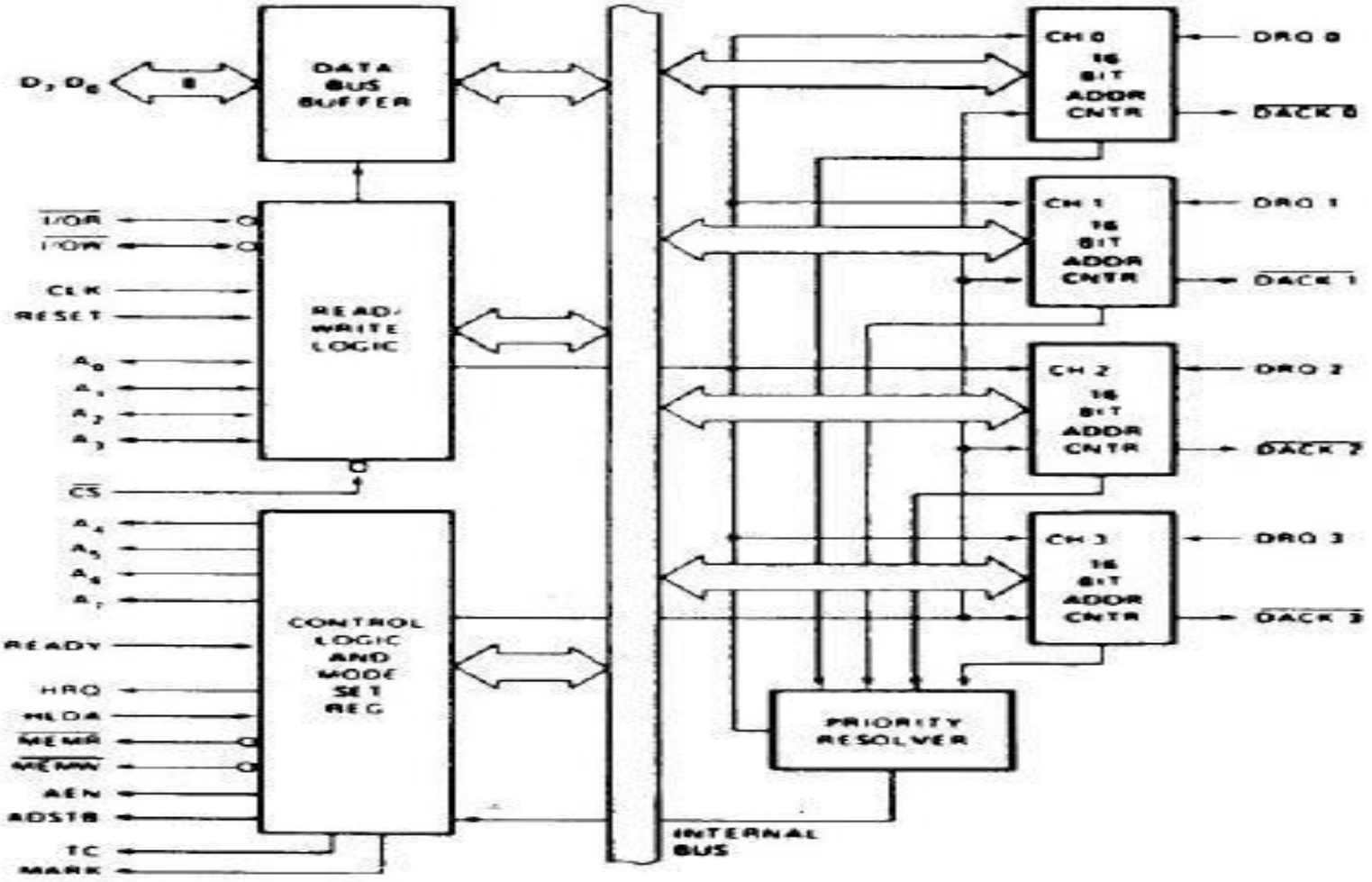
8257 DMA Controller



Description

- It containing five main Blocks.

1. Data bus buffer
2. Read/Control logic
3. Control logic block
4. Priority resolver
5. DMA channels.

Cont..

- DATA BUS BUFFER:
  - It contain tristate ,8 bit bi-directional buffer.
  - Slave mode ,it transfer data between microprocessor and internal data bus.
  - Master mode ,the outputs A8-A15 bits of memory address on data lines (Unidirectional).
- READ/CONTROL LOGIC:
  - It control all internal Read/Write operation.
  - Slave mode ,it accepts address bits and control signal from microprocessor.
  - Master mode ,it generate address bits and control signal.

Cont..

- Control logic block:

  It contains:

  1. Control logic
  2. Mode set register and
  3. Status Register.

- CONTROL LOGIC:
  - Master mode: It controls the sequence of DMA operation during all DMA cycles.
  - It generates address and control signals.
  - It increments 16 bit address and decrement 14 bit counter registers.
  - It activates a HRQ signal on DMA channel Request.
  - Slave mode: It is disabled.

Cont..

- MODE SET REGISTERS:
  - It is a write only registers.
  - It is used to set the operating modes.
  - This registers is programmed after initialization of DMA channel.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
AL	TCS	EW	RP	EN_3	EN_2	EN_1	EN_0

Cont..

- AL=1=Auto load mode
- AL=0=Rotating mode

- TCS=1=Stop after TC (Disable Channel)
- TCS=0=Start after TC (Enable Channel)

- EW=1=Extended write mode
- EW=0=normal mode.

- RP=1=Rotating priority
- RP=0=Fixed priority.

Cont..

- EN3=1=Enable DMA CH-3
- EN3=0=Disable DMA CH-3
- EN2=1=Enable DMA CH-2
- EN2=0=Disable DMA CH-2
- EN1=1=Enable DMA CH-1
- EN1=0=Disable DMA CH-1
- EN0=1=Enable DMA CH-0
- EN0=0=Disable DMA CH-0

Cont..

- STATUS REGISTERS:
  - It is read only register.
  - It tells the status of DMA channels
  - TC status bits are set when TC signal is activated for that channel.
  - Update flag is not affected during read operation.
  - The UP bit is set during update cycle . It is cleared after completion of update cycle.

Cont..

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	UP	TC_3	TC_2	TC_1	TC_O

- UP=Update flag
- UP=1=8257 executing update cycle
- UP=0=8257 executing DMA cycle
- TC3=1=TC activated CH-3
- TC3=0=TC activated CH-3
- TC2=1=TC activated CH-2
- TC2=0=TC activated CH-2
- TC1=1=TC activated CH-1
- TC1=0=TC activated CH-1
- TC0=1=TC activated CH-0
- TC0=0=TC activated CH-0
- The address of status register is A3A2A1A0=1000.

Cont..

FIRST/LAST FLIP FLOP:

- 8257 have 8bit data line and 16 bit address line.
- 8085 it is getting 8-bit data in simultaneously.
- 8085 can not access 16-bit address in simultaneously.
- A0-A3 lines are used to distinguish between registers, but they are not distinguish lower and higher address.
- It is reset by external RESET signal.
- It is also reset by whenever mode set register is loaded.
- So program initialization with a dummy (00 H).
- FF=1=Higher byte of address
- FF=0=Lower byte of address.

Modes of Operation

- Rotating priority Mode: The priority of the channels has a circular sequence.
- Fixed Priority Rotating Mode: The priority is fixed.
- TC Stop Mode
- Auto Load mode
- Extended Write mode

DMA Cycles

- DMA read
- DMA write
- DMA verify

Scope of Research

- Now a days lot of research are doing for speed up the data transfer rate and the equipment are coming which used data transfer without interfering the microprocessor.