Microprocessor & Interfacing
Lecture 24
Direct Memory Access--1

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Introduction

- Direct memory access is the method in which data is transfer from memory to port or input output device with out used of the microprocessor or we can say that here data are transfer without microprocessor. We can develop such device which can direct transfer of data.

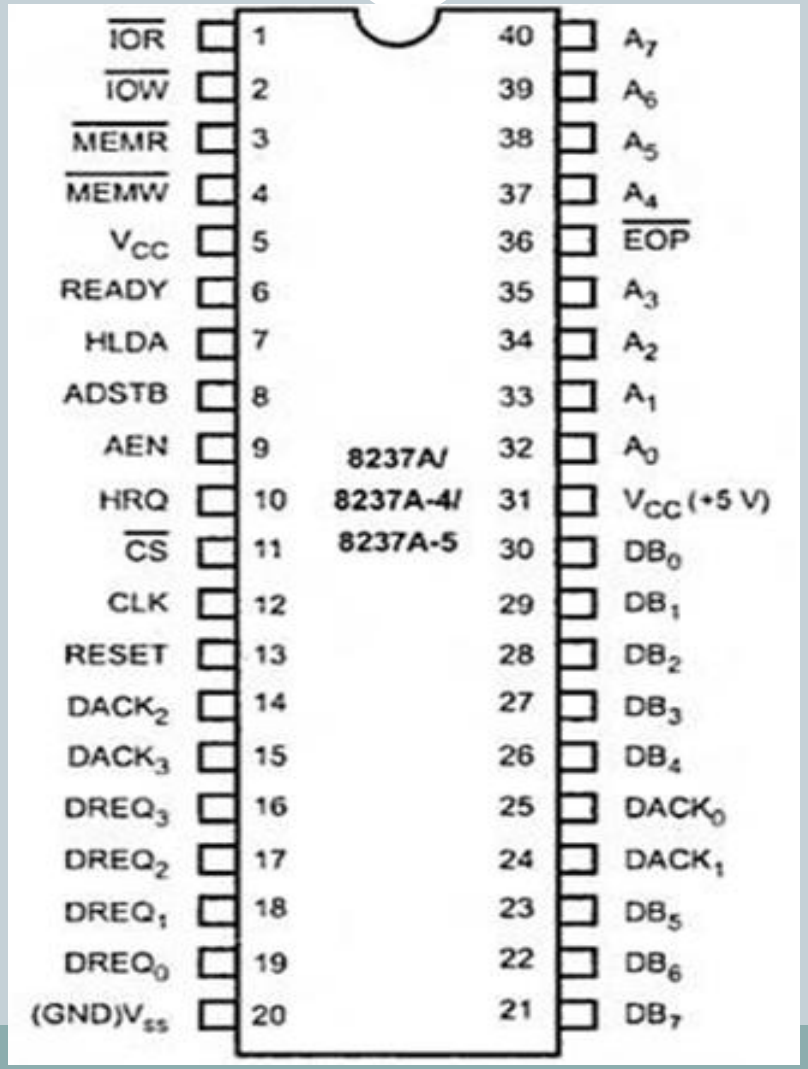
Features

- It is a 4-channel DMA, so 4 I/O devices can be interfaced to DMA
- It is designed by Intel
- Each channel have 16-bit address and 14 bit counter
- It provides chip priority resolver that resolves priority of channels in fixed or rotating mode.
- It provide on chip channel inhibit logic.
- It generates a TC signal to indicate the peripheral that the programmed number of data bytes have been transferred.
- It generates MARK signal to indicate the peripheral that 128 bytes have been transferred.

Features Cont..

- It requires single phase clock.
- The maximum frequency is 3Mhz and minimum frequency is 250 Hz.
- It executes 3 DMA cycles:
  - 1.DMA read 2.DMA write 3.DMA verify.
- It provides AEN signal that can be used to isolate CPU and other devices from the system bus.
- It operates in two modes:
  - 1.Master Mode
  - 2.Slave Mode

Pin Diagram of 8237 DMA Controller



Pin Description

- D0-D7:
  - It is a bidirectional, tri state, Buffered, Multiplexed data (D0-D7) and (A8-A15).
  - In the slave mode it is a bidirectional (Data is moving).
  - In the Master mode it is a unidirectional (Address is moving).
- IOR:
  - It is active low, tristate, buffered, Bidirectional lines.
  - In the slave mode it function as a input line. IOR signal is generated by microprocessor to read the contents 8257 registers.
  - In the master mode it function as a output line. IOR signal is generated by 8257 during write cycle

Cont..

- IOW:
  - It is active low, tristate, buffered, Bidirectional control lines.
  - In the slave mode it function as a input line. IOR signal is generated by microprocessor to write the contents 8257 registers.
  - In the master mode it function as a output line. IOR signal is generated by 8257 during read cycle
- CLK:
  - It is the input line, connected with TTL clock generator.
  - This signal is ignored in slave mode.
- RESET:
  - Used to clear mode set registers and status registers.

Cont..

- A0-A3:
  - These are the tristate, buffer, bidirectional address lines.
  - In slave mode, these lines are used as address inputs lines and internally decoded to access the internal registers.
  - In master mode, these lines are used as address outputs lines, A0-A3 bits of memory address on the lines.
- CS:
  - It is active low, Chip select input line.
  - In the slave mode, it is used to select the chip.
  - In the master mode, it is ignored.

Cont..

- A4-A7:
  - These are the tristate, buffer, output address lines.
  - In slave mode ,these lines are used as address outputs lines.
  - In master mode, these lines are used as address outputs lines, A0-A3 bits of memory address on the lines.
- READY:
  - It is a asynchronous input line.
  - In master mode,
    - **When ready is high it is received the signal.**
    - **When ready is low, it adds wait state between S1 and S3**
  - In slave mode, this signal is ignored.

Cont..

- HRQ:
  - It is used to receiving the hold request signal from the output device.
- HLDA:
  - It is acknowledgment signal from microprocessor.
- MEMR:
  - It is active low, tristate, Buffered control output line.
  - In slave mode, it is tristated.
  - In master mode, it activated during DMA read cycle.
- MEMW:
  - It is active low, tristate, Buffered control input line.
  - In slave mode, it is tristated.
  - In master mode, it activated during DMA write cycle.

Cont..

- AEN (Address enable):
  - It is a control output line.
  - In master mode ,it is high
  - In slave mode ,it is low
  - Used it isolate the system address ,data ,and control lines.
- ADSTB (Address Strobe):
  - It is a control output line.
  - Used to split data and address line.
  - It is working in master mode only.
  - In slave mode it is ignore.

Cont..

- TC (Terminal Count):
  - It is a status of output line.
  - It is activated in master mode only.
  - It is high ,it selected the peripheral.
  - It is low ,it free and looking for a new peripheral.
- MARK:
  - It is a modulo 128 MARK output line.
  - It is activated in master mode only.
  - It goes high ,after transferring every 128 bytes of data block.

Cont..

- DRQ0-DRQ3(DMA Request):
  - These are the asynchronous peripheral request input signal.
  - The request signals is generated by external peripheral device.
- DACK0-DACK3:
  - These are the active low DMA acknowledge output lines.
  - Low level indicate that ,peripheral is selected for giving the information (DMA cycle).
  - In master mode it is used for chip select.