Microprocessor & Interfacing
Lecture 11
8086 Microprocessor--1

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Introduction

- 8086 is the first 16 bit microprocessor which has 40 pin IC and operate on 5volt power supply. which has twenty address limes and works on two modes minimum mode and maximum.

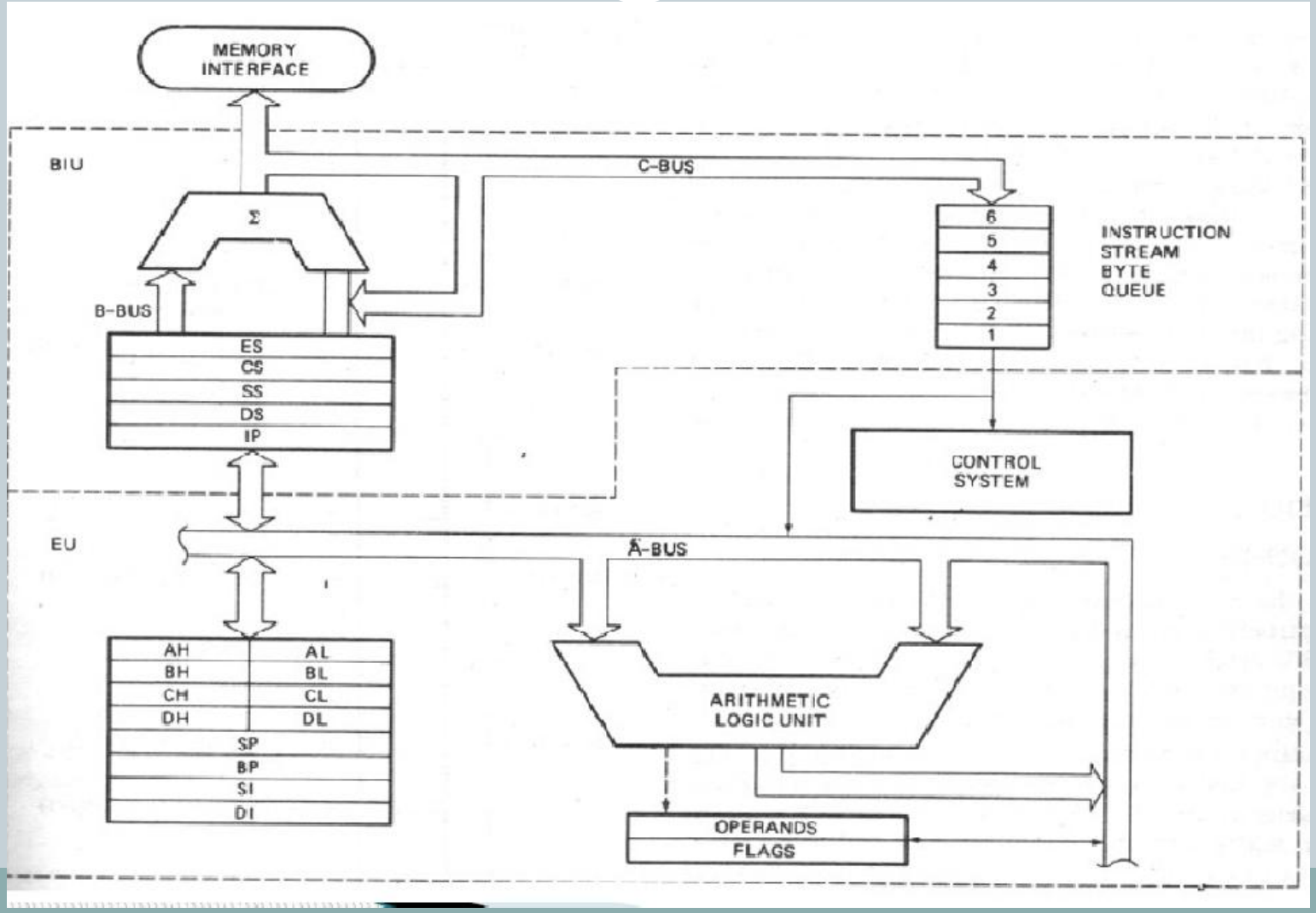
Features of 8086 Microprocessor

- 8086 is a 16bit processor. It's ALU, internal registers works with 16bit binary word
- 8086 has a 16bit data bus. It can read or write data to a memory/port either 16bits or 8 bit at a time
- 8086 has a 20bit address bus which means, it can address upto 2^20 = 1MB memory location
- Frequency range of 8086 is 6-10 MHz

Architecture

- Basic Components
- CPU Registers
  - – special memory locations constructed from flip-flops and implemented on-chip – e.g., accumulator, count register, flag register
- Arithmetic and Logic Unit (ALU)
  - – ALU is where most of the action take place inside the CPU

8086 block diagram



Basic Components

- Bus Interface Unit (BIU) – responsible for controlling the address and data busses when accessing main memory and data in the cache
- Control Unit and Instruction Set – CPU has a fixed set of instructions to work on, e.g., MOV, CMP, JMP

Microprocessor Architecture Instruction processing

- Modern microprocessors can process several instructions simultaneously at various stages of execution
  - – this ability is called pipelining
- Operation of a pipelined microprocessor like the Intel 80486
- Processing of an instruction by microprocessor consists of three basic steps
  - – fetch instruction from the memory
  - – decode the instruction
  - – execute (usually involves accessing the memory for getting operands and storing results)
- Operation of an early processor like the Intel 8085

Important 8086 Pin Diagram/Description

- AD15±AD0ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address and data bus.
- ALE Address Latch Enable. A HIGH on this line causes the lower order 16bit address bus to be latched that stores the addresses and then, the lower order 16bit of the address bus can be used as data bus.

Ready

- READY is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer.
- INTR INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.