LECTURE 28

Timer

Topics to be covered

- WatchdogTimer

The Watchdog Timer (WDT)

- During normal operation a WDT time-out generates a device reset.
- If the device is in SLEEP mode, the watchdog timer can wake it and the device will continue with normal operation. (External resets, RB0/INT, RB port change and EEPROM interrupts will also wake the device.)
- The watchdog timer is configured via the OPTION register. It has a nominal time-out of 18ms which can be increased to ~2.5s by use of the prescaler bits in the OPTION register. The prescalers divide the clock input by one of 8 values which effectively reduce the clock frequency.

2.3.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

Note: When the prescaler is assigned to the WDT (PSA = '1'), TMR0 has a 1:1 prescaler assignment.

REGISTER 2-2: OPTION REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **$\overline{\text{RBPU}}$**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6 **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5 **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

The Watchdog Timer (WDT)

- The WDT is cleared by SLEEP and **CLRWDT** instructions.
- Bits 2-0 of the OPTION register define the prescaler value and hence the WDT time-out period.
- Bit 3 is the prescaler assignment. When this bit is set the prescaler is assigned to the WDT. When it is clear the prescaler is assigned to TMR0, the timer counter.
- The /TO bit in the STATUS register is cleared by a WDT time-out.

2.3.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

Note: When the prescaler is assigned to the WDT (PSA = '1'), TMR0 has a 1:1 prescaler assignment.

REGISTER 2-2: OPTION REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **RBPU**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6 **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5 **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

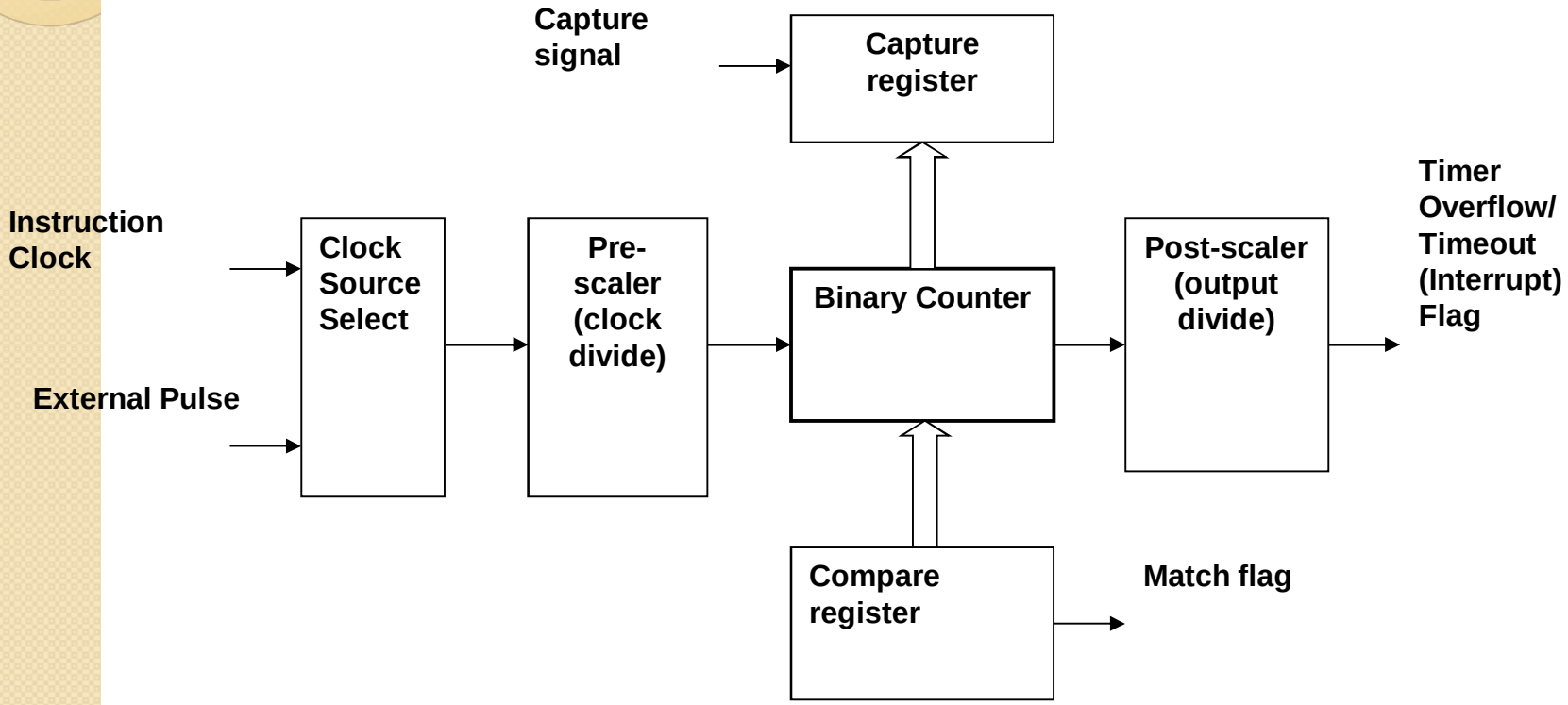
bit 4 **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

General Timer Operation



A binary counter is used as a timer when driven from the clock

Timer Modules :

PIC 16C74A has three modules, viz., Timer-0, Timer-1 and Timer-2.

Timer-0 and Timer-2 are 8-bit timers.

Timer-1 is a 16-bit timer.

Each timer module can generate an interrupt on timer overflow.

•Timer-0 Overview:

•The timer-0 module is a simple 8-bit UP counter.

•The clock source can be either the internal clock (f_{osc} /4) or an external clock.

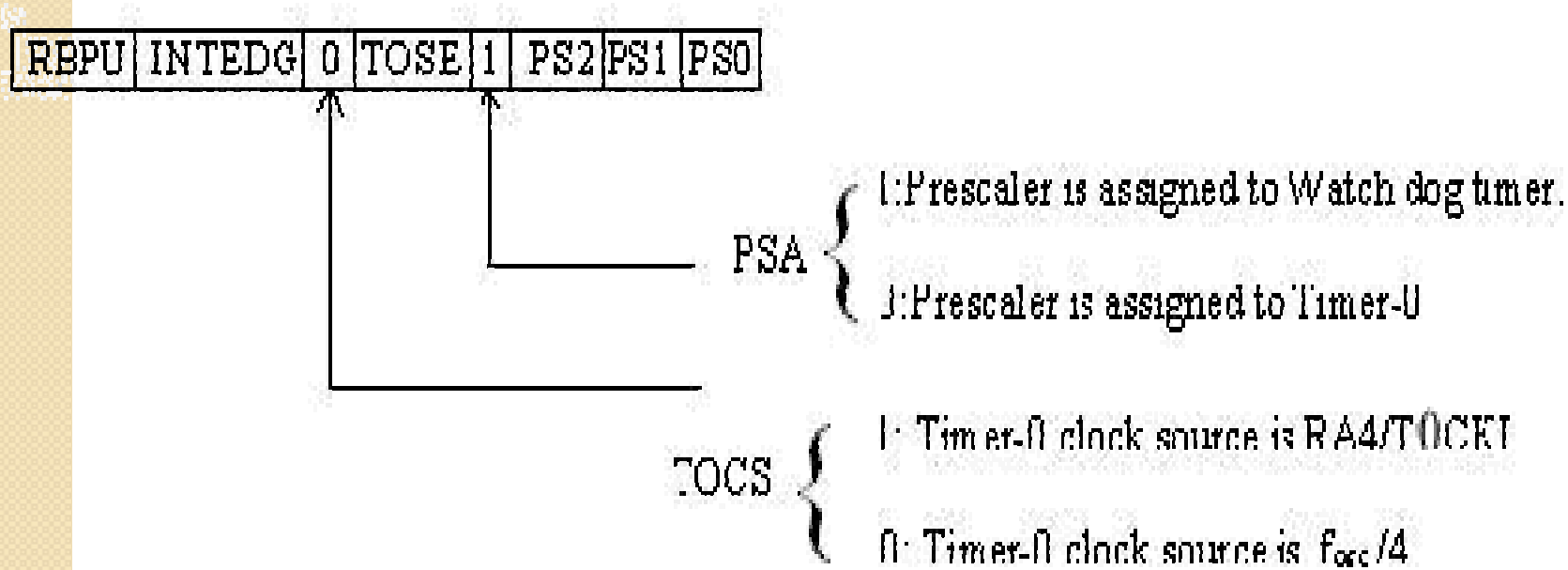
• When the clock source is external, the Timer-0 module can be programmed to increment on either the rising or falling clock edge.

• Timer-0 module has a programmable pre-scaler option. This pre-scaler can be assigned either to Timer-0 or the Watch dog timer, but not to both.

•The Timer-0 Counter sets a flag T0IF (Timer-0 Interrupt Flag) when it overflows and can cause an interrupt at that time if that interrupt source has been enabled, (T0IE = 1), i.e., timer-0 interrupt enable bit = 1.

OPTION Register Configuration :

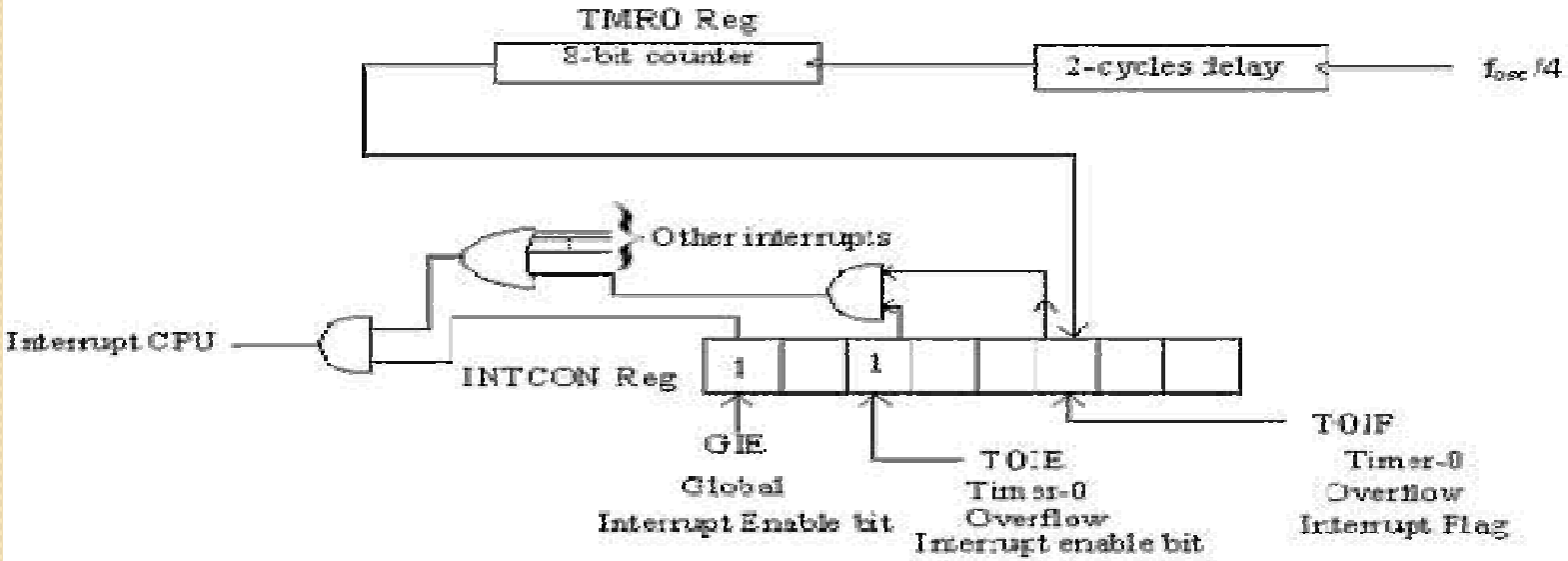
Option Register (Addr: 81H) Controls the prescaler and Timer -0 clock source. The following OPTION register configuration is for clock source = fosc /4 and no Watchdog timer.



Timer-0 use without pre-scalar(As Interrupt)

Internal clock source of $f_{osc}/4$. (External clock source, if selected, can be applied at RA4/TOCKI input at PORTA).

The following diagram shows the timer use without the prescaler.

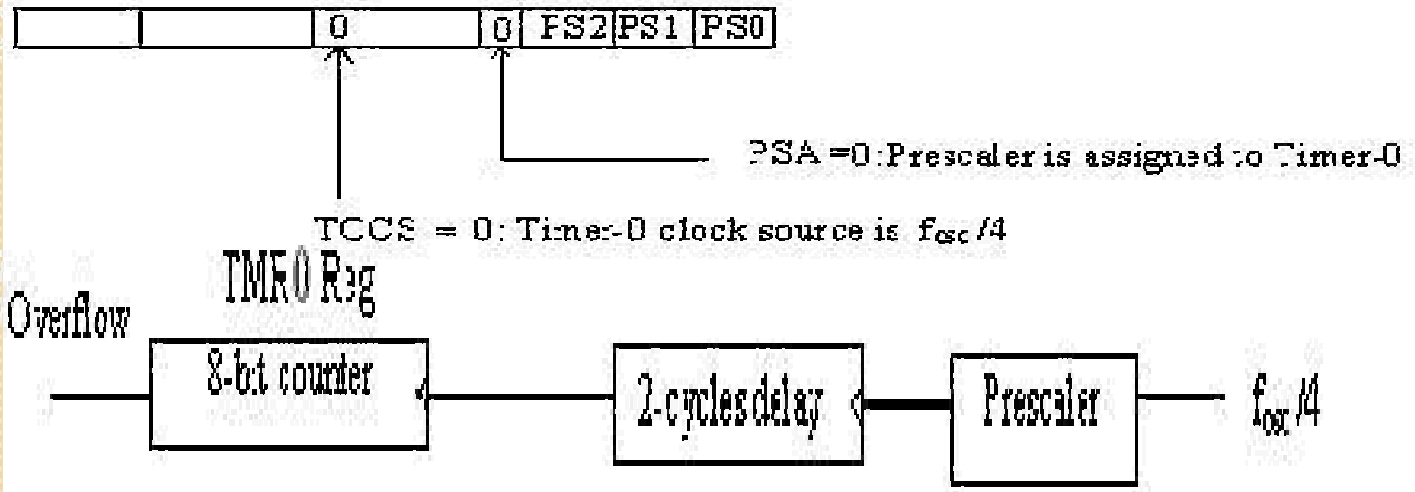


Timer - 0 operation without prescaler

Timer-0 use with pre-scalar:

The pre-scalar can be used either with the Timer-0 module or with the Watchdog timer. The pre-scalar is available for Timer-0 if the pre-scalar assignment bit PSA in the OPTION register is 0.

Pre-scalar is a programmable divide by n counter that divides the available clock by a pre-specified number before applying to the Timer-0 counter.



Timer - 0 with prescaler

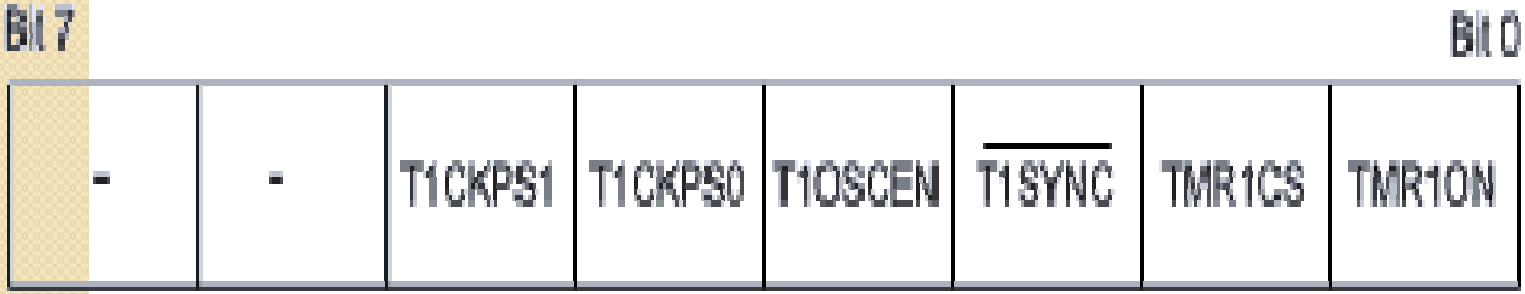
Prescaler bits			Divide by N
PS2	PS1	PS0	
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Timer - 1 Module

Timer 1 module is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable.

The TMR1 register pair (TMR1H:TMR1L) increments from 0000H to FFFFH and rolls over to 0000H.

The operating and control modes of Timer1 are determined by the special purpose register T1CON.



TMR1 ON : Timer1 ON bit

0 = stops Timer 1; 1 = Enables Timer 1

TMR1CS : Timer 1 Clock source Select Bit

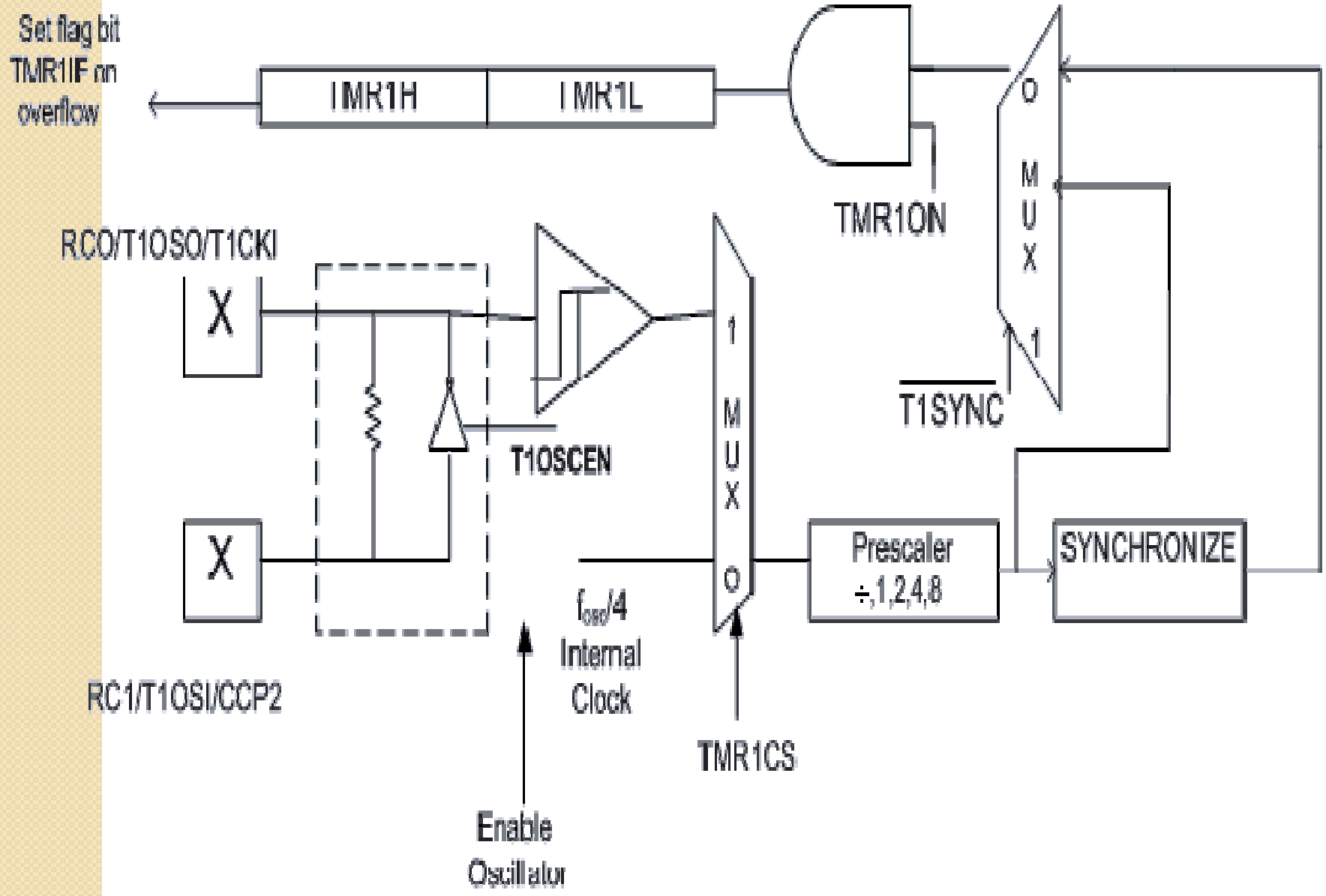
1 = External Clock (RCO/T1OSO/T1CKI)

0 = Internal Clock ( ) $f_{osc}/4$

$\overline{T1SYNC}$: Timer 1 External Clock Input Synchronization Bit
(Valid if TMR1CS = 1)
1 - Do not synchronize
0 - Synchronize

T1OSCEN: Oscillator enable control bit
1 = Oscillator is enabled
0 = Oscillator is shut off

Select bits		**Prescaler Value**
T1CKPS1	**T1CKPS0**	
1	1	1:8
1	0	1:4
0	1	1:2
0	0	1:1

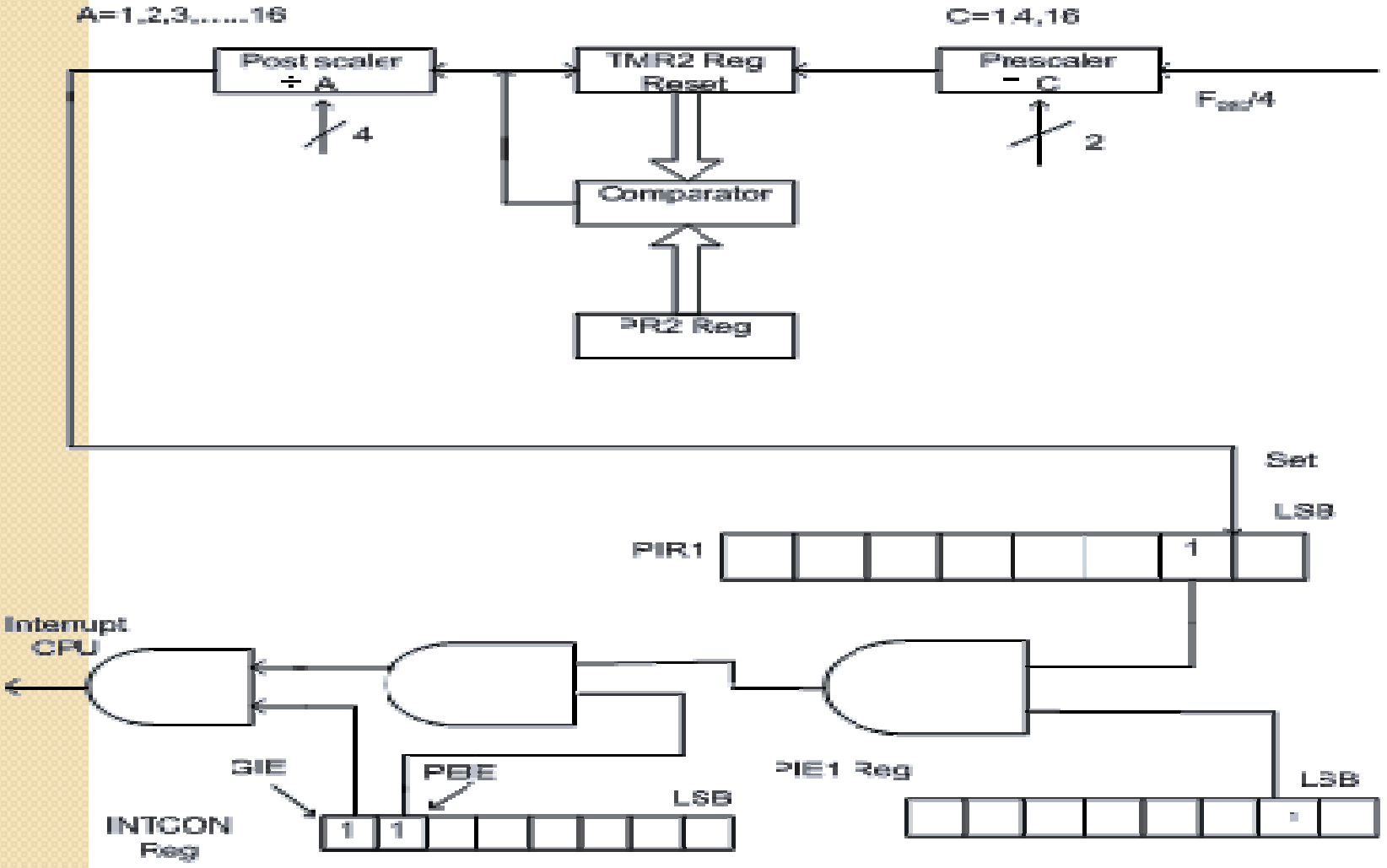

Set flag bit
TMR1IF on
overflow
TMR1H
TMR1L
TMR1ON
O
M
U
X
1
T1SYNC
RC0/T1OSO/T1CKI
X
T1OSCEN
1
M
U
X
O
X
RC1/T1OSI/CCP2
Prescaler
÷,1,2,4,8
SYNCHRONIZE
$f_{osc}/4$
Internal
Clock
TMR1CS
Enable
Oscillator

Timer 1 can operate in one of the two modes

- As a timer (TMR1CS = 0). In the timer mode, Timer 1 increments in every instruction cycle. The timer 1 clock source is $f_{osc}/4$
-
- Since the internal clock is selected, the timer is always synchronized and there is no further need of synchronization.

- As a counter (TMR1CS = 1). In the counter mode, external clock input from the pin RCO/T1CKI is selected.

Timer 2 :


A=1,2,3,.....16
Post scaler
÷ A
4
TMR2 Reg
Reset
Comparator
PR2 Reg
C=1,4,16
Prescaler
÷ C
2
Fosc/4
Set
LSB
PIR1
1
Interrupt
CPU
GIE
PBE
INTCON
Reg
1
1
LSB
PIE1 Reg
LSB

Timer 2:Scalarlization

Timer 2 is an 8 - bit timer with a pre-scaler and a post-scaler. It can be used as the PWM time base for PWM mode of capture compare PWM (CCP) modules.

The TMR2 register is readable and writable and is cleared on device reset.

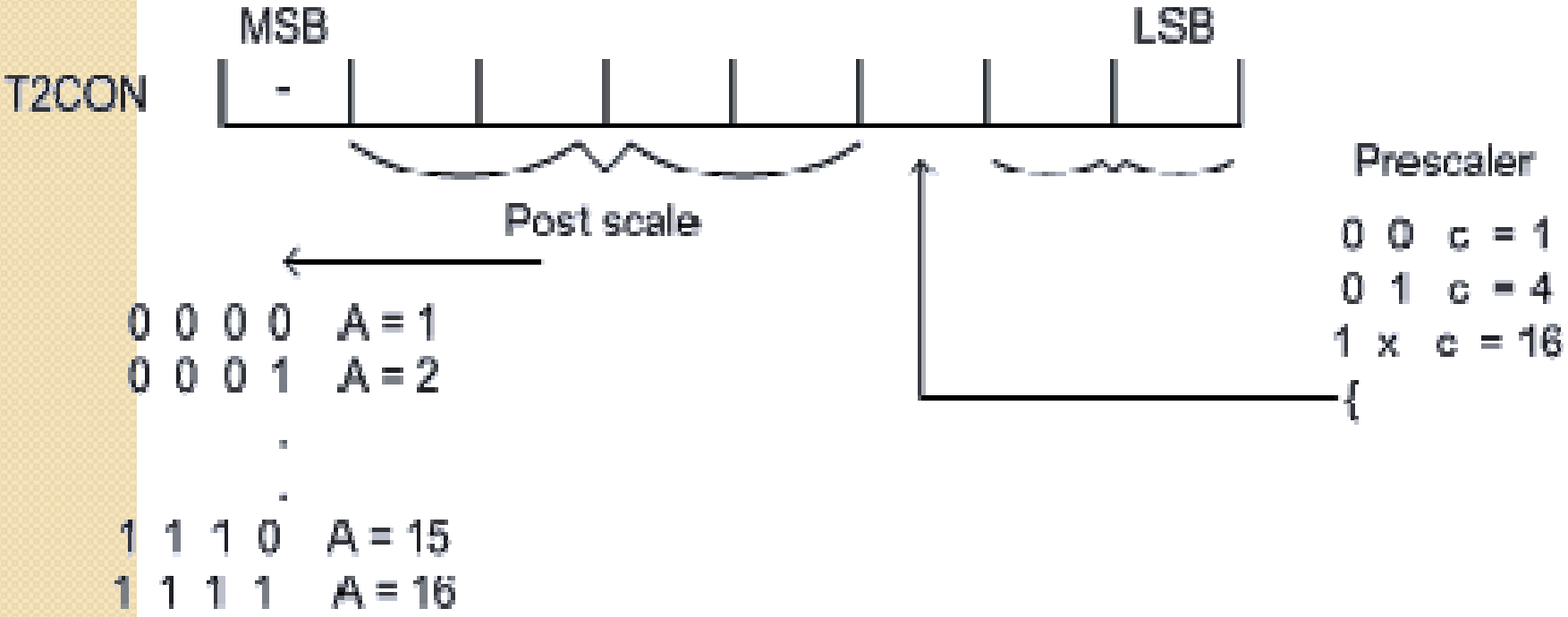
The input clock $f_{osc}/4$ has a pre-scaler option of 1:1, 1:4 or 1:16 which is selected by bit 0 and bit 1 of T2CON register respectively.

The Timer 2 module has an 8bit period register (PR2).

Timer-2 increments from 00H untill it is equal to PR2 and then resets to 00H on the next clock cycle.

PR2 is a readable and writable register. PR2 is initailised to FFH on reset.

The output of TMR2 goes through a 4bit post-scaler (1:1, 1:2, to 1:16) to generate a TMR2 interrupt by setting TMR2IF.



The T2CON Register

Capture / Compare /PWM (CCP) Modules:

PIC16C74A has two CCP Modules. Each CCP module contains a 16 bit register (two 8-bit registers) and can operate in one of the three modes, viz., 16-bit capture, 16-bit compare, or up to 10-bit Pulse Width Modulation (PWM). The details of the two modules (CCP1 and CCP2) are given as follows.

CCP1 Module:

CCP1 Module consists of two 8-bit registers, viz., CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1 Module.

CCP2 Module:

CCP2 Module consists of two 8 bit registers, viz., CCPR2L (Low byte) and CCPR2H (high byte). The CCP1CON register controls the operation of CCP2 Module.

Both CCP1 and CCP2 modules are identical in operation with the exception of the operation of special event trigger.

The following table shows the timer resources for the CCP Mode.

CCP Mode	Timer Used
Capture	Timer 1
Compare	Timer 1
PWM	Timer 2

CCP1CON Register (Address 17H)

CCP2CON Register is exactly similar to CCP1CON register.

CCP2CON Register address is 1DH.

CCP1CON controls CCP module1 where as CCP2CON controls CCP Module2.

Bit 5-4:

CCP1X CCP1Y: PWM least significant bits.

These bits are of no use in Capture mode.

In PWM Mode, these bits are the two Lsbs of the PWM duty cycle.

The eight Msbs are found in CCPR1L. Thus the PWM mode operates in 10-bit mode.

Bit 3-0:

CCP1M3:CCP1MO (CCP1 Mode select bits)

0000=Capture/Compare/PWM Mode off
0100=Capture mode, every falling edge
0101=Capture mode, every rising edge
0110=Capture mode, every 4 th rising edge
0111=Capture mode, every 16 th rising edge

1000=Compare mode, set output on match (CCP1IF bit is set)
1001=Compare mode, clear output on match (CCP1IF bit is set)
1010=Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin unaffected)
1011=Compare mode, trigger special event (CCP1IF bit is set;CCP1 resets Tmr1; CCP2 resets TMR1 and starts A/D conversion if A/D module is Enabled)

11XX=PWM mode.

Capture Mode (CCP1):

Capture Mode captures the 16-bit value of TMR1 into CCPR1H:CCPR1L register pair in response to an event occurring on RC2/CCP1 pin. Capture Mode for CCP2 is exactly similar to that of CCP1.

An event on RC2/CCP1 pin is defined as follows:

- Every falling edge
- Every rising edge.
- Every 4 th rising edge.
- Every 16 th rising edge.

As mentioned earlier, this event is decided by bit 3-0 of CCP1CON register.

Schematic diagram for capture mode of operation

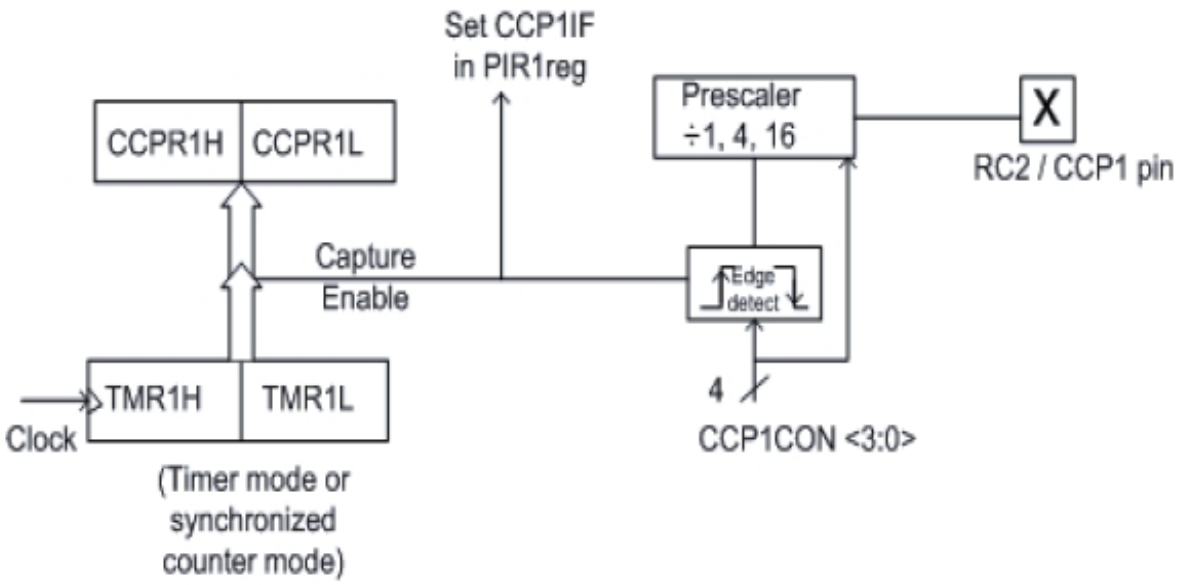


Fig20: Capture operation

Required condition for capture mode:

1. RC2/CCP1 pin should be configured as an input by setting TRISC (bit 2).
2. Timer 1 should be operated from the internal clock (fosc/4), i.e., timer mode or in synchronized counter mode

Compare Mode (CCP1)

Compare mode for CCP2 is similar to that of CCP1, except that in special event trigger mode, CCP1 resets TMR1 only, whereas CCP2 resets TMR1 and starts A/D conversion if A/D module is enabled.

In compare mode, the 16-bit CCPR1 register value is compared against TMR1 register pair (TMR1H and TMR1L) value. When a match occurs, the RC2/CCP1 pin is driven high or driven low or remains unchanged as decided by CCP1CON<3:0> bits.

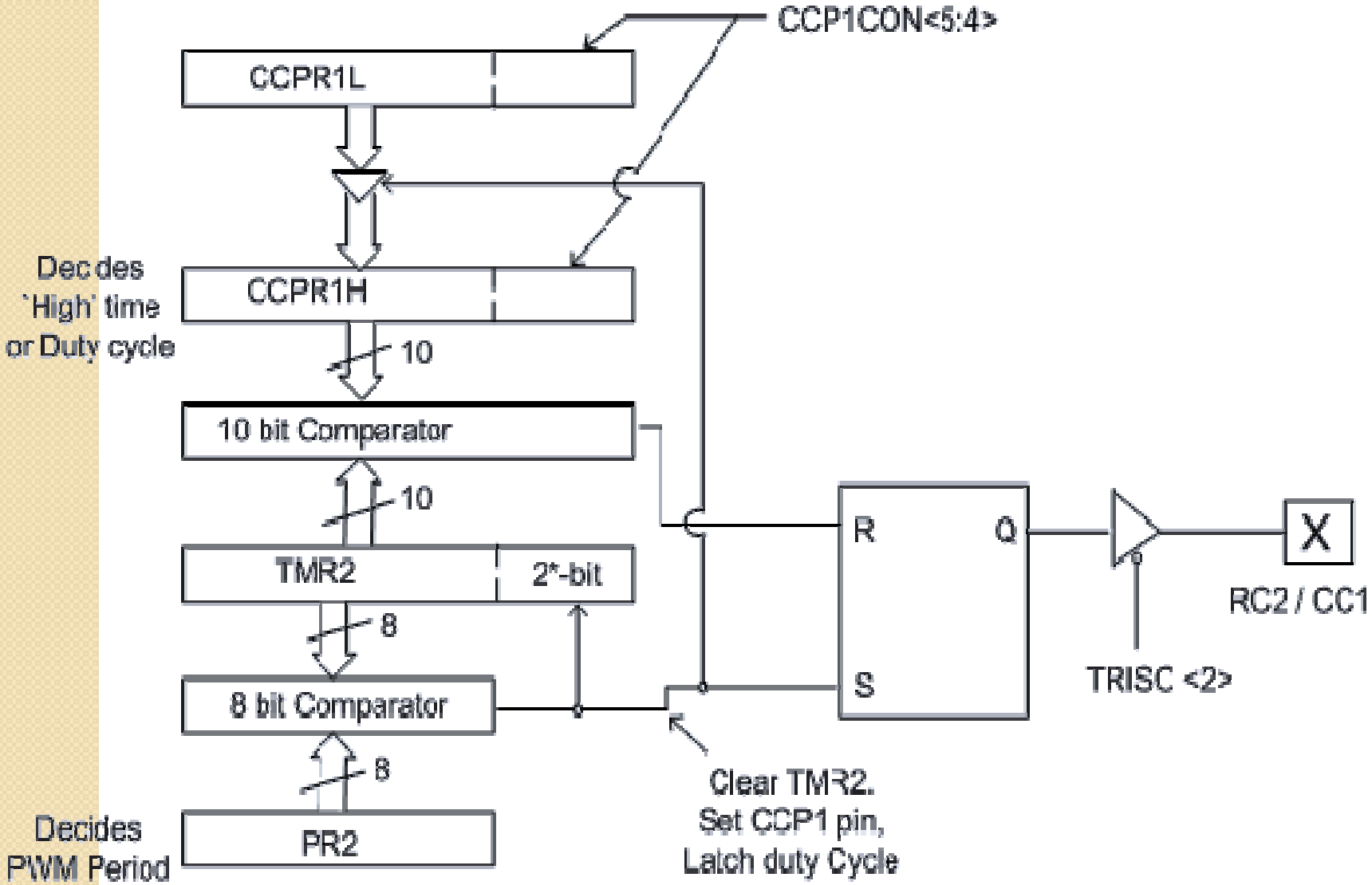
PWM mode (CCP1)

Both CCP1 and CCP2 have similar operation in PWM mode.

In PWM mode, the CCP1 pin produces up to a 10-bit resolution Pulse Width Modulation (PWM) output. .

RC2/CCP1 pin should be configured in the output mode by clearing TRISC<2> bit.

The schematic block diagram of CCP1 module in PWM mode is shown in the figure.

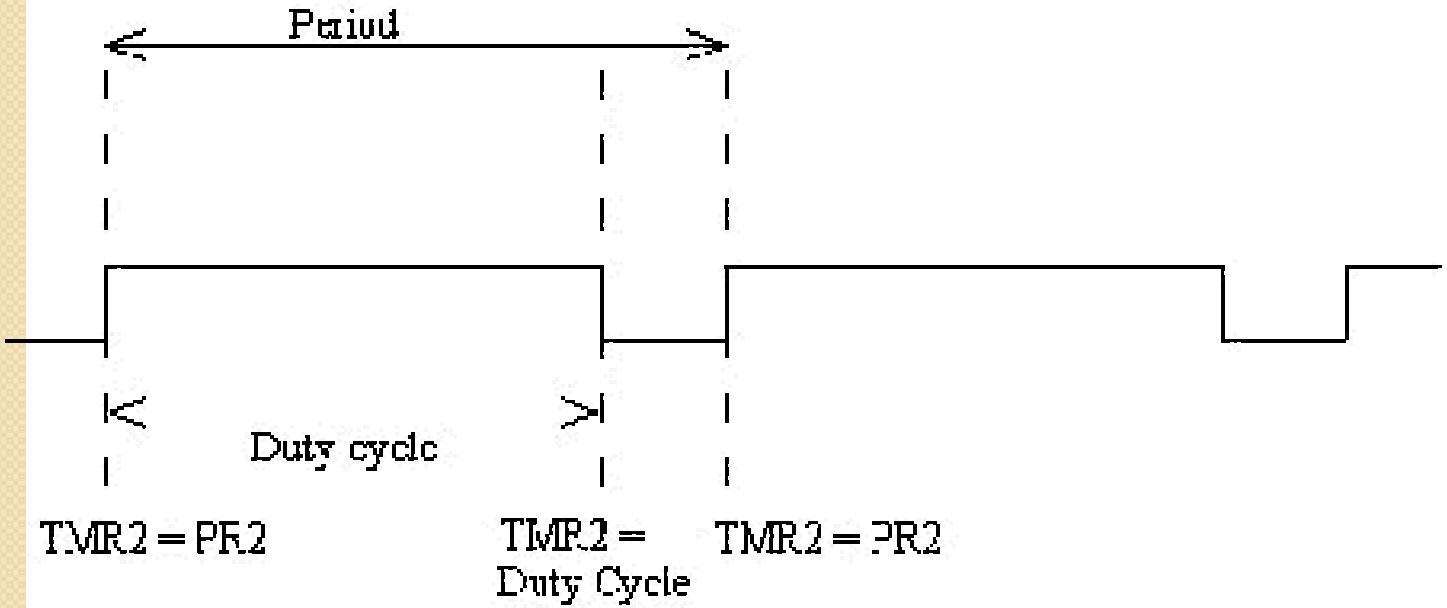

CCP1CON<5:4>
CCPR1L
CCPR1H
Decides
'High' time
or Duty cycle
10
10 bit Comparator
10
TMR2
2*-bit
8
8 bit Comparator
8
PR2
Decides
PWM Period
R
Q
S
X
RC2 / CC1
TRISC <2>
Clear TMR2.
Set CCP1 pin,
Latch duty Cycle

PR2 (Period Register, 8 bit) decides the PWM period where CCPR1L (8-bits) and CCP1CON <5:4> (2-bits) decide the PWM duty cycle.

When TMR2 equals PR2, the SR latch is set and RC2/CCP1 pin is pulled high.

In the same time, TMR2 is cleared and the duty cycle value available in CCPR1L is latched to CCPR1H.

CCPR1H, CCP1CON <5:4> decide the duty cycle and when this 10-bit equals the TMR2+2 prescaler or Q-bits, the SR latch is reset and RC2/CCP1 pin is driven low



The time for which the output stays high is called duty cycle.

PWM Period

The PWM period is specified by writing to PR2 register. The PWM period can be calculated using the following formula:
PWM period = [(*PR* 2) + 1] × 4 × *T osc* × (TMR2 prescale value)

PWM frequency = 1/ PWM period

When TMR2 is equal to PR2, the following events occur on the next increment cycle.

- TMR2 is cleared
- the CCP1 pin is set (if PWM duty cycle is 0
- The PWM duty cycle is latched from CCPR1L into CCPR1H

PWM duty cycle

The PWM duty cycle is specified by writing to the CCPR1L register and to CCP1CON < 5 : 4 > bits.
Up to 10-bit resolution is available where CCPR1L contains the eight MSBs and CCP1CON < 5 : 4 > contains the two LSB's. The 10-bit value is represented by CCPR1L : CCP1CON < 5 : 4 >.

PWM duty cycle = (CCPR1L : CCP1CON < 5 : 4 >). *T osc* . (TMR2 prescale value)