

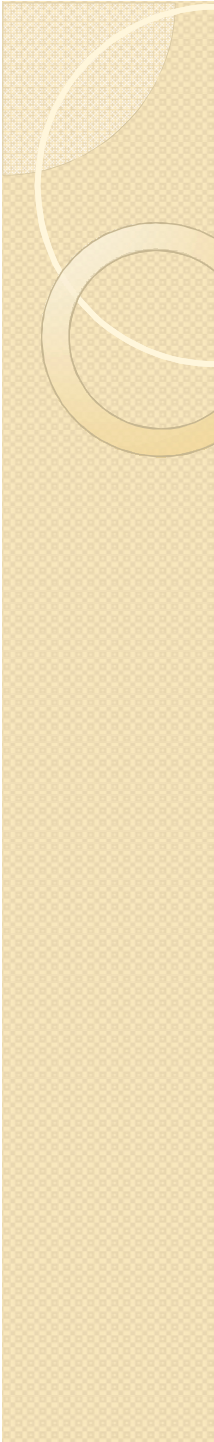
LECTURE 11

PIC



Topics to be covered

- PIC

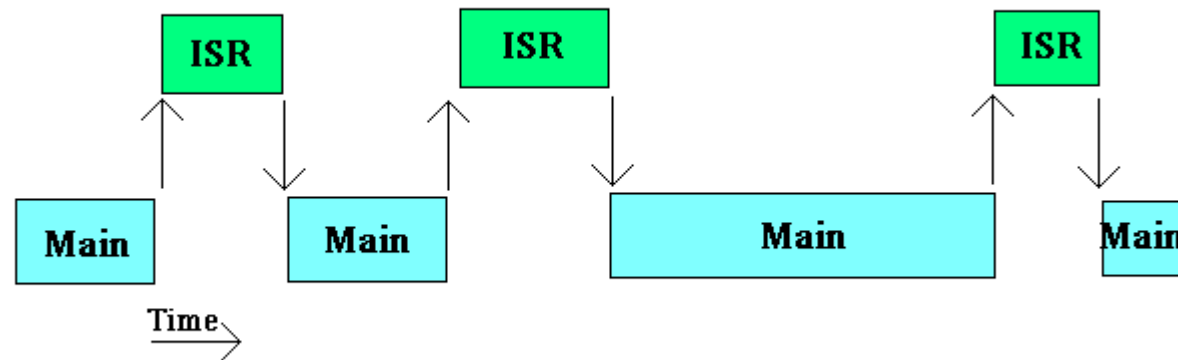
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- **Interrupts**
 - **Interrupts are just *special subroutines that may (or may not)* be called explicitly.**
 - **If conditions are “right”, when an interrupt occurs,**
 - **then the processor will stop what it is doing, and**
 - **jump to a specific place in memory (decided by the**
 - **Intel 8051 designers) hooked by that particular**
 - **interrupt.**
 - **It is up to the programmer to make sure that you**
 - **supply a sensible further course of action. This is**
 - **called the interrupt handler routine or *interrupt***
 - ***service routine , ISR.***

Interrupt :

Program execution without intrrupts :



Program execution with intrrupts :



ISR : Intrrupt Service Routin

INTERRUPTS

All interrupt functions are under the control of the program. The programmer can alter the bits of IE, IP and TCON register.

Each interrupt forces the processor to jump at the interrupt location in the memory.

The interrupted program must resume operation at the instruction where the interrupt took place. Program resumption is done by storing the interrupted PC address on to stack. RETI instruction at the end of ISR will restore the PC address.

Types of Interrupts

Five interrupts are provided on 8051.

3 are generated by internal operations.

Generated by internal timer/counter

Timer flag 0 – TF0

Timer flag 1 – TF1

Indicates that a character has been received or the buffer is empty and a character can be transmitted

Serial port interrupt (RI or TI)

2 are triggered by external signals

INT0~

INT1~

**IN 8052 ONE MORE INTERRUPT IS THERE FOR
TIMER 2.**

INTERRUPTS

INTERRUPT ENABLE REGISTER

- EA- ENABLE/DISABLES THE INTERRUPTS
- -*- RESERVE FOR FUTURE USE.
- ET2- ENABLE OR DISABLE THE TIMER 2 OVERFLOW.
- ES- ENABLE OR DISABLE THE SERIAL PORT INTERRUPT.
- ET1- ENABLE OR DISABLE THE TIMER 1 OVERFLOW
- EX1- ENABLE OR DISABLE EXTERNAL INTERRUPT 1.
- ET0- ENABLE OR DISABLE THE TIMER 0 OVERFLOW
- EX0- ENABLE OR DISABLE EXTERNAL INTERRUPT 0.