Dronacharya College of Engineering, Gurgaon

Department of Electronics and Computers Engineering

Subject:Digital Electronics(EC-412-F) **Semester/Branch: IV** ECS

Short Answer questions

Section A

Q1 Combinational circuits are adders, subtractors, multiplexers, demultiplexer, magnitude comparator, parity generator/checker etc.

Q2. Arithmetic circuits are used for addition, subtraction multiplication division

Q3. Half adder is used for addition of two binary numbers.

Q4. Full adder is used to perform addition of more than 2 bits

Q5. Serial adder require one full adder for one additional bit while parallel adders requires N full adders for n bit addition.

Section B

Q1 Two more adders are look ahead carry adder why?.

Q2 Half subtractor subtracts two numbers we get 2 output variables i e difference and borrow give demonstration.

Q3 Full subtractor is subtraction of 3 bits how?.

Q4 Encoder converts human language into machine language give examples.

Q5 Decoder is used to convert machine language to human language give examples.

Q6 Multiplexers are universal circuits which selects one input out of multiple inputs and give it as a result, prove it by taking an example.

Q7 Demultiplexer receives information on single line and distribute to the 2 lines where n are selection lines.

Section C

Q 1. List the applications of decoders.

Ans. 1 Decoders are used in counter systems

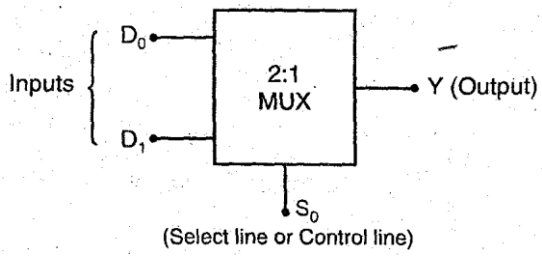
2. Decoders are used for A/D conversion.

3 Decoders are used for D/A conversion

4. Decoders are used in seven segment digital displays.

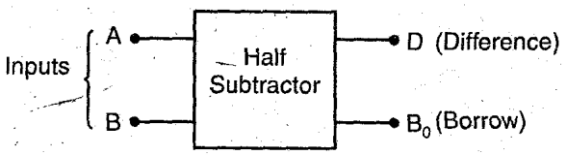
Q 2 Give functional block diagram of 2 1 MUX

Ans.



Q 3 Explain half subtractor with the help of its internal circuit

Ans. To subtract two numbers i e two Input variables A and B we get two output variable i e difference 'D' and borrow 'Bo' It is known as half subtractor Functional diagram is shown:



Its truth table is as shown:

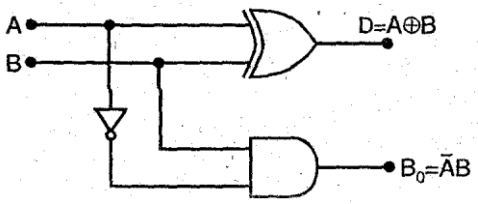
Inputs		Outputs	
A	**B**	**D**	**B_0**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Thus, the minimized logic functions are:

$$D = \bar{A}B + A\bar{B} = A \oplus B$$

$$B_0 = \bar{A}B$$

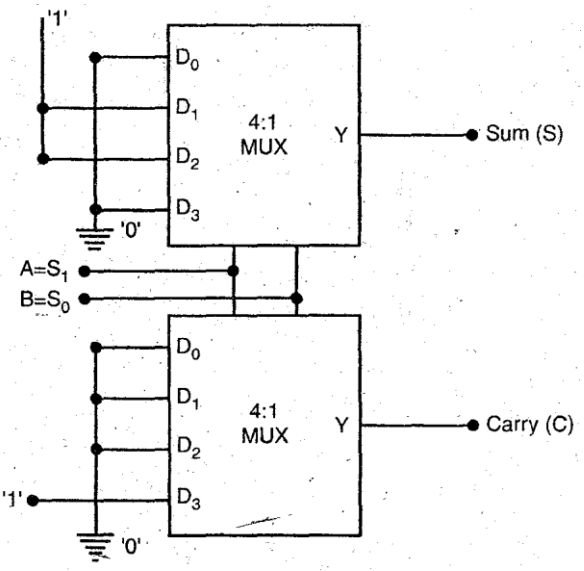
The circuit diagram is as shown:



Q 4. Implement half adder circuit using 4 : 1 MUX or multiplexers only.

Ans. Truth table of half adder is as shown:

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Section D

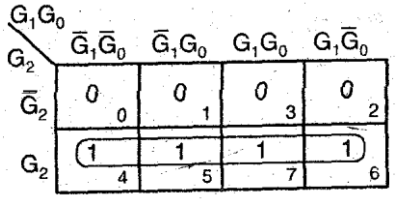
Q1**. Design 3 bit Gray Code to binary converters**

Ans. The truth table for 3 bit Gray Code to binary conversion is as shown:

Decimal Equipment	Gray Code			Binary Code		
	G_2	G_1	G_0	B_2	B_1	B_0
0	0	0	0	0	0	0
1	0	0	1	0	0	1
3	0	1	1	0	1	0
2	0	1	0	0	1	1
6	1	1	0	1	0	0
7	1	1	1	1	0	1
5	1	0	1	1	1	0
4	1	0	0	1	1	1

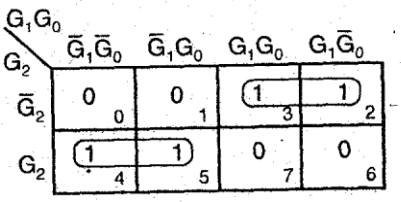
K-Maps:

For B2:



$\therefore B_2 = G_2$

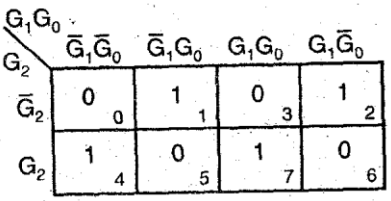
For B1:



$\therefore B_1 = \bar{G}_2 G_1 + G_2 \bar{G}_1$

$B_1 = G_1 \oplus G_2$

For Bo:



$$\therefore B_0 = \bar{G}_2 \bar{G}_1 G_0 + \bar{G}_2 G_1 \bar{G}_0 + G_2 \bar{G}_1 \bar{G}_0 + G_2 G_1 G_0$$

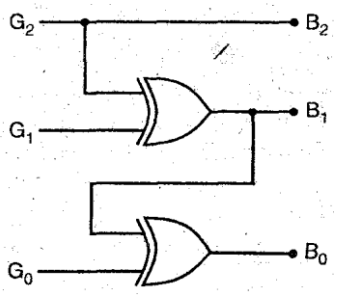
$$= \bar{G}_2 \left(\bar{G}_1 G_0 + G_1 \bar{G}_0\right) + G_2 \left(\bar{G}_1 \bar{G}_0 + G_1 G_0\right)$$

$$= \bar{G}_2 \left(G_1 \oplus G_0\right) + G_2 \left(G_1 \odot G_0\right)$$

$$= \bar{G}_2 \left(G_1 \oplus G_0\right) + G_2 \left(\overline{G_1 \oplus G_0}\right)$$

$\therefore B_0 = G_1 \oplus G_0 \oplus G_2.$

Circuit Implementation is as shown:



Q 2. Design BCD to Excess-3 code converter.

Ans. BCD to Excess-3 Code Converter:

The input variables are BCD's (A, B, C and D) and output variables are excess-3 code (E3, E2, E1 and E0)