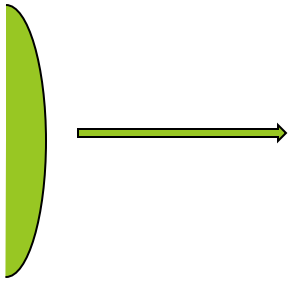
LECTURE 17

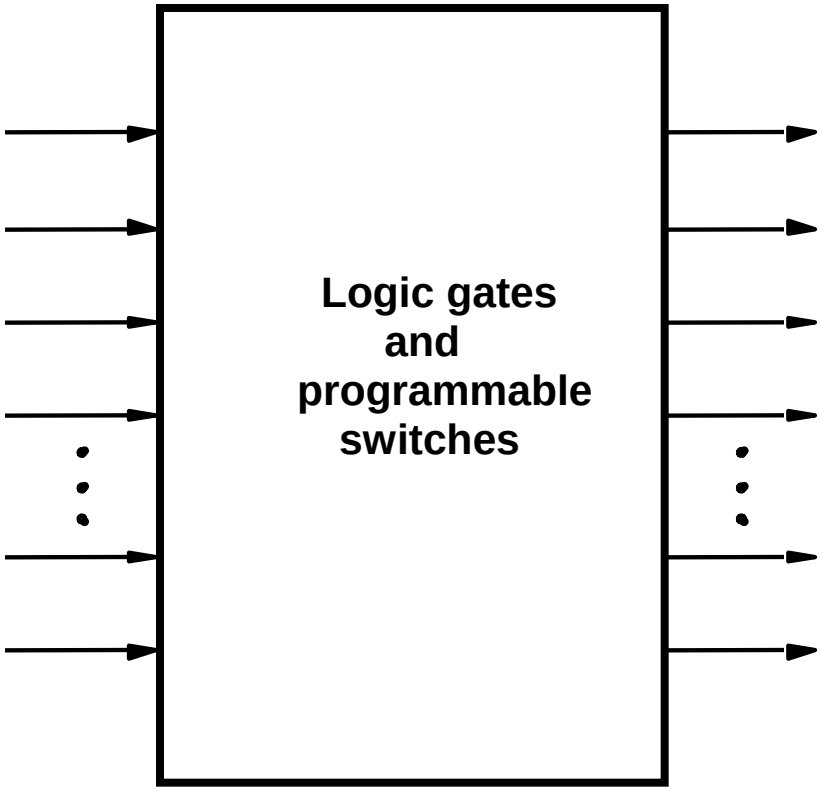
COMBINATIONAL DESIGN USING MSI DEVICES

- PLDs

  - Programmable Logic Devices (PLD)
    - General purpose chip for implementing circuits
    - Can be customized using programmable switches
  - Programmable devices have their functionality programmed before they are first used.
  - Range in complexity from 100's to 10,000's of logic gates.
  - Main types of PLDs
    - ROM
    - PLA
    - PAL Simple/Sequential Prog Logic Devices
    - CPLD (Complex Prog. Logic Devices)
    - FPGA (Field Prog Gate Array)
  - Custom chips: standard cells, sea of gates

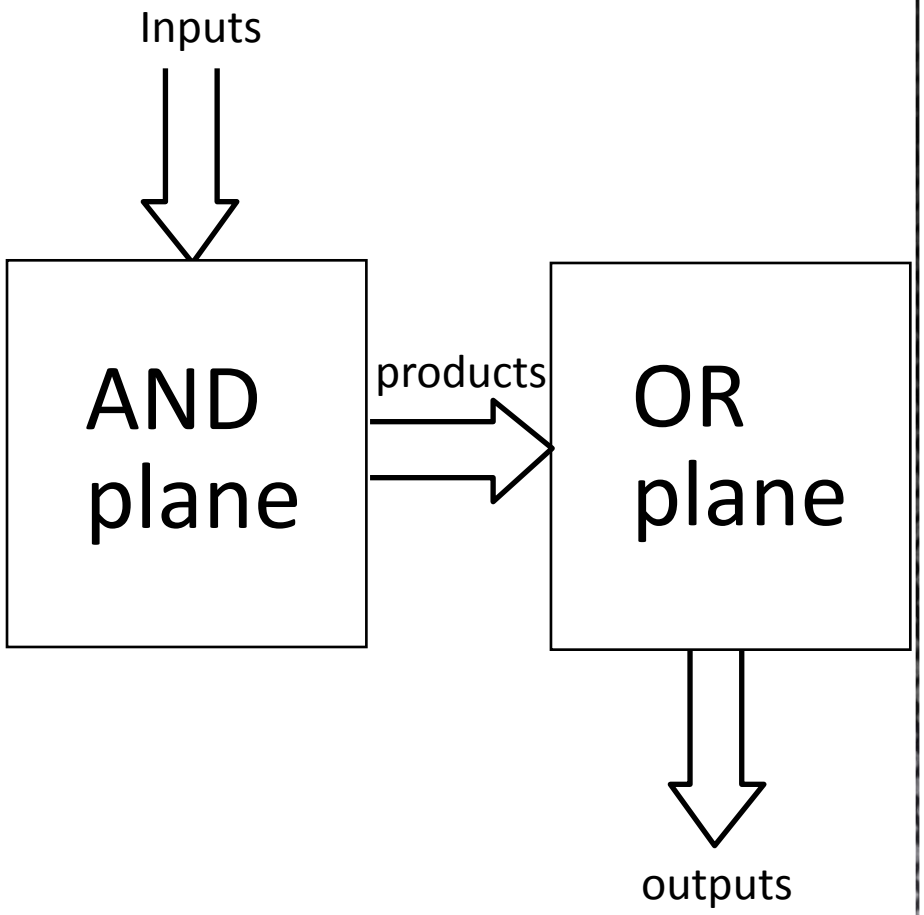


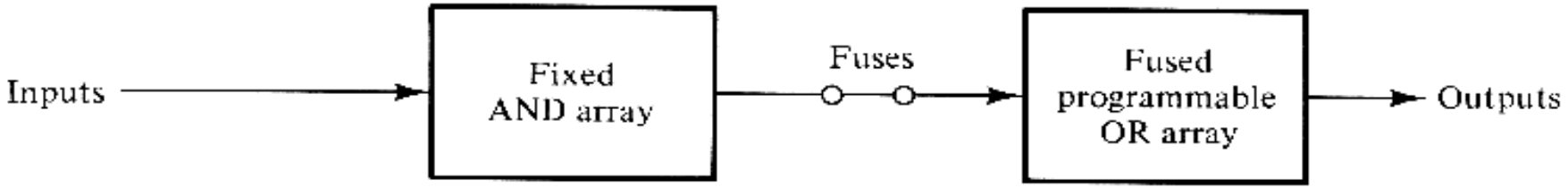
- PLD as a Black Box



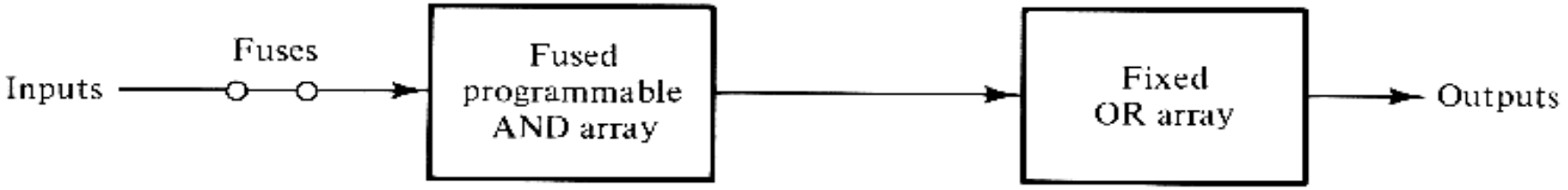
PLD's

Most of these devices are based on a two level structure (sum of products form).

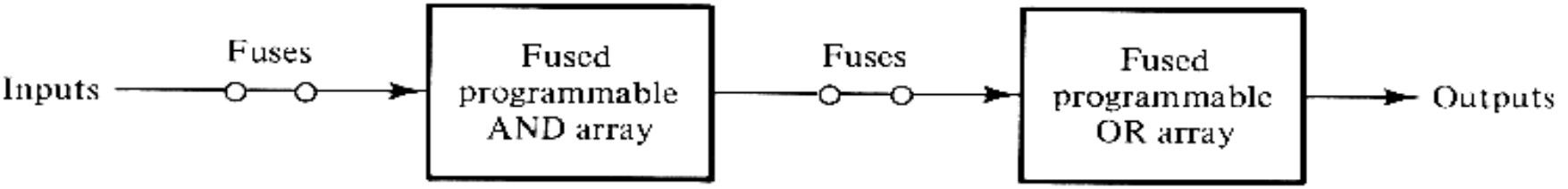




(a) Programmable read-only memory (PROM)



(b) Programmable array logic (PAL)



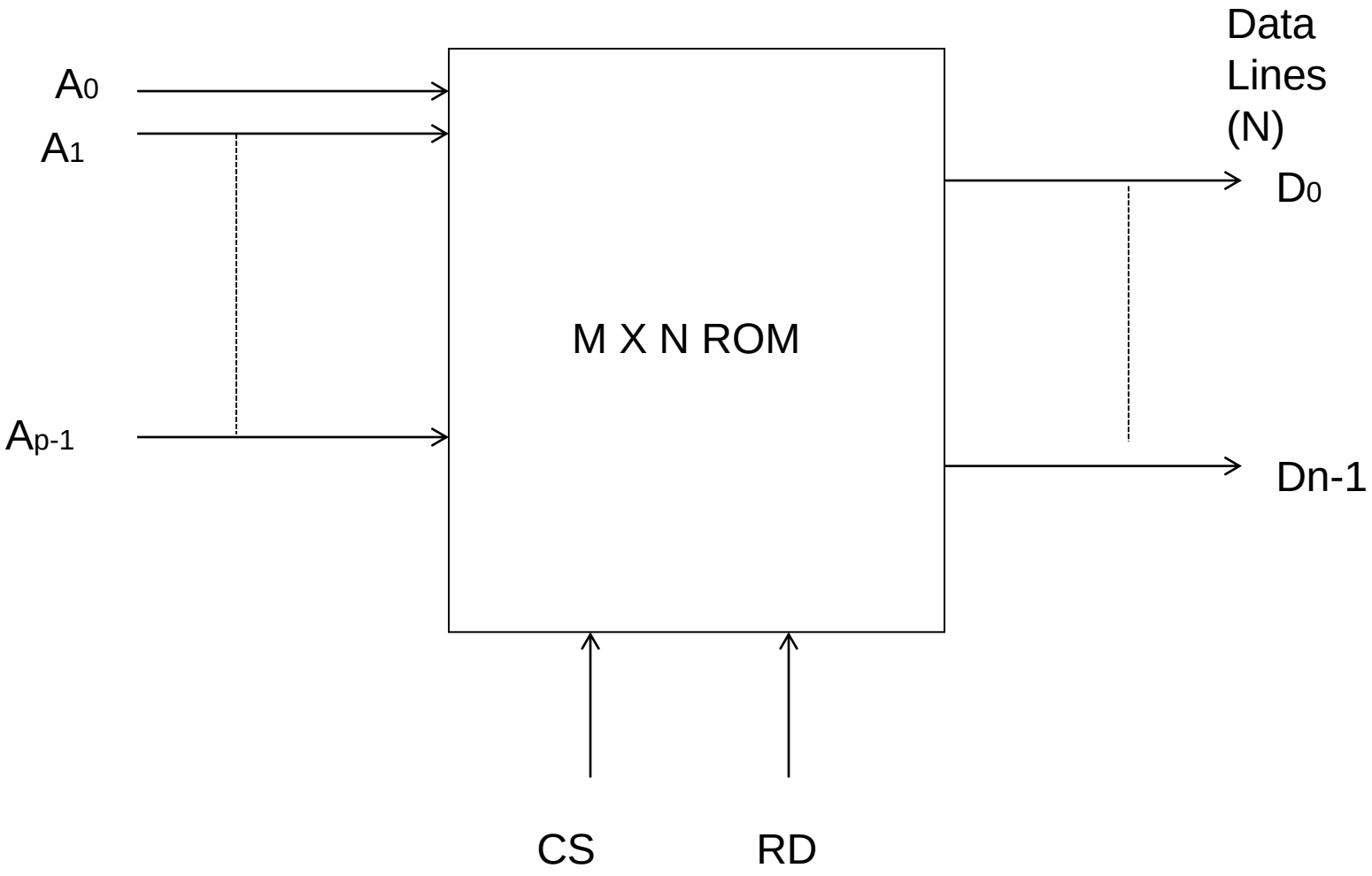
(c) Programmable logic array (PLA)

- ROM
  - A ROM (Read Only Memory) has a fixed AND plane and a programmable OR plane
  - Size of AND plane is 2^n where n = number of input pins
    - Has an AND gate for every possible minterm so that all input combinations access a different AND gate
  - OR plane dictates function mapped by the ROM

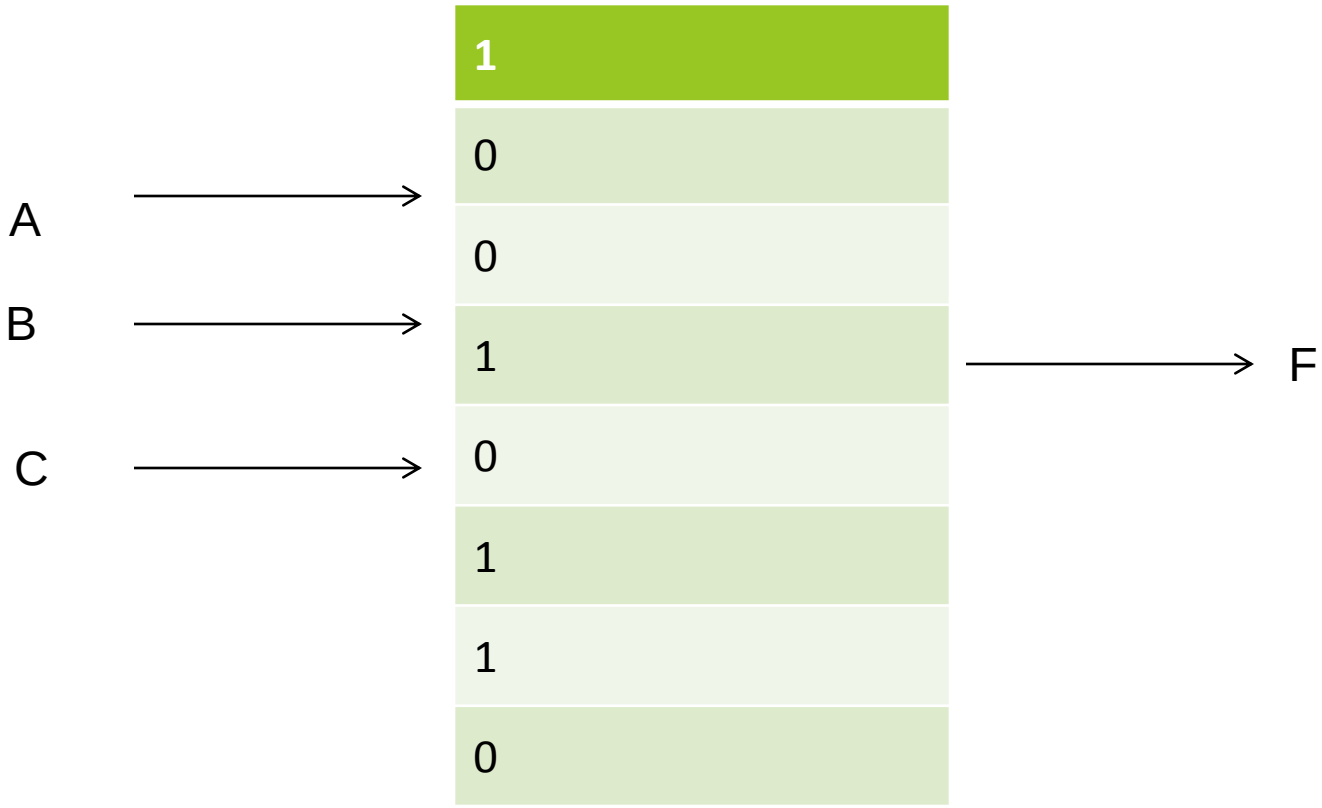
- ROM
  - a memory device of permanent b

  - P input lines: address lines
  - 2^p distinct addresses = M locations
  - N of bits at each location = Data
  - n output lines: word (no of bits stored data)
  - CS Signal – Chip Select Signal
  - RD Signal – Read Signal

Address Lines (P) such that $2^P >= M$ (M is no of locations)

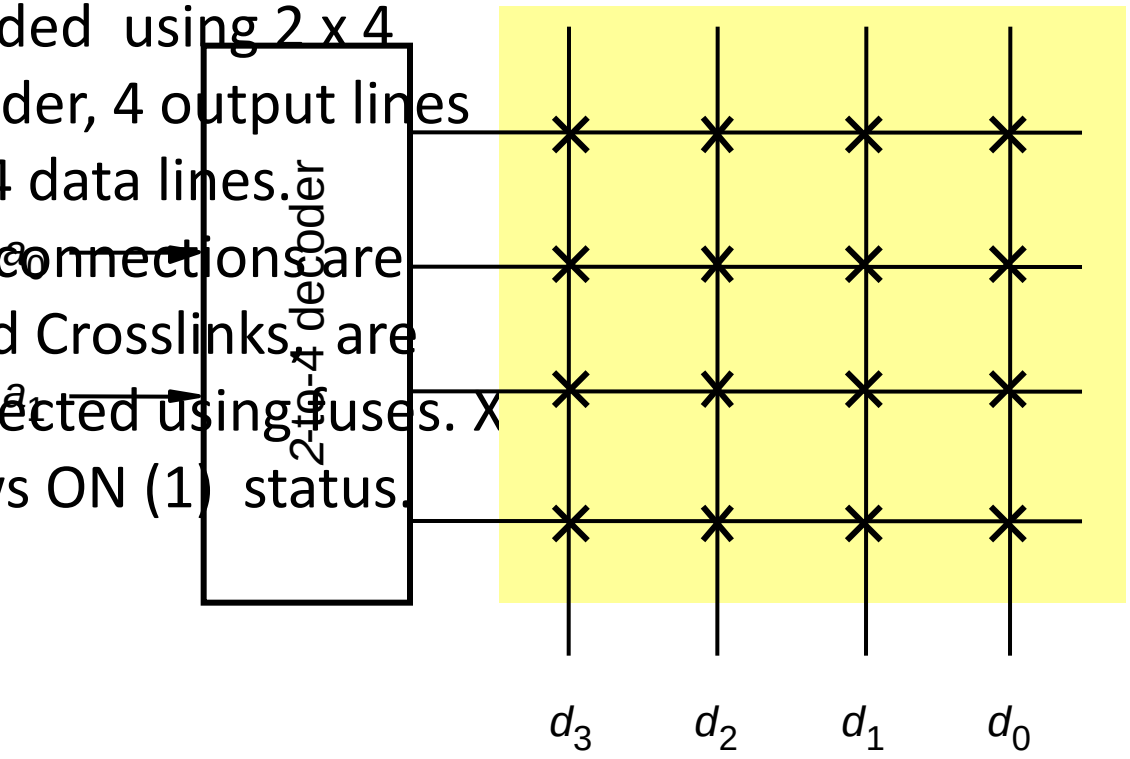


$F(A,B,C) = \Sigma(0,3,5,6)$

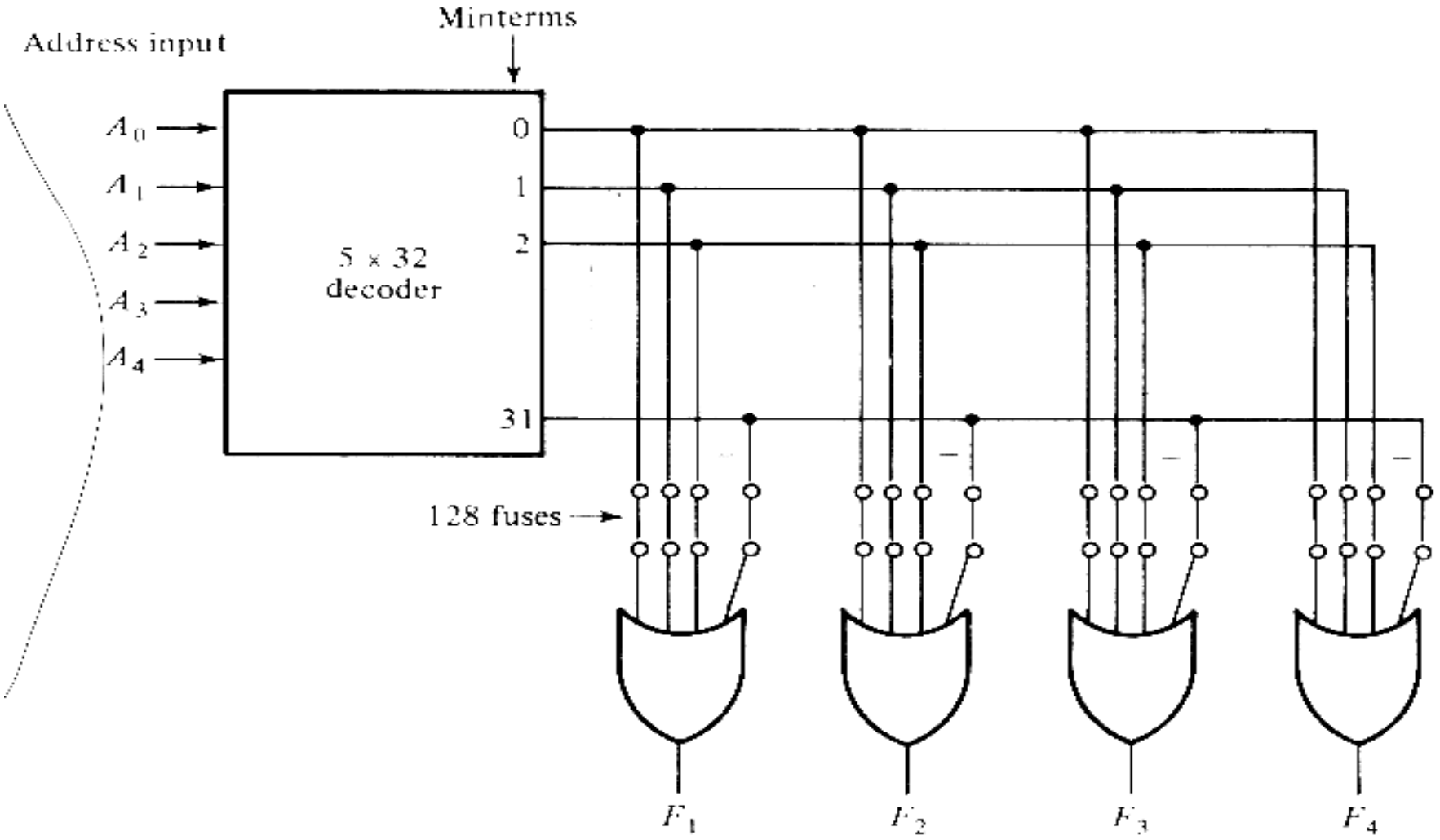


- a M x N decoder is used to select the location
- plus m OR gates
- can be used to implement any Boolean functions of n input variables
- a fixed AND array and a programmable OR array

- 4x4 ROM
  - 4x4 ROM has 4 addresses that are decoded using 2 x 4 Decoder, 4 output lines and 4 data lines. Interconnections are called Crosslinks, are connected using fuses. X shows ON (1) status.



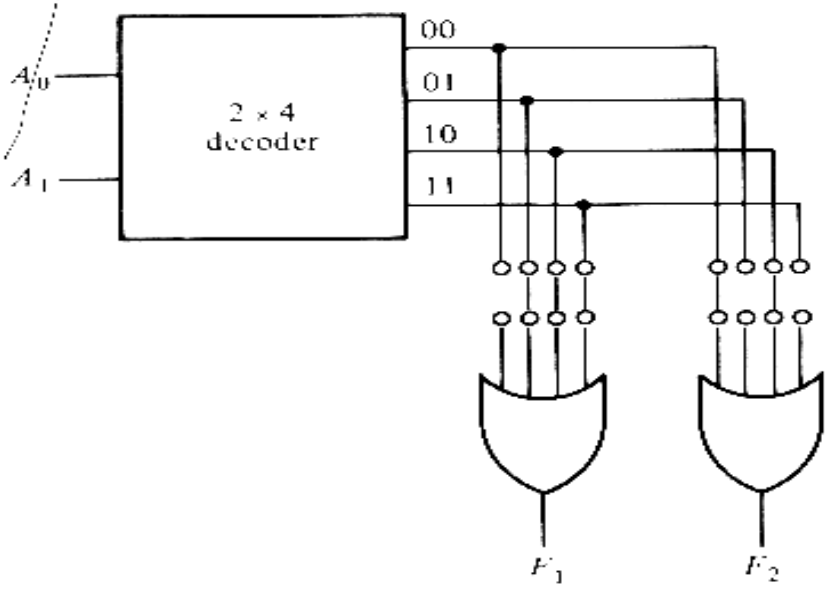
- A 32x4 ROM


Minterms
Address input
A_0
A_1
A_2
A_3
A_4
5 × 32
decoder
0
1
2
31
128 fuses
F_1
F_2
F_3
F_4

- combinational logic Circuit implementation
  - store the truth table in a ROM

A_1	A_0	F_1	F_2
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	0

(a) Truth table



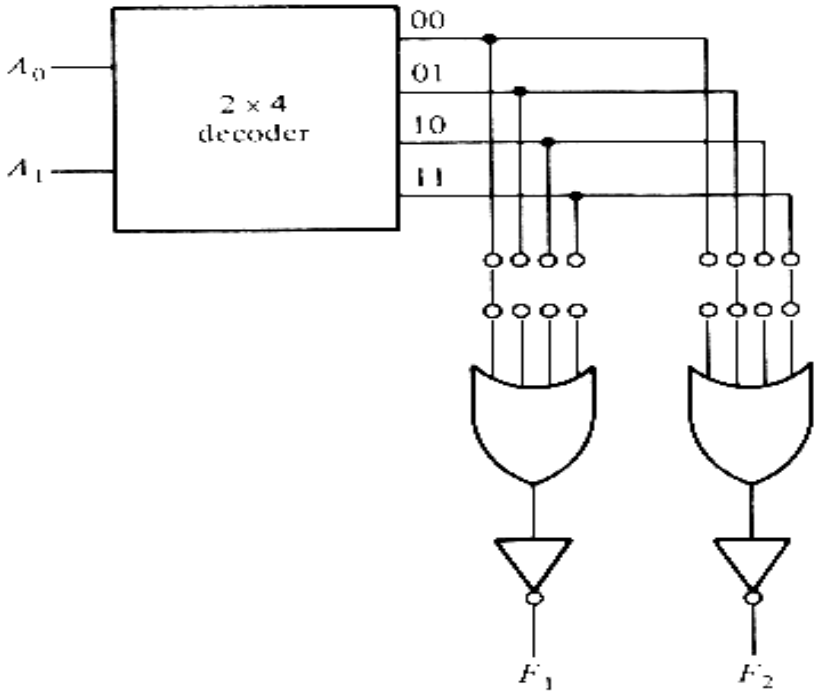
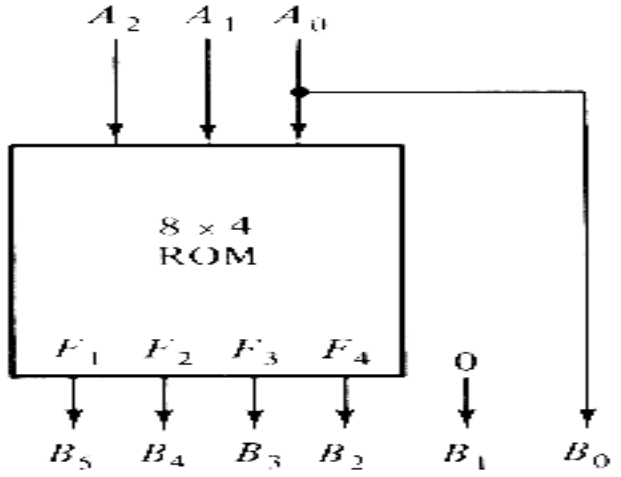


TABLE 5-5
Truth Table for Circuit of Example 5-3

Inputs			Outputs						
A_2	A_1	A_0	B_5	B_4	B_3	B_2	B_1	B_0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49



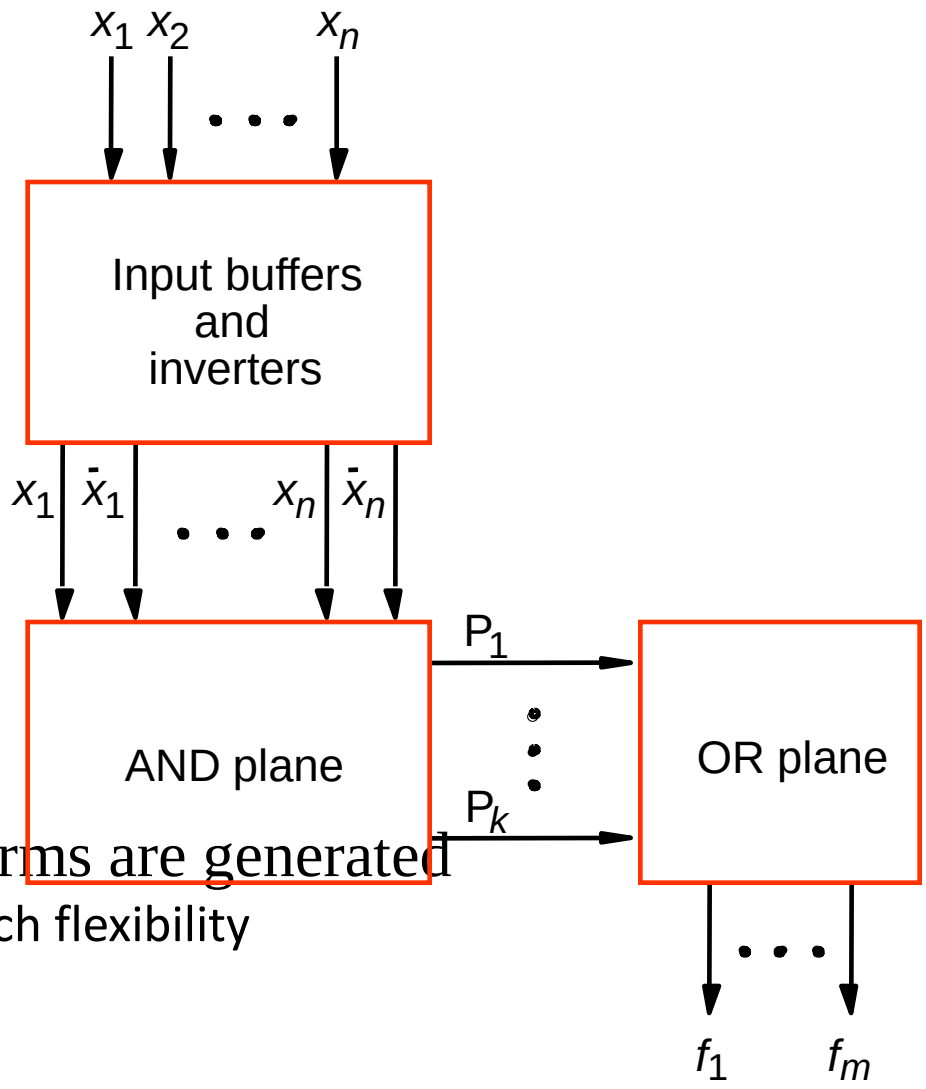
(a) Block diagram

A_2	A_1	A_0	F_1	F_2	F_3	F_4
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

(b) ROM truth table

- Types of ROMs
  - mask programming ROM
    - IC manufacturers
    - is economical only if large quantities
  - PROM: Programmable ROM
    - fuses
    - universal programmer
  - EPROM: erasable PROM
    - floating gate
    - ultraviolet light erasable
  - EEPROM: electrically erasable PROM
    - longer time is needed to write
    - flash ROM
    - limited times of write operations

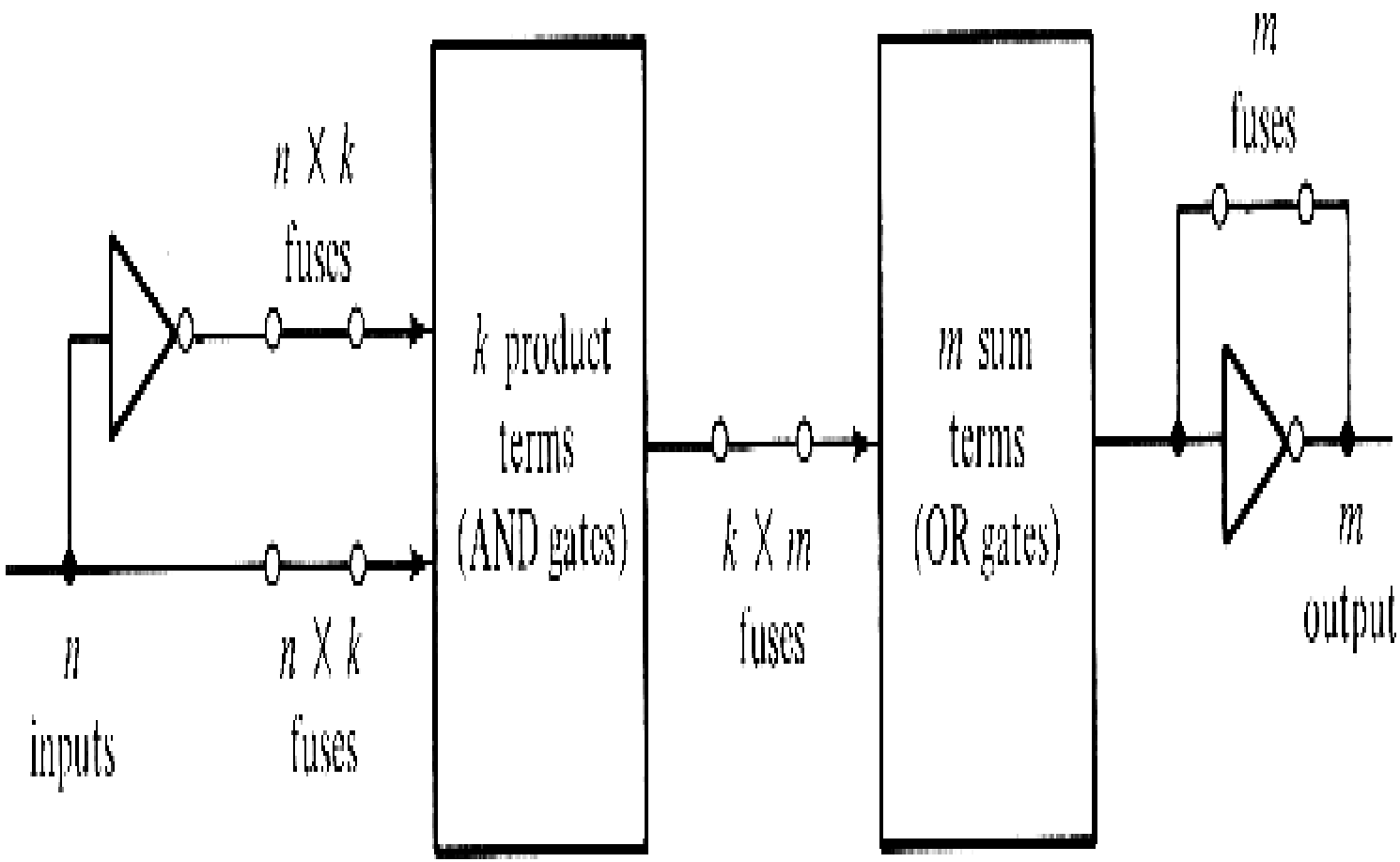
- Programmable Logic Array (PLA) – (Both Array are programmable)
  - Use to implement circuits in SOP form
  - The connections in the AND plane are programmable
  - The connections in the OR plane are programmable



only the needed product terms are generated

- Many applications don't require such flexibility

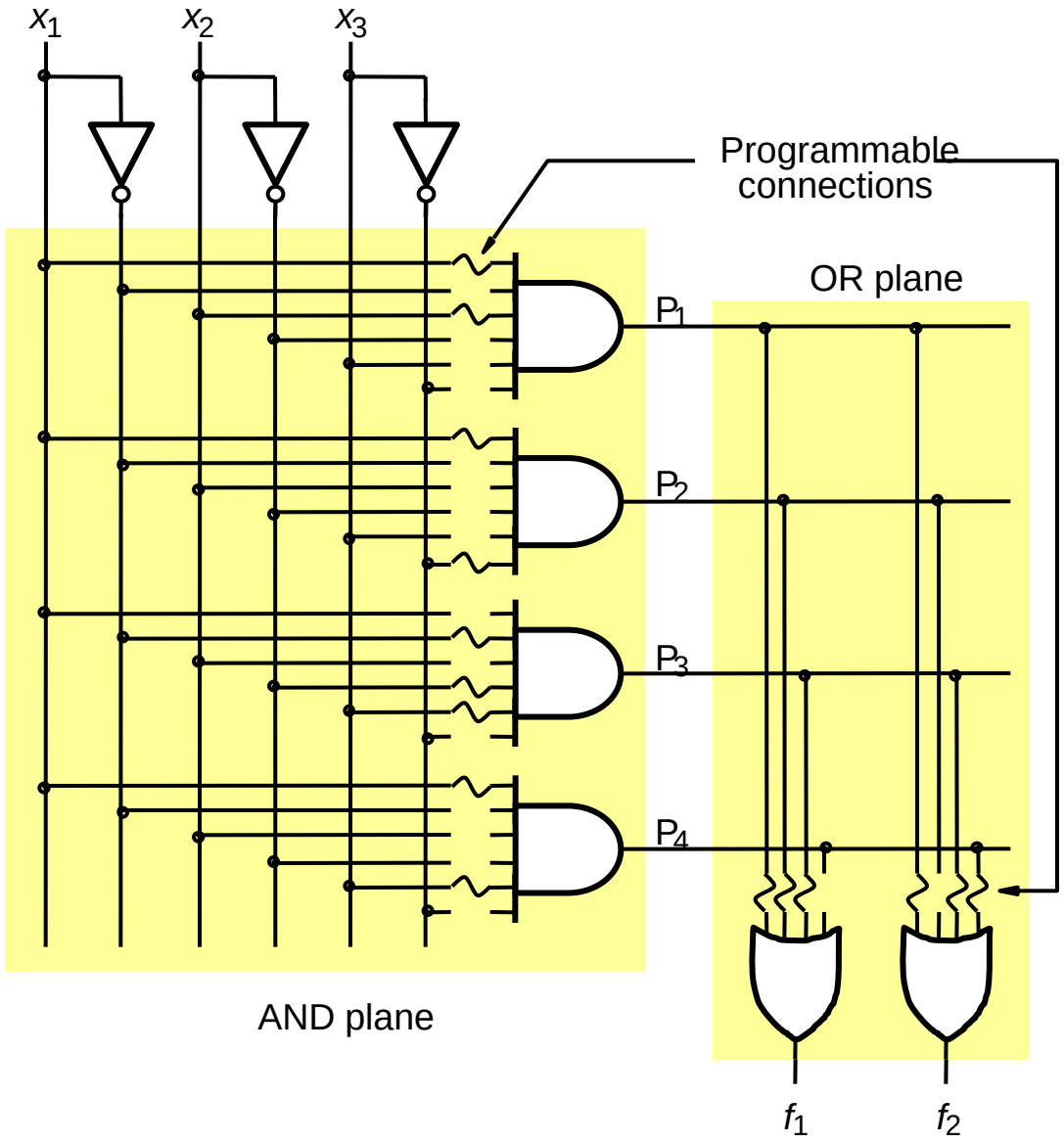
PLA


n X k
fuses
k product
terms
(AND gates)
k X m
fuses
m sum
terms
(OR gates)
m
fuses
m
output
n
inputs
n X k
fuses

$f_1 = x_1x_2+x_1x_3'+x_1'x_2'x_3$

- Gate Level Version of PLA

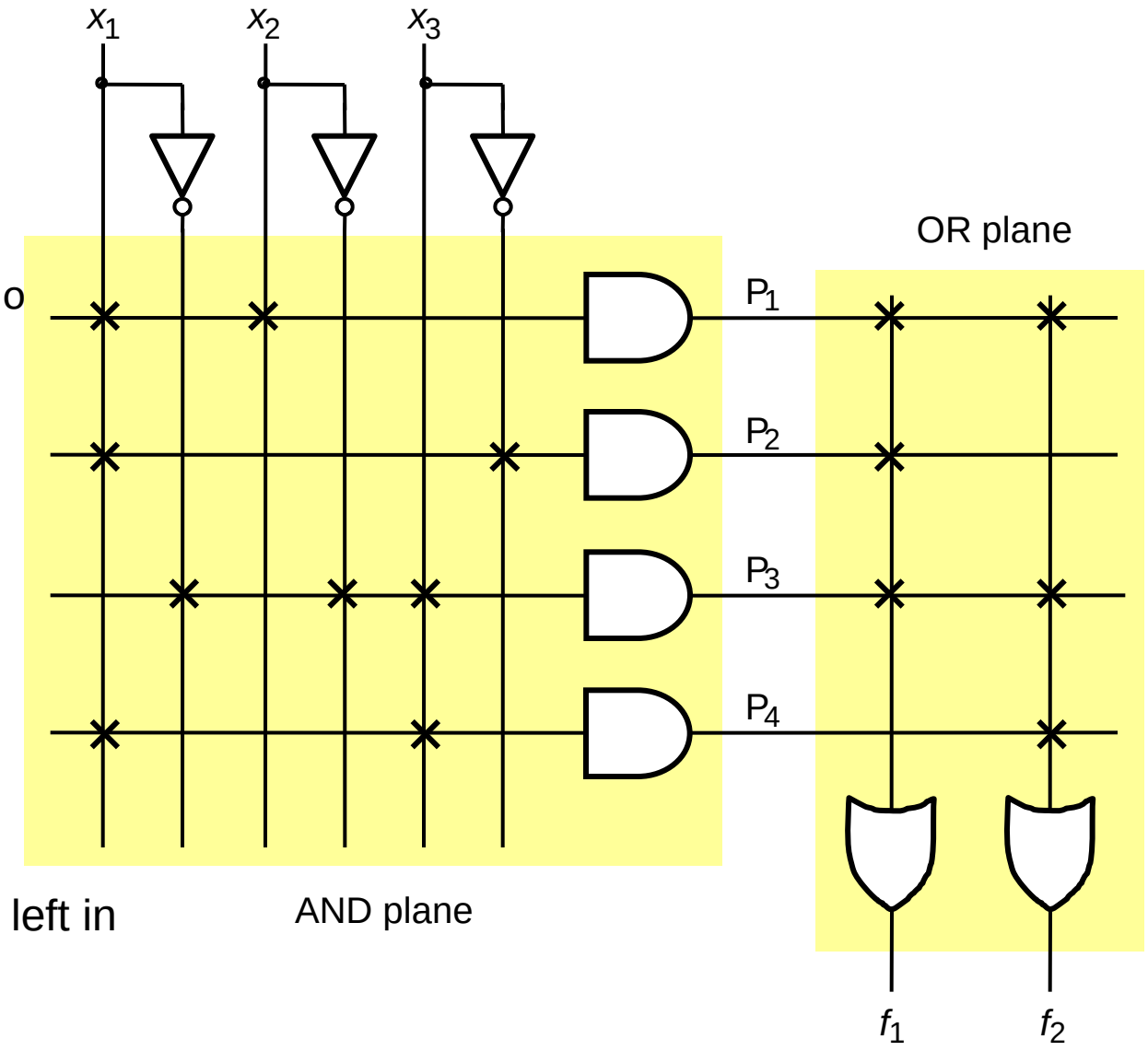
$f_2 = x_1x_2+x_1'x_2'x_3+x_1x_3$



$f_1 = x_1x_2+x_1x_3'+x_1'x_2'x_3$

- Customary Schematic o

$f_2 = x_1x_2+x_1'x_2'x_3+x_1x_3$



x marks the connections left in place after programming

Advantages of PLA:

- Both AND and OR array are programmable,
- It gives flexibility for implementation of Logic design.
- Included as a part of larger chips such as microprocessors.
- Power requirement is less than ROM.
- Cost is also less.

Disadvantages:

Simplification of boolean expression is required.