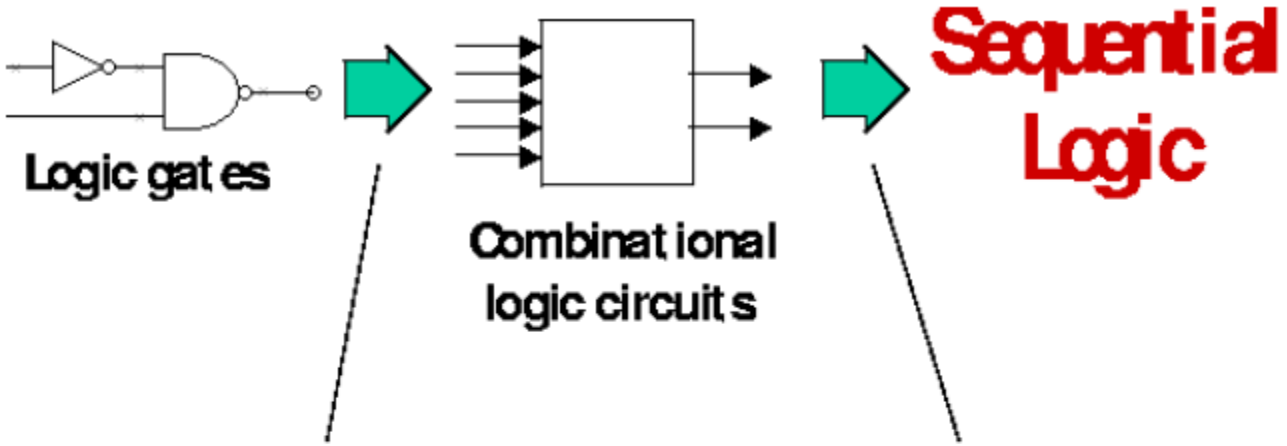
LECTURE 9

COMBINATIONAL DESIGN USING MSI DEVICES

Sequential Circuits Problems

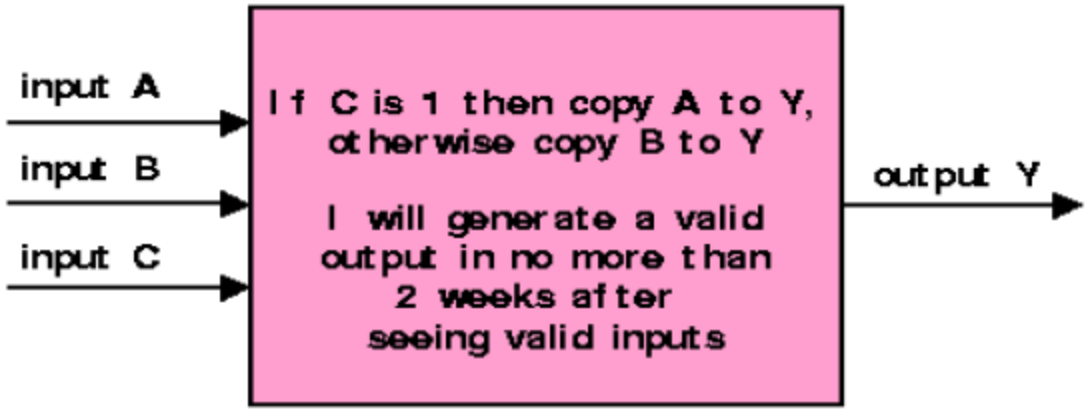


Acyclic connections
Composable blocks
Design:
- truth tables
- sum-of-products
- simplification
- muxes, ROMs, PLAs

Storage & state
Dynamic discipline
Finite-state machines
Metastability
Throughput & latency
Pipelining

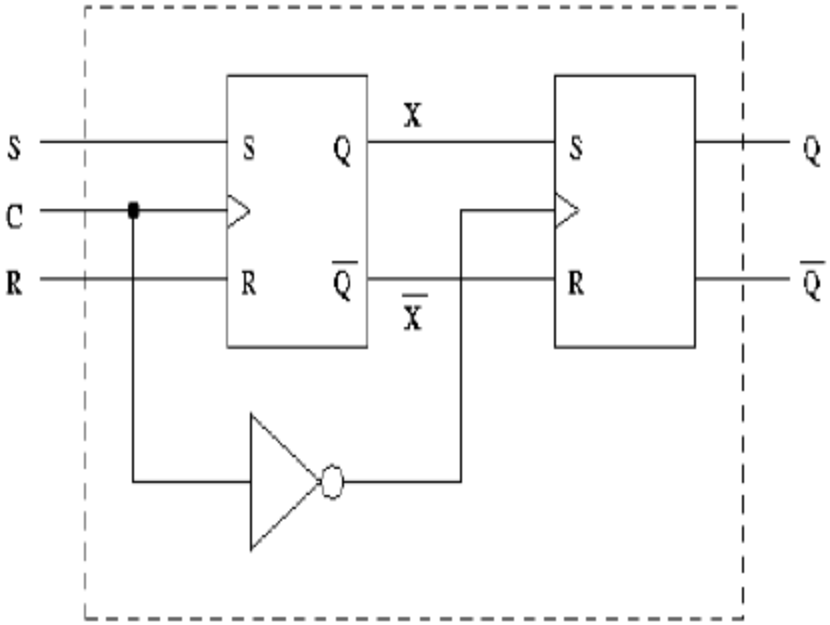
- A *combinational device* is a circuit element that has
  - one or more digital *inputs*
  - one or more digital *outputs*
  - a *functional specification* that details the value of each output for every possible combination of valid input values
  - a *timing specification* consisting (at minimum) of an upper bound t_{pd} on the required time for the device to compute the specified output values from an arbitrary set of stable, valid input values

Static discipline



SR Master-Slave Flip-Flop

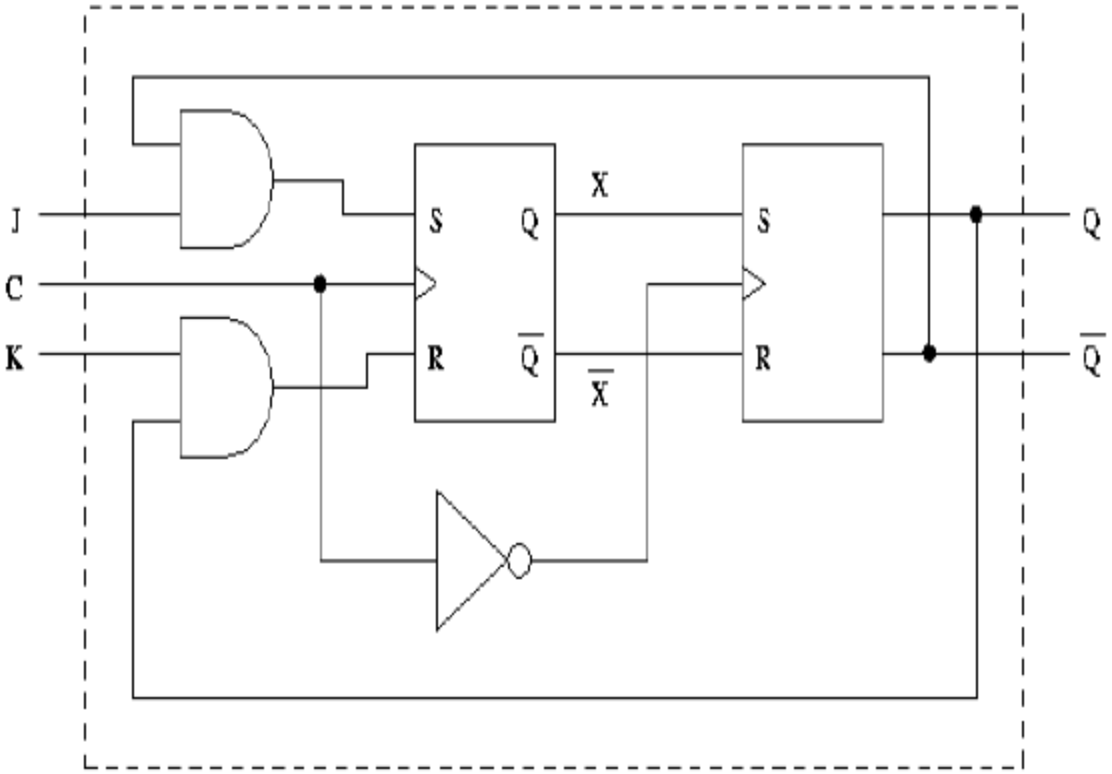
The SR Master-Slave Flip-Flop is constructed from two SR latches and an inverter



The left hand latch is called the *master* and the right hand latch the *slave*.

JK Flip-Flop

The *JK flip-flop* is constructed from and is similar in operation to the SR flip-flop. The circuit is



J	K	Q	Q^+
0	0	x	Q
0	1	x	0
1	0	x	1
1	1	x	$\overline{Q}$

For three of the four possible input combinations the operation is identical to the SR. The difference lies in the case where the two inputs are both 1. In