LECTURE 8

COMBINATIONAL DESIGN USING MSI DEVICES

Clock Signal

Sequential logic circuits have memory
Output is a function of input and present state
Sequential circuits are synchronized by a periodic “clock” signal

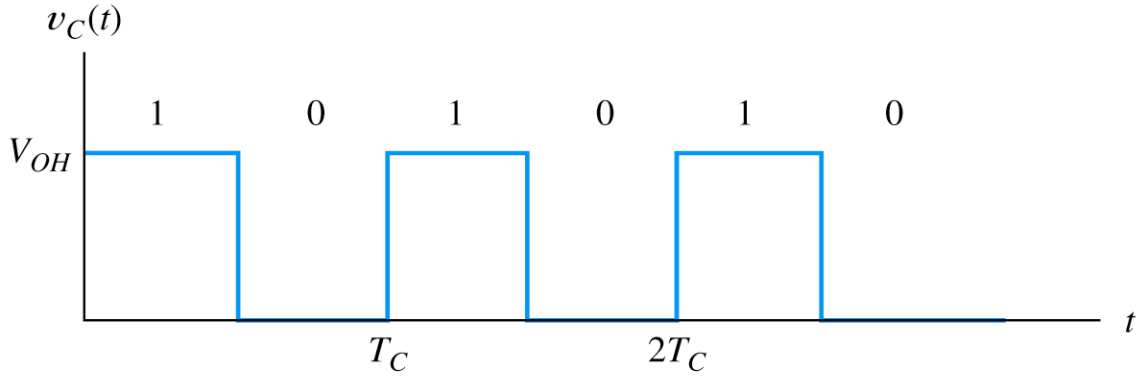
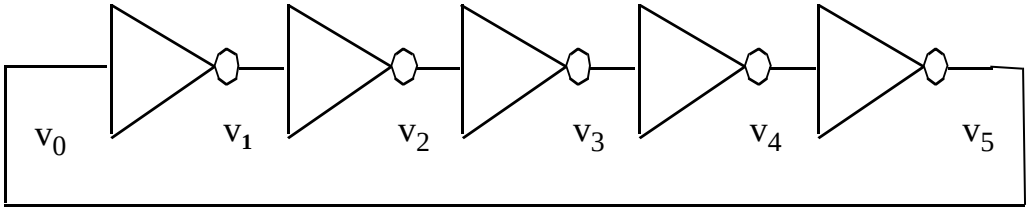
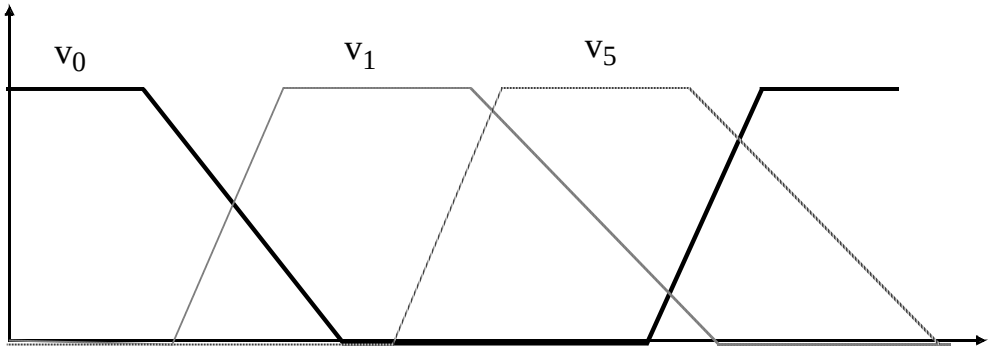


Figure 7.33 The clock signal consists of periodic logic-1 pulses.

Clock Signal generator

Clock signals can be generated using odd number of inverters





$$T = 2 \times t_p \times N$$

Flip Flop

A basic sequential circuit is a flip-flop
Flip-flop has two stable states of complementary output values

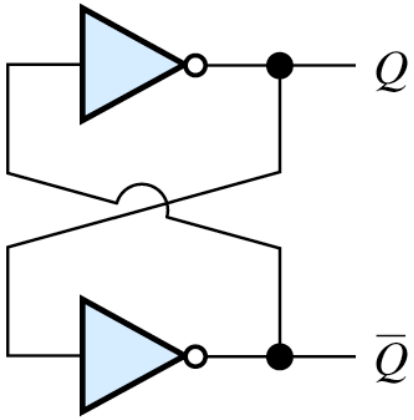


Figure 7.34 Simple flip-flop.

SR Flip Flop

SR (set-reset) flip-flop based on two nor gates

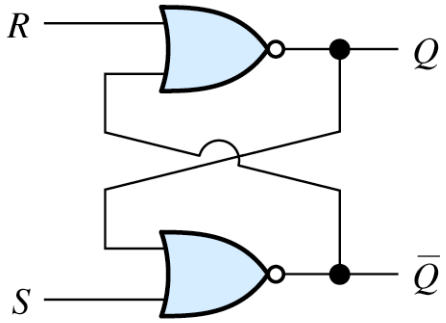


Figure 7.35 An SR flip-flop can be implemented by cross coupling two NOR gates.

SR Flip Flop

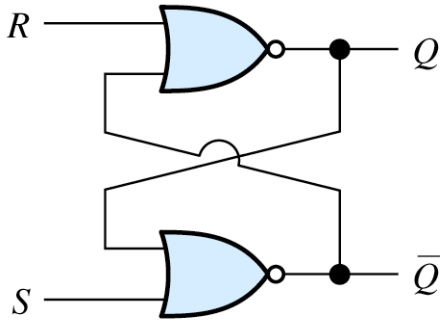
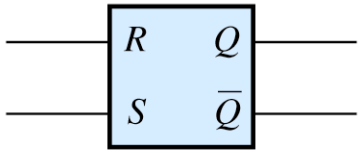


Figure 7.35 An SR flip-flop can be implemented by cross coupling two NOR gates.

R	S	Q_n
0	0	Q_{n-1}
0	1	1
1	0	0
1	1	Not allowed

(a) Truth table

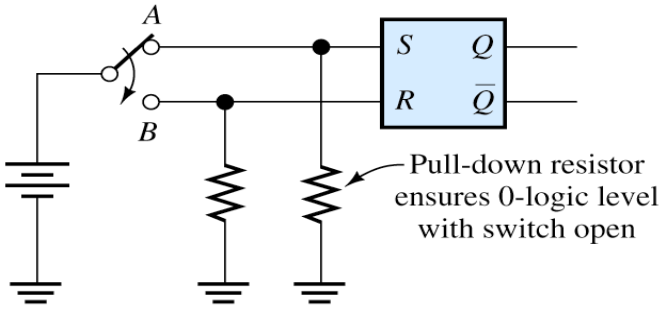


(b) Circuit symbol

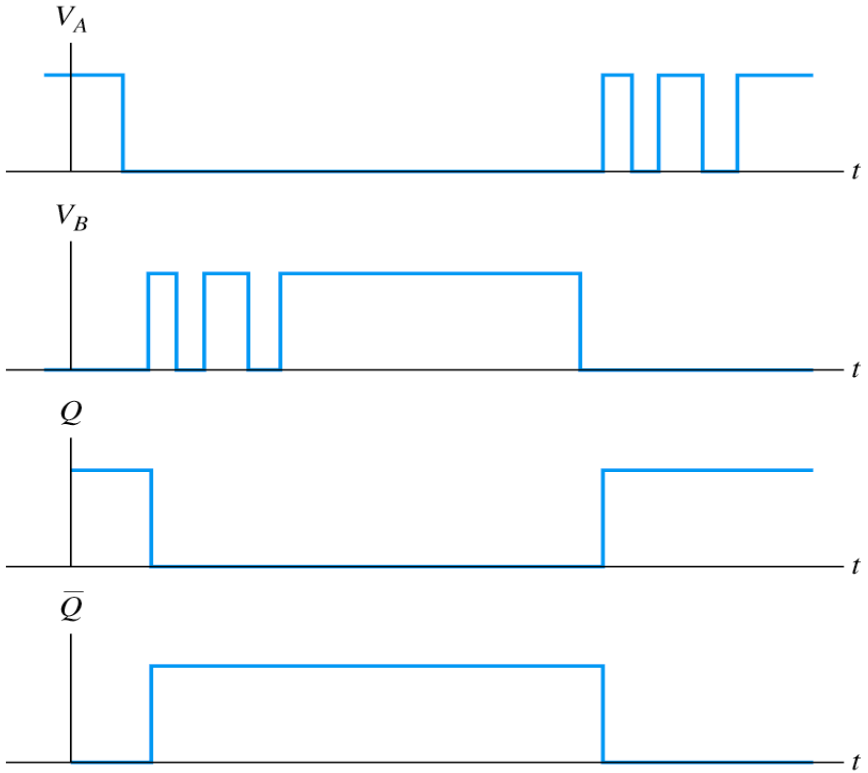
Figure 7.36 The truth table and symbol for the SR flip-flop.

Noise Reduction in SR Flip Flop

SR flip flop can reduce a switching noise
When switch is pulled down some oscillations may occur at B
They will be eliminated by the flip-flop



(a) Circuit diagram



(b) Waveforms

Figure 7.37 An SR flip-flop can be used to eliminate the effects of switch bounce.

Exercise

For a given S and R inputs to SR flip-flop,
sketch the output signal Q

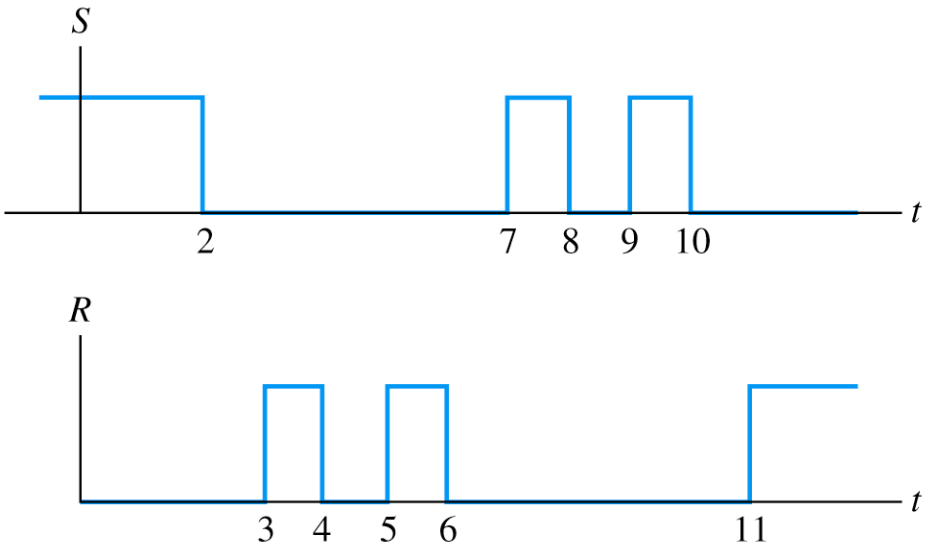


Figure 7.38 See Exercise 7.18.

Exercise

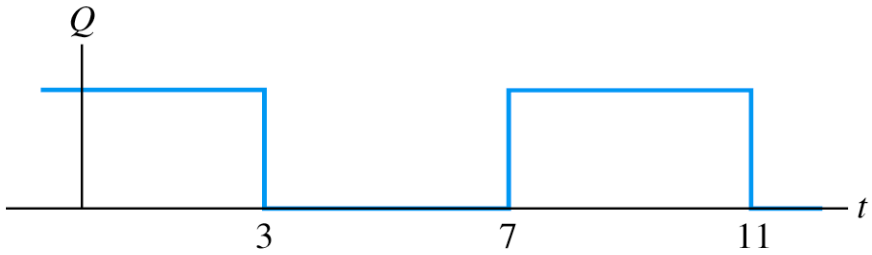


Figure 7.39 Answer for Exercise 7.18.

SR Flip Flop

SR (set-reset) flip-flop based on two nand gates

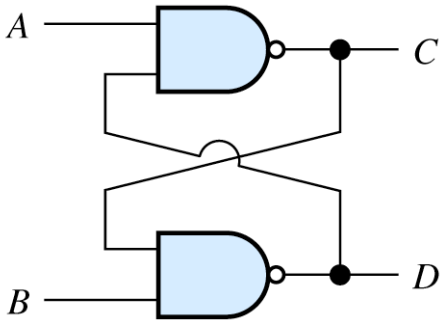
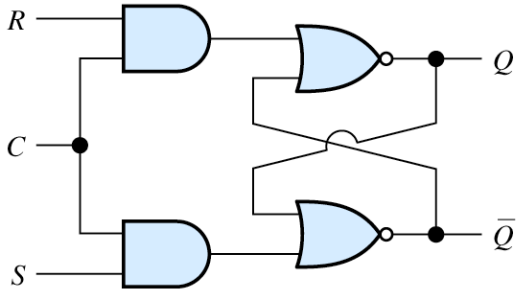


Figure 7.40 A flip-flop implemented with NAND gates. See Exercise 7.19.

Clocked SR Flip Flop Circuit

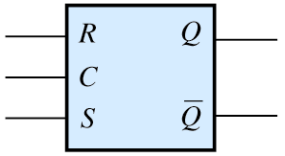
Clock controlled flip-flop changes its state only when the clock C is high



(a) Circuit diagram

R	S	C	Q_n
0	0	×	Q_{n-1}
0	1	1	1
1	0	1	0
1	1	1	Not allowed
×	×	0	Q_{n-1}

(b) Truth table

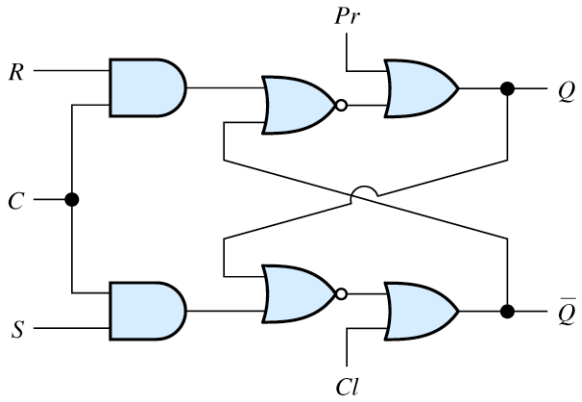


(b) Circuit symbol

Figure 7.41 A clocked SR flip-flop.

Clocked SR Flip Flop Circuit with Reset

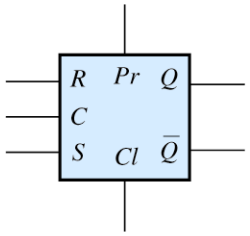
Some flip-flops have asynchronous
preset Pr and clear Cl signals.
Output changes once these signals change, however
the input signals must wait for a change in clock
to change the output



(a) Circuit diagram

Pr	Cl	R	S	C	Q_n
0	0	0	0	×	Q_{n-1}
0	0	0	1	1	1
0	0	1	0	1	0
×	×	1	1	1	Not allowed
0	1	×	×	×	0
1	0	×	×	×	1
1	1	×	×	×	Not allowed

(b) Truth table



(c) Circuit symbol

Figure 7.42 A clocked SR flip-flop with asynchronous preset and clear inputs.

Edge Triggered Flip Flop

Edge triggered flip-flop changes only when the clock C changes

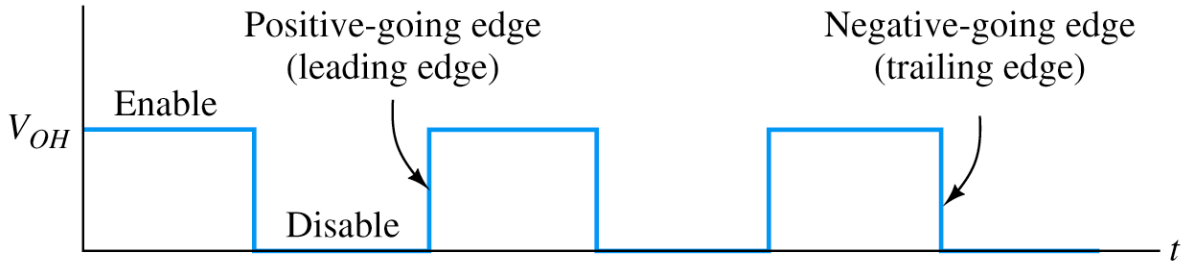
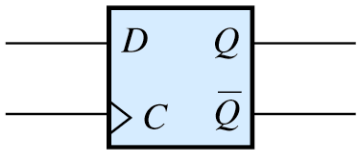


Figure 7.43 Clock signal.

Positive Edge Triggered Flip Flop

Positive-edge triggered flip-flop changes only on the rising edge of the clock C



(a) Circuit symbol

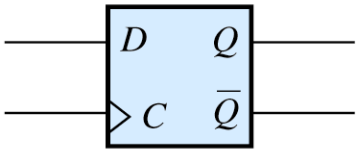
C	D	Q_n
0	×	Q_{n-1}
1	×	Q_{n-1}
↑	0	0
↑	1	1

(b) Truth table
↑ indicates a transition from low to high

Figure 7.44 A positive-edge-triggered D flip-flop.

Exercise

The input D to a positive-edge triggered flip-flop is shown
Find the output signal Q



(a) Circuit symbol

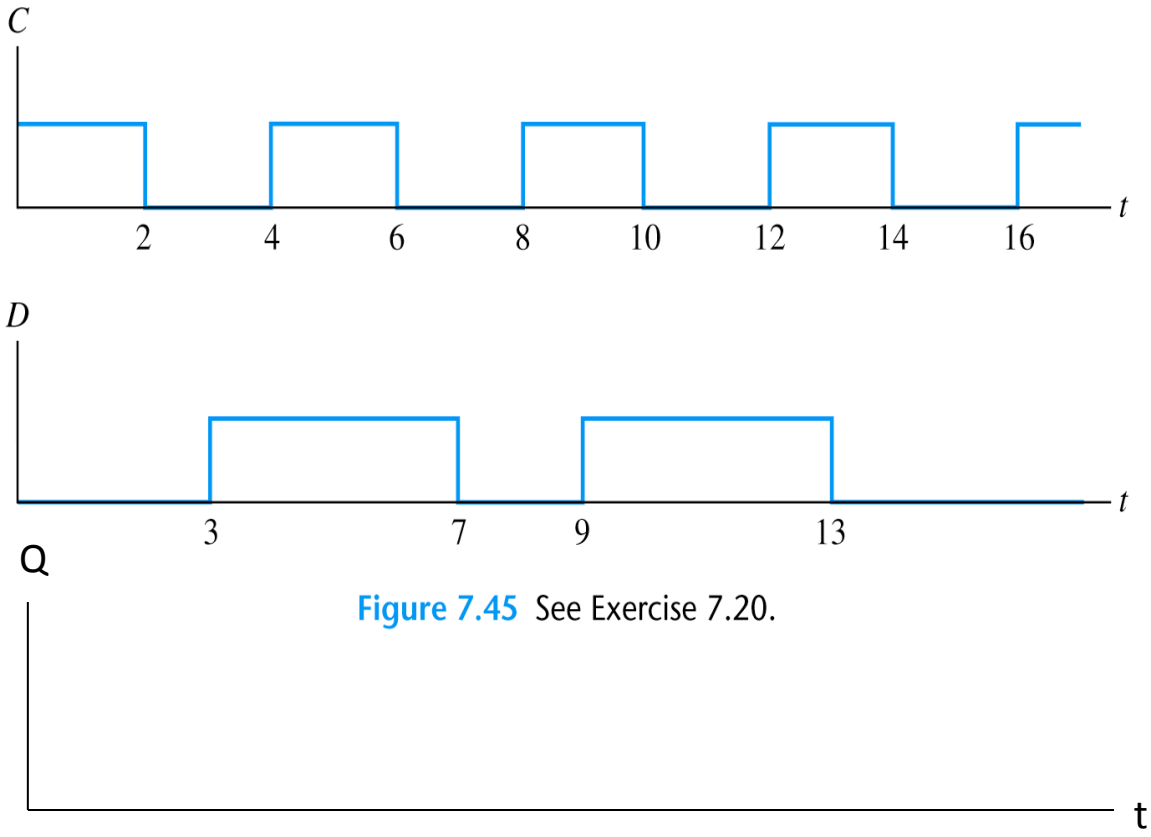


Figure 7.45 See Exercise 7.20.

Exercise

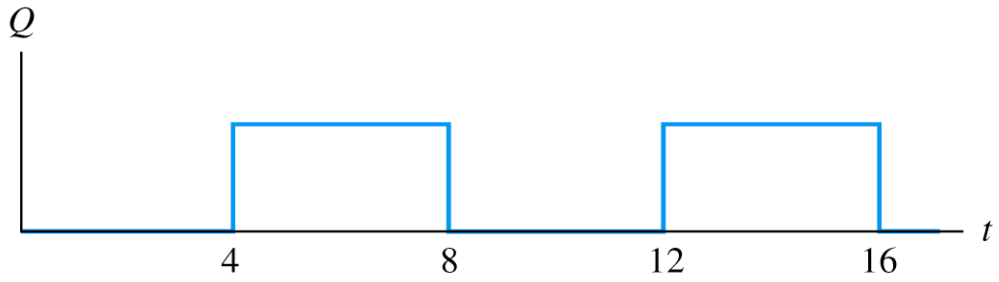
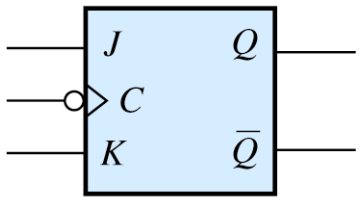


Figure 7.46 Answer for Exercise 7.20.

Negative Edge Triggered JK Flip Flop



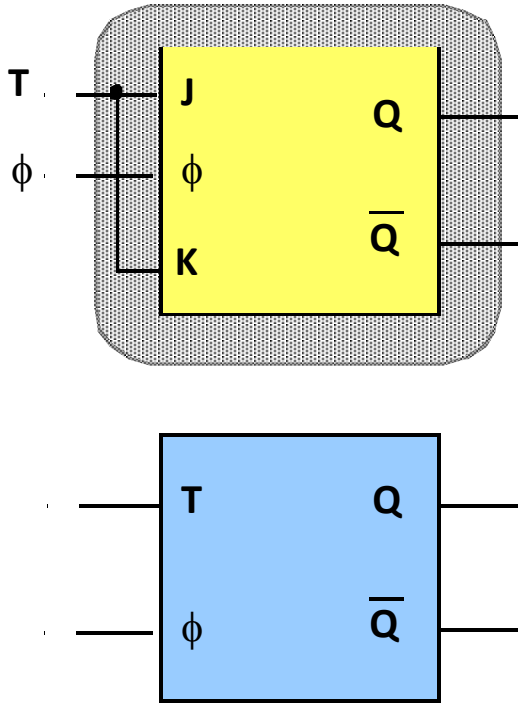
(a) Circuit symbol

C	J	K	Q_n	Comment
0	×	×	Q_{n-1}	Memory
1	×	×	Q_{n-1}	Memory
↓	0	0	Q_{n-1}	Memory
↓	0	1	0	Reset
↓	1	0	1	Set
↓	1	1	$\overline{Q}_{n-1}$	Toggle

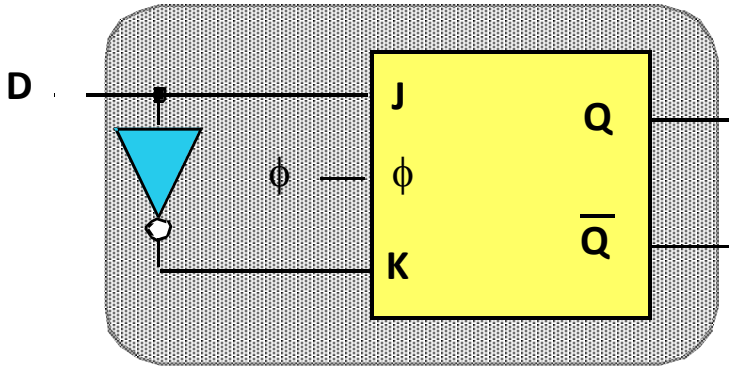
(b) Truth table
↓ indicates a transition
from low to high

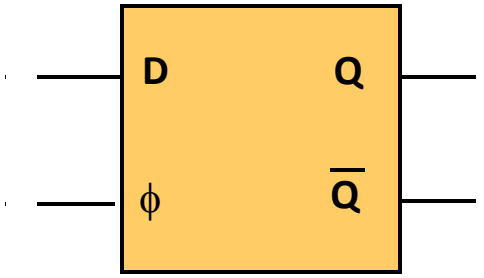
Figure 7.47 Negative-edge-triggered JK flip-flop.

Other Flip Flops



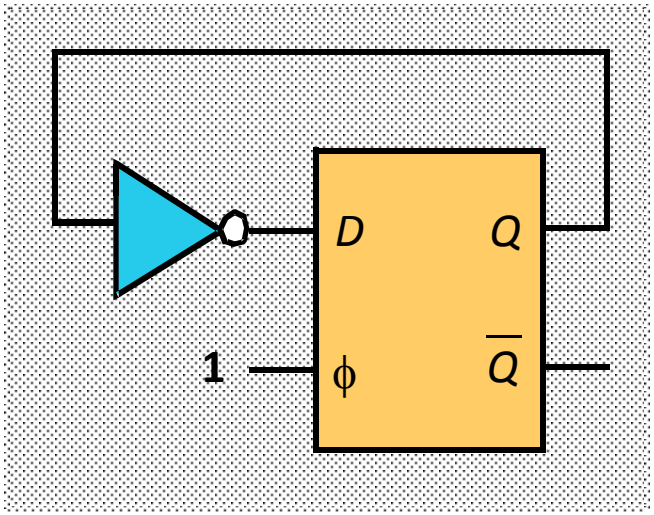
Toggle Flip-Flop

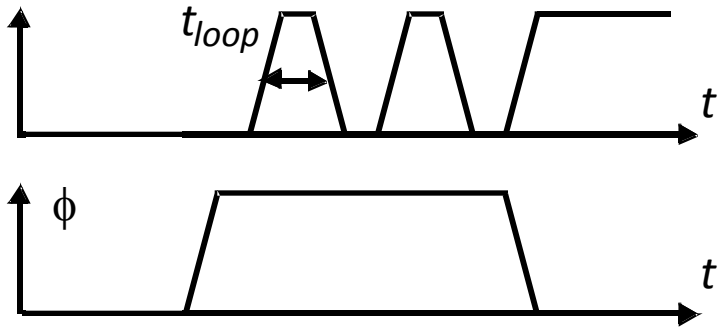




Delay Flip-Flop (D-latch)

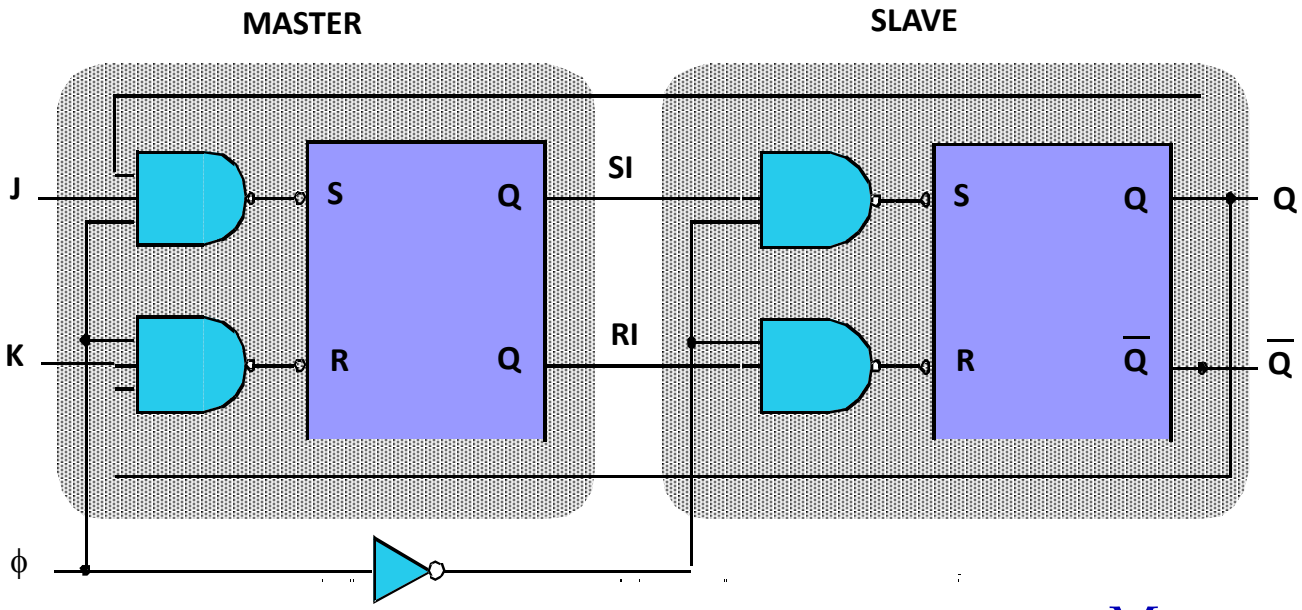
Race Problem

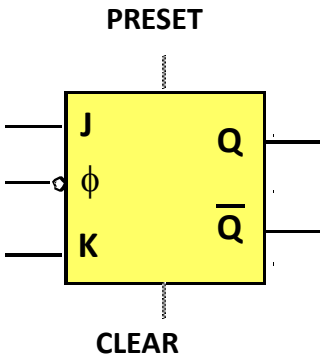




Signal can race around during ϕ = 1

Master-Slave Flip Flop Implementation





Master transmits the signal to the output during the high clock phase and slave is waiting for the clock to change this prevents race conditions

Shift Registers

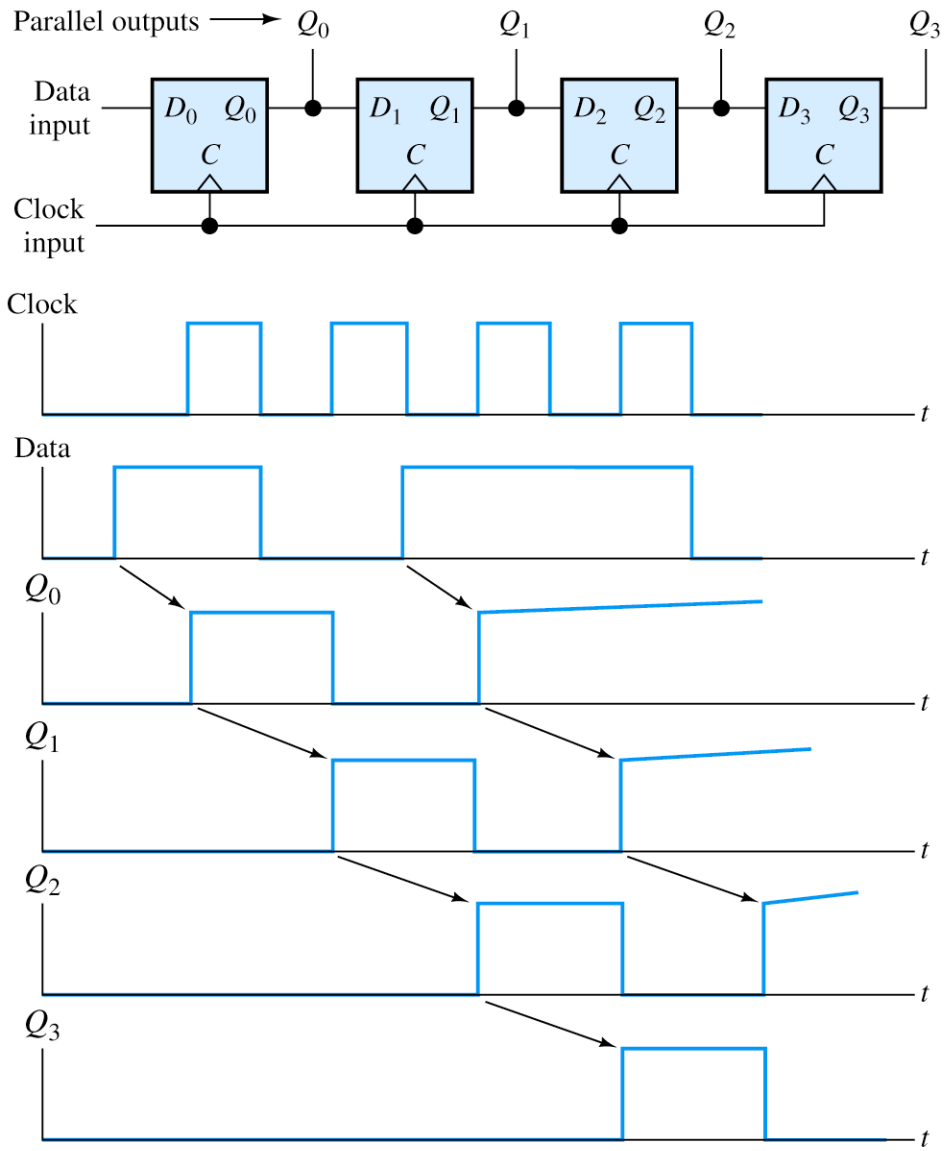


Figure 7.48 Serial-input parallel-output shift register.

Shift Registers

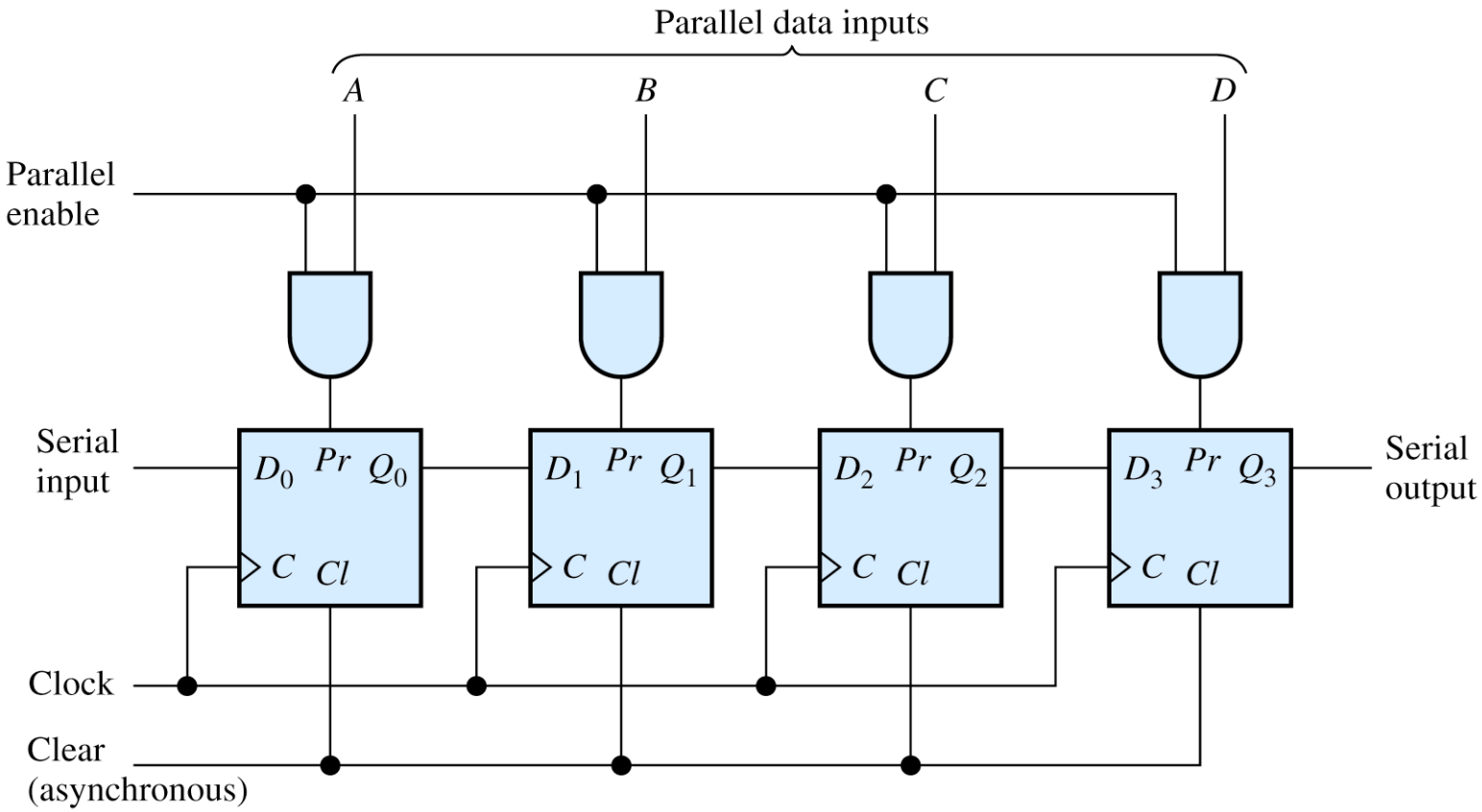


Figure 7.49 Parallel-input serial-output shift register.

Counter

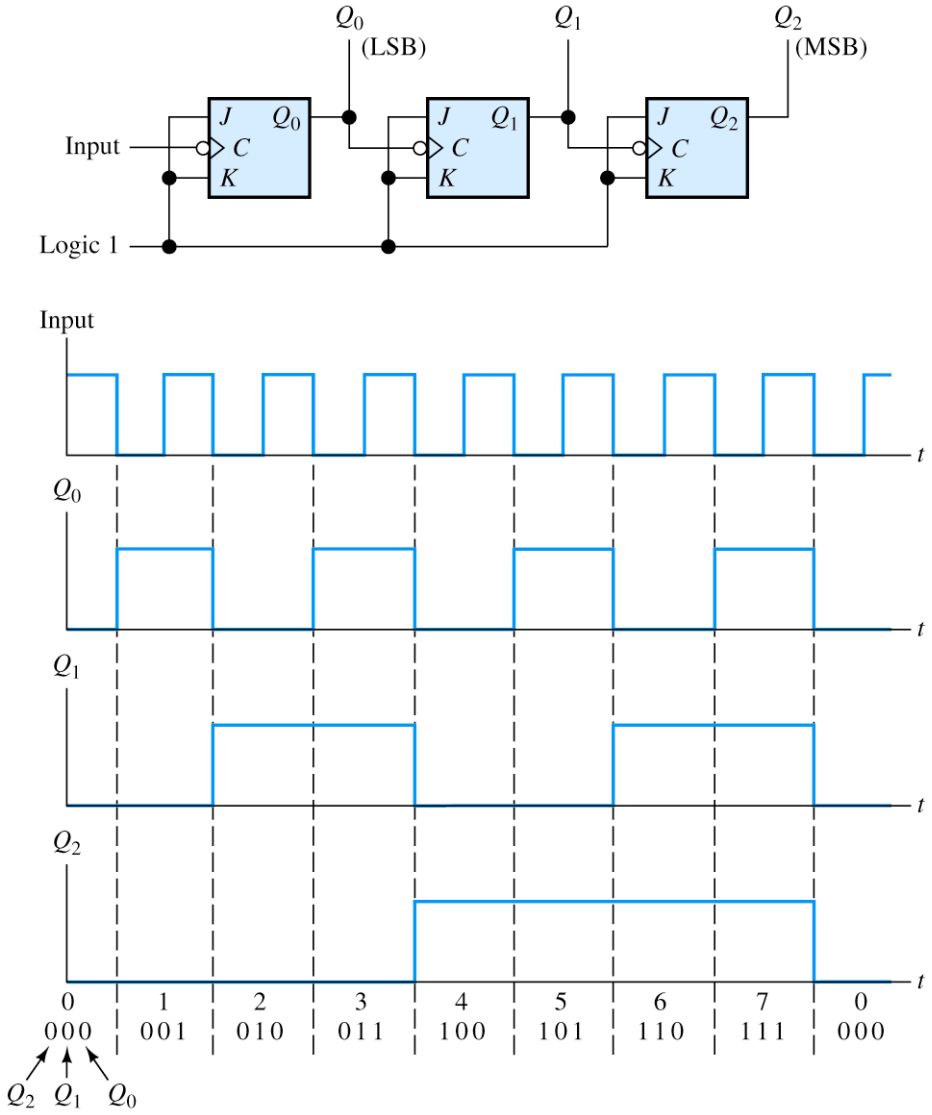


Figure 7.50 Ripple counter.