CAO: Lecture 27
8086 Microprocessor

Topics Covered

- Features of 8086 Microprocessor
- 8086 microprocessor
- 20 bits address bus?
- 8086 INTERNAL ARCHITECTURE
- BIU and EU
- Pin diagram

Features of 8086 Microprocessor

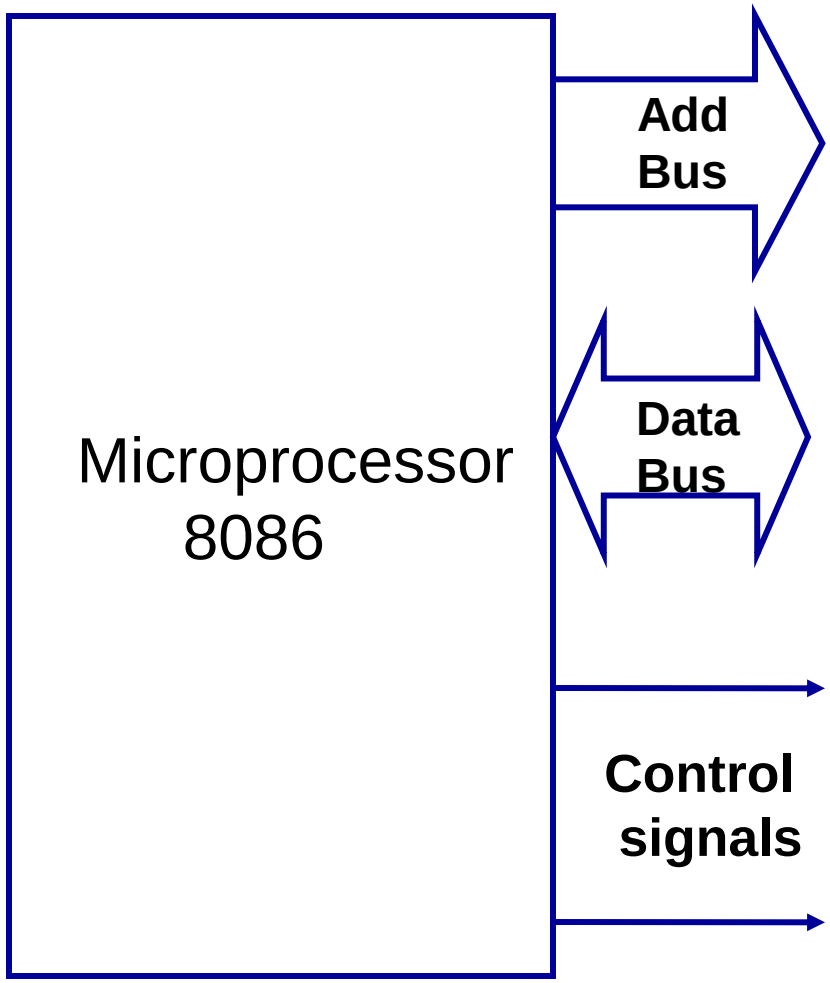
- - 8086 is a 16bit processor. It's ALU, internal registers works with 16bit binary word
- - 8086 has a 16bit data bus. It can read or write data to a memory/port either 16bits or 8 bit at a time
- - 8086 has a 20bit address bus which means, it can address upto 220 = 1MB memory location
- - Frequency range of 8086 is 6-10 MHz

8086 microprocessor

Address Bus – 20 lines – A_{19} – A_0

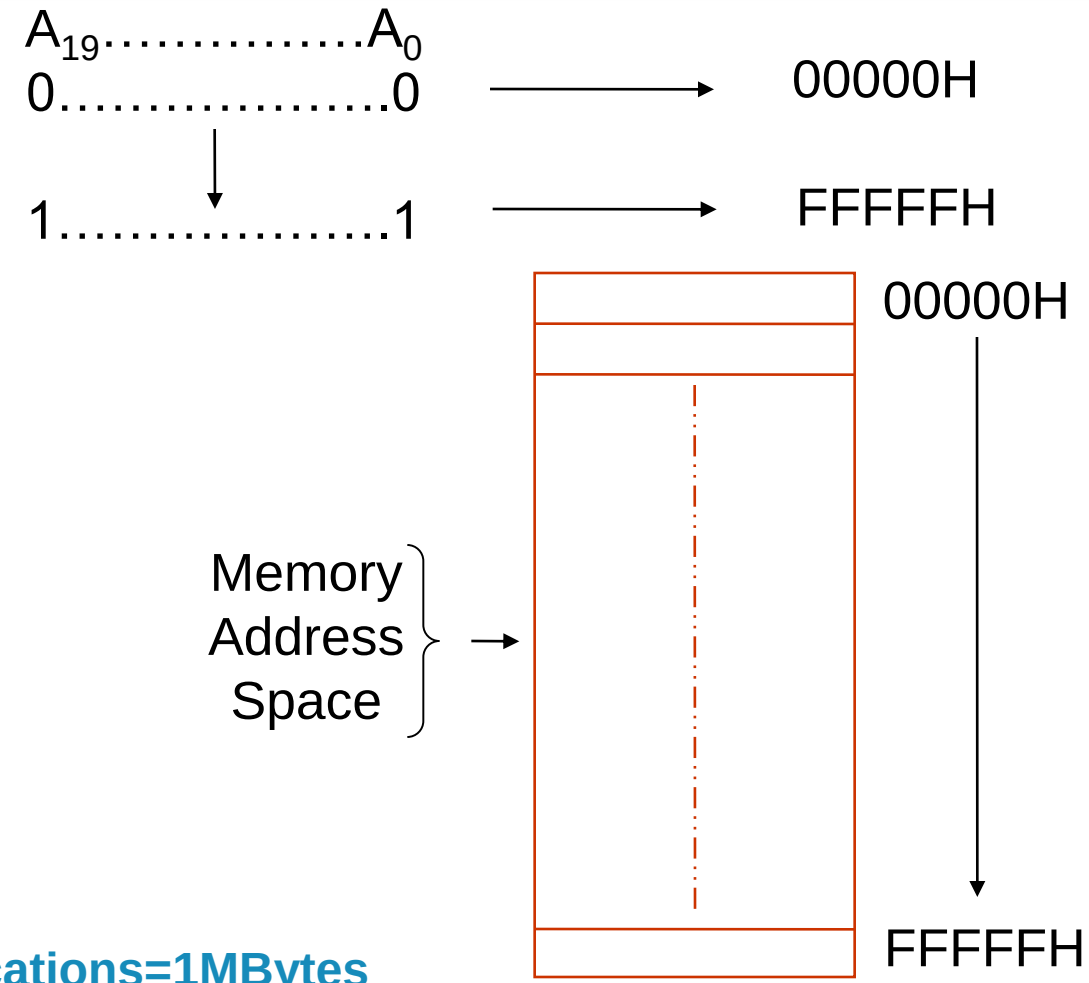
Data Bus – 16 lines – D_{15} – D_0

- 16 bit- microprocessor ?
- 16-bits data bus?



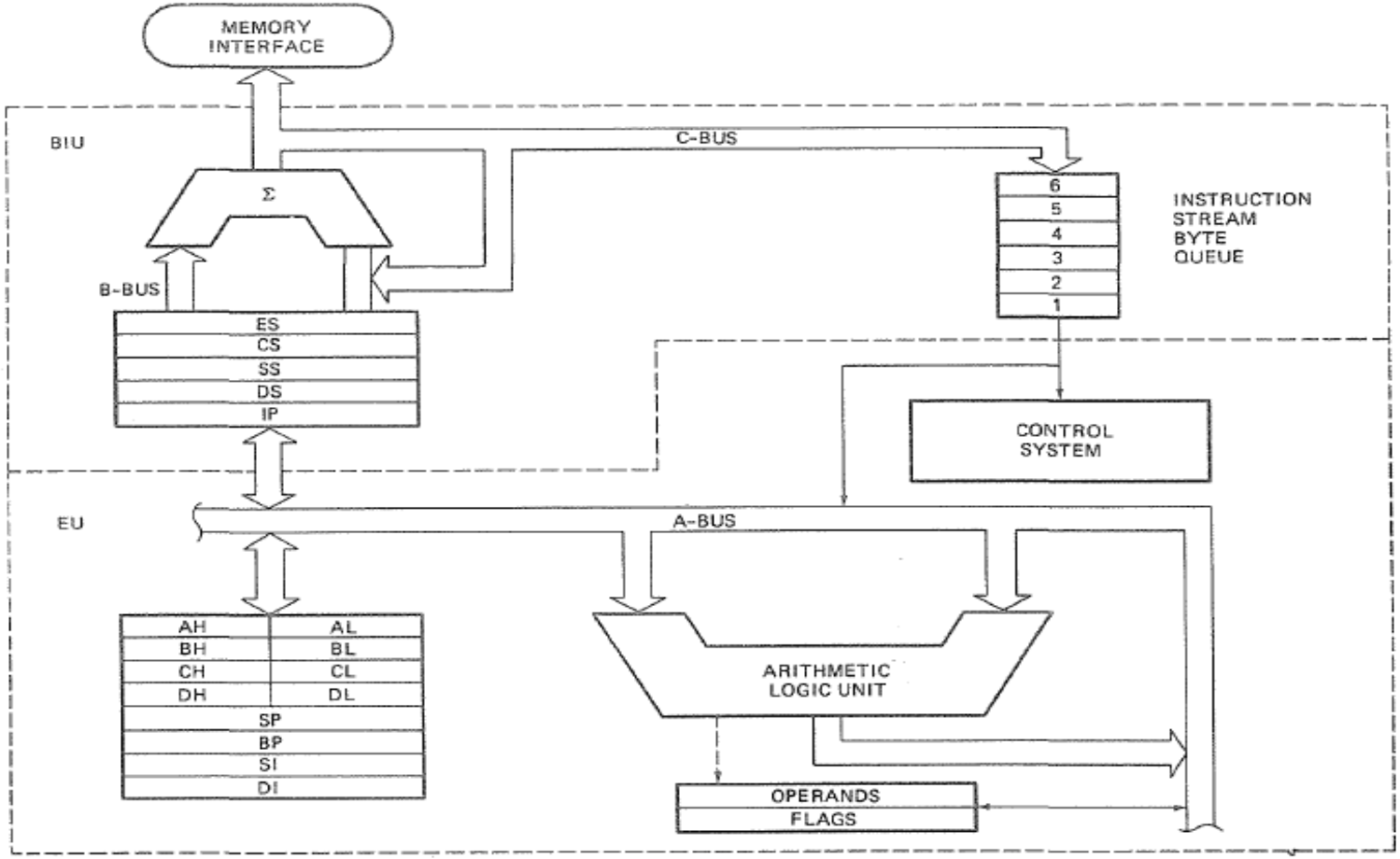
20 bits address bus?

- It can address any one of 1,048,576 (=2^{20}) memory locations/addresses.
- Each memory location is one byte wide.
- To store a word of 16 bit 2 memory locations are required.
- If the first byte of the word is at even address 8086 can read the entire word in one operation.
- If the first byte of the word is at an odd address, the 8086 will read the first byte with one bus operation and the second byte with another bus operation.



1,048,576 memory locations=1MBytes

8086 INTERNAL ARCHITECTURE



2 units are:

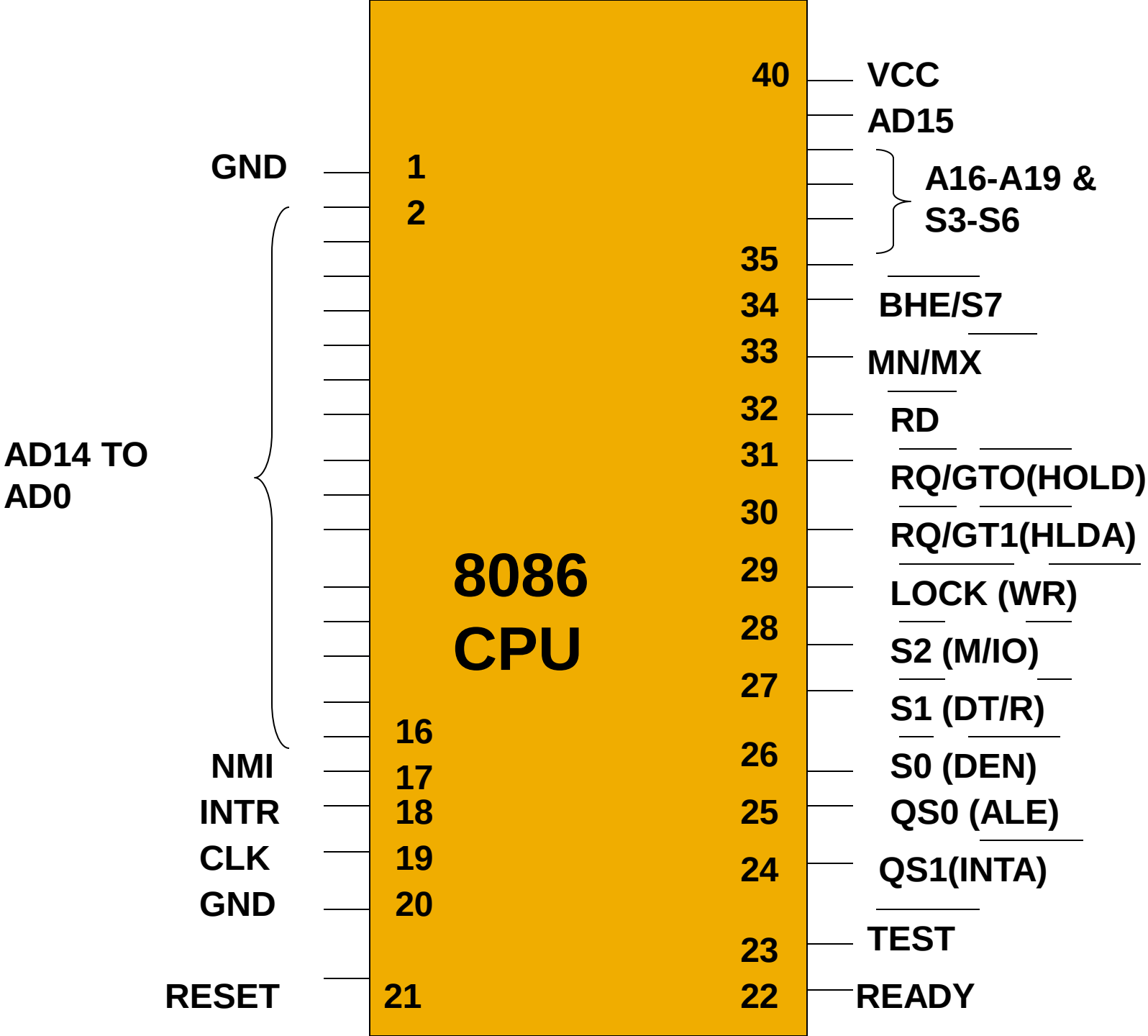
1. **BIU**
2. **EU**

Fig: 8086 Internal block diagram

BIU and EU

- **BIU (bus interface unit)** sends out addresses, fetches instructions from memory, reads data from ports and memory, and writes data to ports and memory. In other words, the BIU handles all transfers of data and addresses on the buses for the execution unit.
- **EU (execution unit)** of the 8086 tells the BIU where to fetch instructions or data from, decodes instructions, and executes instructions.

Pin diagram


8086
CPU
GND
1
2
AD14 TO
AD0
NMI
16
17
INTR
18
CLK
19
GND
20
RESET
21
40
VCC
AD15
A16-A19 &
S3-S6
35
34
BHE/S7
33
MN/MX
32
RD
31
RQ/GTO(HOLD)
30
RQ/GT1(HLDA)
29
LOCK (WR)
28
S2 (M/IO)
27
S1 (DT/R)
26
S0 (DEN)
25
QS0 (ALE)
24
QS1(INTA)
23
TEST
22
READY

Important 8086 Pin Diagram/Description

AD15±AD0

ADDRESS DATA BUS:
These lines constitute the time multiplexed memory/IO address and data bus.

ALE

Address Latch Enable. A HIGH on this line causes the lower order 16bit address bus to be latched that stores the addresses and then, the lower order 16bit of the address bus can be used as data bus.

READY

READY is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer.

INTR

INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.

INTA

Interrupt Acknowledge from the MP

NMI :NON-MASKABLE INTERRUPT: an edge triggered input which causes an interrupt request to the MP. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software.

RESET: causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution

MN/MX :MINIMUM/MAXIMUM: indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

1. **Minimum mode :**The 8086 processor works in a single processor environment.

All control signals for memory and I/O are generated by the microprocessor.

2. **Maximum mode :it** is designed to be used when a coprocessor exists in the system.8086 works in a multiprocessor environment. Control signals for memory and I/O are generated by an external BUS Controller

M/IO : Differentiate between the Memory and I/O operation. A LOW on this pin indicated I/O operation and a HIGH indicated a Memory Operation

HOLD : The 8086 has a pin called HOLD. This pin is used by external devices to gain control of the busses.

HLDA : When the HOLD signal is activated by an external device, the 8086 stops executing instructions and stops using the busses. This would allow external devices to control the information on the