CAO: Lecture 22
Amdahl's Law

Topics Covered

- Amdahl's law
- Basic Page Replacement
- Modes of transfer
- Programmed I/O
- Interrupt Initiated IO
- Types of Interrupt
- DMA (Direct Memory Access)

Basic Page Replacement

1. Find the location of the desired page on disk

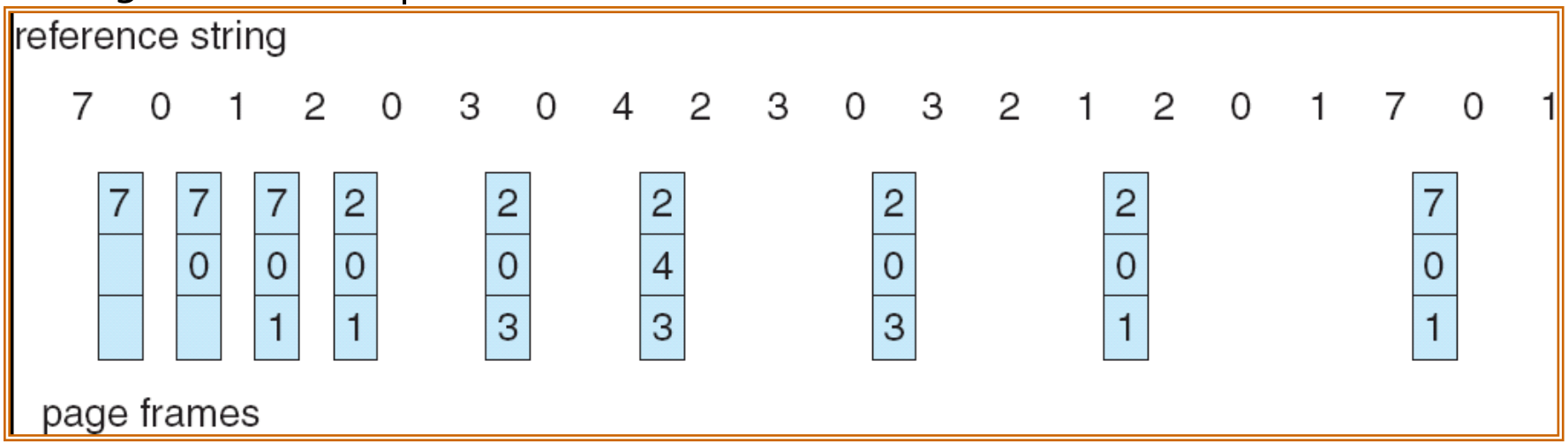
2. Find a free frame:
   - If there is a free frame, use it
   - If there is no free frame, use a page replacement algorithm to select a **victim** frame

3. Bring the desired page into the (newly) free frame; update the page and frame tables

4. Restart the process

Page Replacement : OPT (Optimal Policy)

- Replace page that will not be used for longest period of time. It requires future knowledge.
- 3 frames example



- Adv : Reduces Page Faults
- Disadv : It is difficult to implement as future knowledge of reference string is required.

CAO Model Question Paper
Unit – 2

Q:1 Discuss hardwired control design method.

Q:2 Explain the concept of Micro programmed Sequencer.

Q:3 Explain five stages instruction cycle with the help of flowchart.

Q:4 What is Content Addressable Memory? Explain the match logic in CAM.

Q:5 What do you mean by "Next Address Generator" present in a Microprogrammed Control Unit? Explain briefly along with its block diagram.

Q:6 Explain 2D RAM organization with suitable diagram. (J. P. Hayes-Sec-6.1.2,fig 6.8, fig 6.13)

CAO Model Question Paper
Unit – 3

Q: 1 Discuss the principle of Locality of Reference associated with the Memory Hierarchy.

Q: 2 What are the reasons for using Virtual memory? Distinguish between Paging and Segmentation.

Q: 3 What are LRU and OPT Policies of page replacement? Compare them.

Q: 4 Explain working of a cache memory. What are the relative advantages and disadvantages of direct and Associative mapping of cache memory?

Modes of transfer

- Data transfer between the central computer and the I/O devices may be handled in a variety of modes.

- The modes of transfer are:

1. Programmed I/O.
2. Interrupt-initiated I/O
3. Direct memory access (DMA)

Programmed I/O

- Programmed I/O operations are the result of I/O instructions written in the computer program.
- Each data item transfer is initiated by an instruction in the program.
- Usually, the transfer is to and from CPU register and peripheral.
- Other instructions are needed to transfer the data to and from CPU and memory.
- Transferring data under program control requires constant monitoring of the peripheral by the CPU.
- Once a data transfer is initiated, the CPU is required to monitor the interface to see when a transfer can again be made.
- It is up to the programmed instructions executed in the CPU to keep close tabs on everything that is taking place in the interface unit and the I/O device.
- In this method, the CPU stays in a program loop until the I/O unit indicates that it is ready for data transfer.
- This is a time-consuming process since it keeps the processor busy needlessly.

Interrupt Initiated IO

- In the programmed I/O method, the CPU stays in a program loop until the I/O unit indicates that it is ready for data transfer.
- This is a time-consuming process since it keeps the processor busy needlessly.
- It can be avoided by using interrupt facility and special commands to inform the interface to issue an interrupt request signal when the data are available from the device.
- In the mean-time the CPU can proceed to execute another program.
- The interface meanwhile keeps monitoring the device.
- When the interface determines that the device is ready for the data transfer, it generates an interrupt request to the computer.
- Upon detecting the external interrupt signal, the CPU momentarily stops the task it is processing, branches to a service program to process the I/O transfer, and then returns to the task it was originally performing.

Types of Interrupt

1. External interrupts
2. Internal interrupts
3. Software interrupts

- External interrupts come from I/O devices, from a timing device, from a circuit monitoring the power supply, or from any other external source. For example: Timeout interrupt

- Internal interrupts arise from illegal or erroneous use of an instruction or data. Internal interrupts are also called ***traps***. For example, attempt to divide by zero.

The difference between internal interrupt and external interrupt

- The internal interrupt is initiated by some exceptional condition caused by program itself rather than by an external event.
- External interrupts depend on external conditions that are independent of the program.

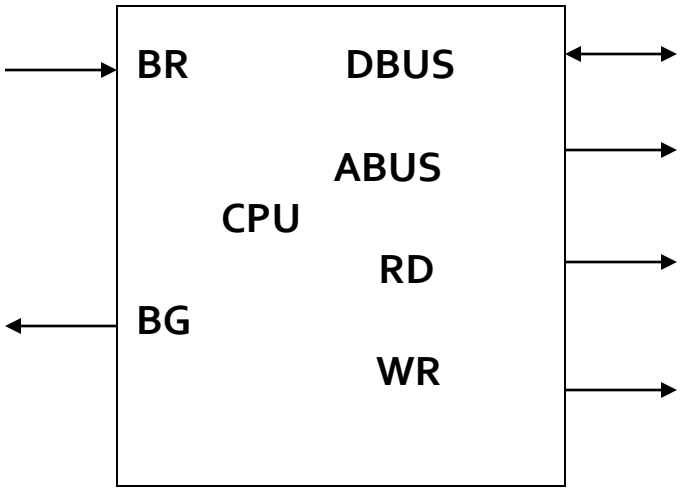
- **Software Interrupt:** A software interrupt is initiated by executing an instruction. Software interrupt is a special call instruction that behaves like an interrupt rather than a subroutine call. The most common use of a software interrupt is associated with a supervisor call instruction. This instruction provides means for switching from a CPU user mode to the supervisor mode.

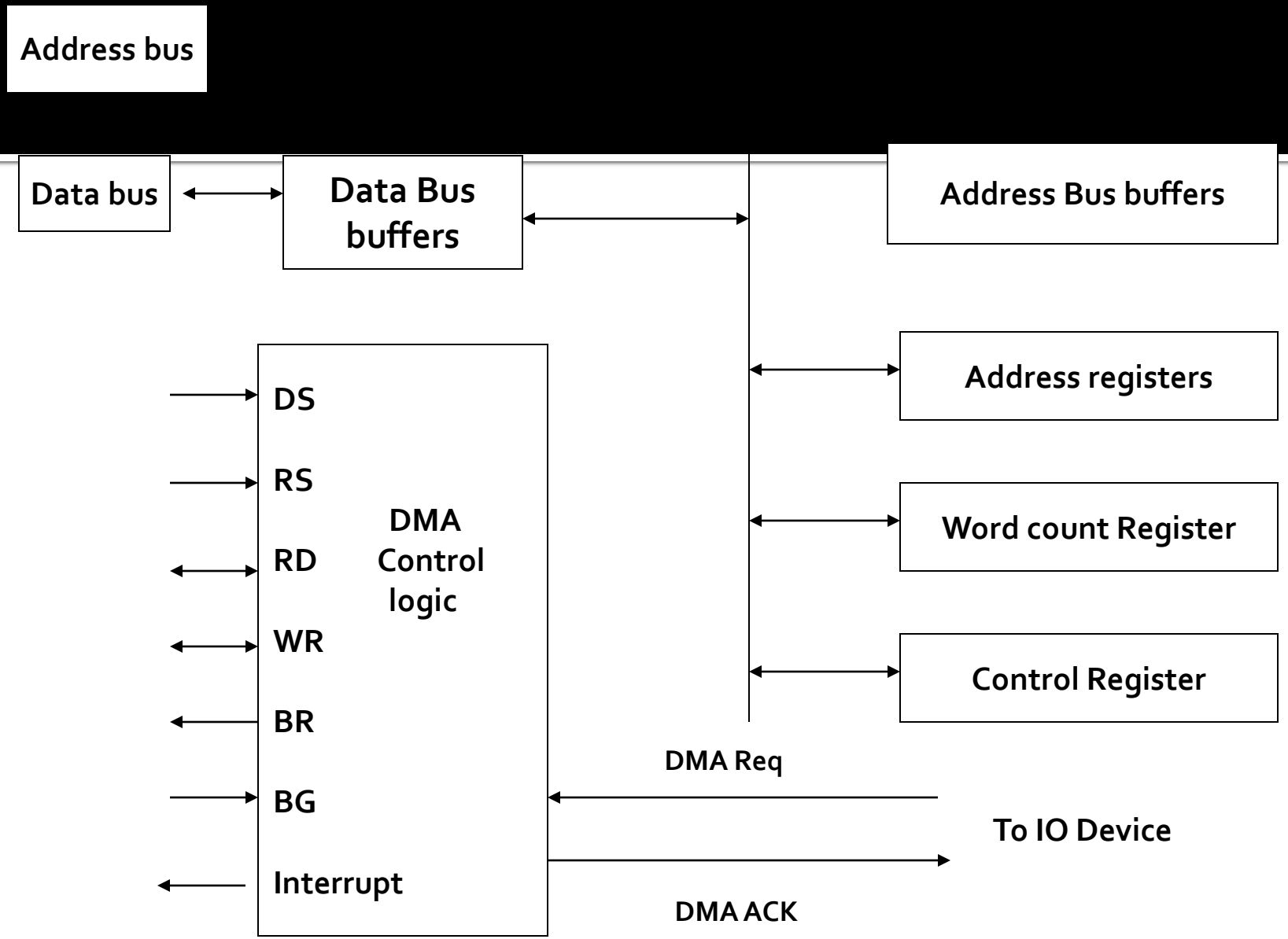
DMA (Direct Memory Access)

- Direct memory access is an I/O technique used for high speed data transfer.
- In DMA, the interface transfers data into and out of the memory unit through the memory bus.
- In DMA, the CPU releases the control of the buses to a device called a DMA controller.
- Removing the CPU from the path and letting the peripheral device manage the memory buses directly would improve the speed of transfer.
- The CPU initiates the transfer by supplying the interface with the starting address and the number of words needed to be transferred and then proceeds to execute other tasks.
- When the transfer is made, the DMA requests memory cycles through the memory bus.
- When the request is granted by the memory controller, the DMA transfers the data directly into memory.
- The CPU merely delays its memory access operation to allow the direct memory I/O transfer.

- Many computers combine the interface logic with the requirements for direct memory access into one unit and call it an I/O processor (IOP).
- A DMA controller takes over the memory buses to manage the transfer directly between the I/O device and memory using 2 special control signals BR And BG.
- The **BR (bus request)** output signal is used by the DMA controller to the CPU to take control of memory buses.
- The CPU then activates the **BG (BUS GRANT)** signal to inform the external DMA that the buses are in high-impedance state.
- Then DMA takes the control of memory buses.
- **DMA CONTROLLER:** It needs the usual circuit of an interface to communicate with the CPU and I/O device.

CPU bus signals for DMA Transfer




Address bus
Data bus
Data Bus buffers
Address Bus buffers
Address registers
Word count Register
Control Register
DS
RS
RD
WR
BR
BG
Interrupt
DMA Control logic
DMA Req
To IO Device
DMA ACK

CAO Model Question Paper
Unit – 4

Q:1 State Amdahl's law. Discuss its significance.

Q:2 Explain 3 major types of instructions.

Q:3 Explain the concept of Memory Hierarchy.

Q:4 Write a note on Computer Registers

Q:5 Short Note on:

1. DMA
2. Priority Interrupt
3. Superscalar Processing