CAO: Lecture 7 Sequential logic blocks (Latches, Flip-Flops, Registers, Counters): Shift registers

Topics Covered

- Overview
- Register with Parallel Load
- Register with Load Control
- Shift Registers
- Parallel Data Transfer

Overview

- Multiple flip flops can be combined to form a data register
- Shift registers allow data to be transported one bit at a time
- Registers also allow for parallel transfer
  - Many bits transferred at the same time
- Shift registers can be used with adders to build arithmetic units
- Remember: most digital hardware can be built from combinational logic (and, or, invert) and flip flops
  - Basic components of most computers

Register with Parallel Load

- Register: Group of Flip-Flops
- Ex: D Flip-Flops
- Holds a Word (Nibble) of Data
- Loads in Parallel on Clock Transition
- Asynchronous Clear (Reset)

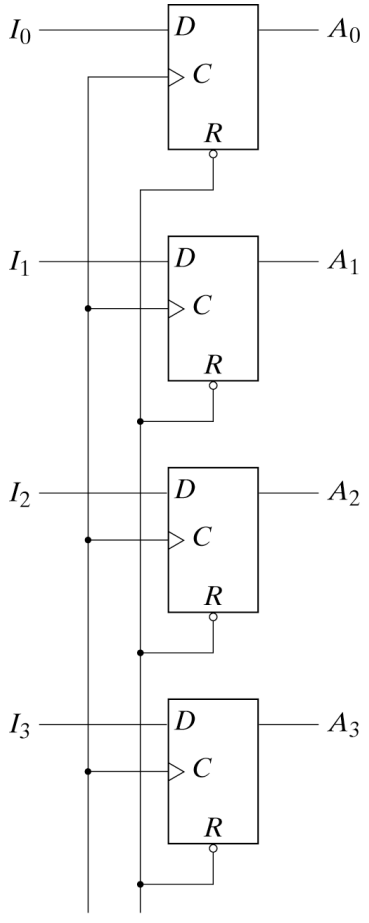

Fig. 6-1 4-Bit Register

Register with Load Control

- Load Control = 1
  - New data loaded on next positive clock edge
- Load Control = 0
  - Old data reloaded on next positive clock edge

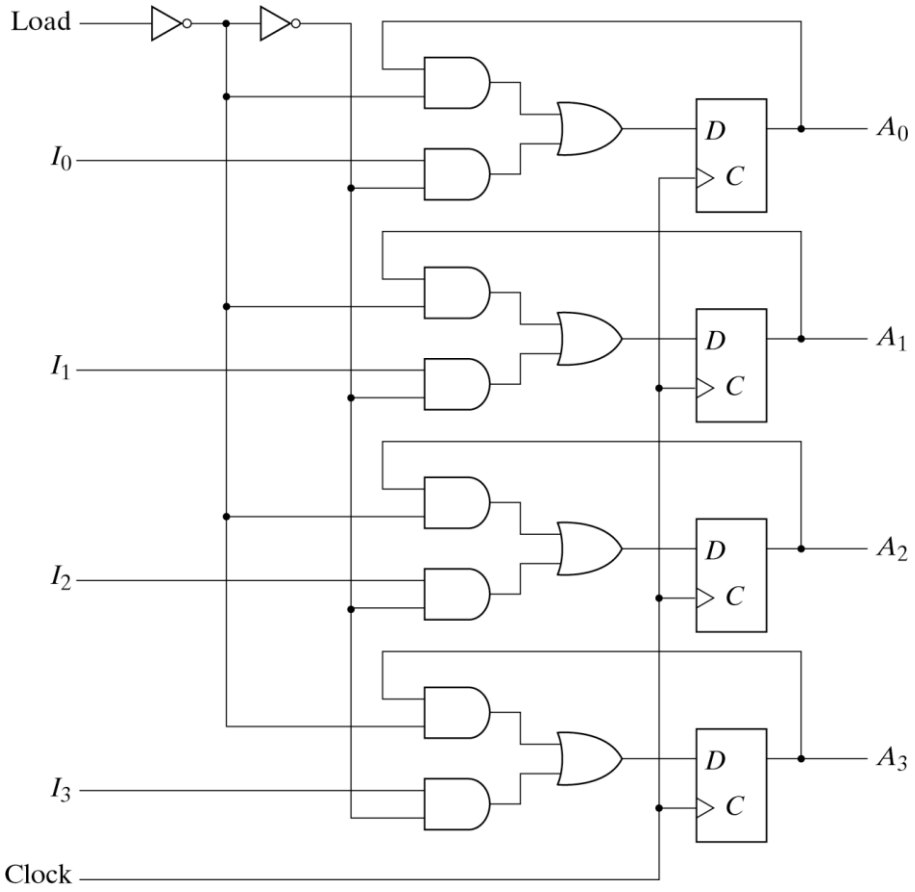

Fig. 6-2 4-Bit Register with Parallel Load

Shift Registers

- Cascade chain of Flip-Flops
- Bits travel on Clock edges
- Serial in – Serial out, can also have parallel load / read

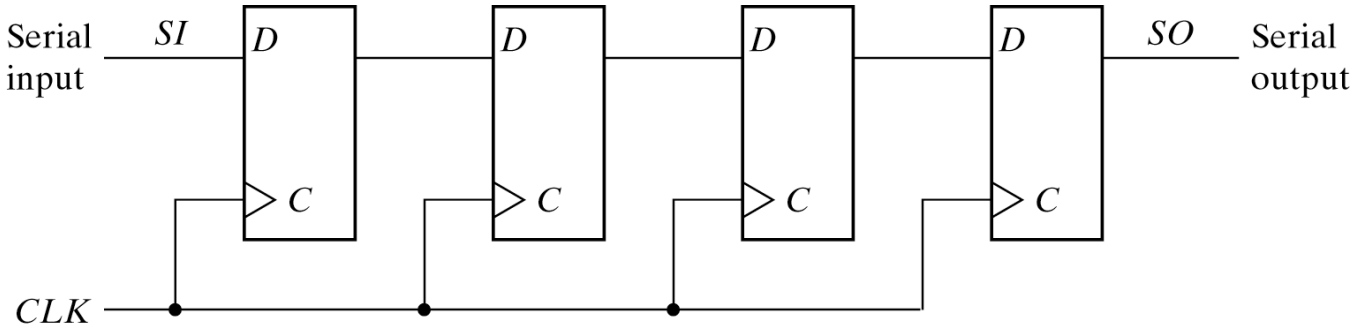

Fig. 6-3 4-Bit Shift Register

Parallel Data Transfer

All data transfers on rising clock edge
Data clocked into register Y