CAO: Lecture 12
Performance metrics; MIPS, MFLOPS

Topics Covered

- What is a performance metric?
- Performance Measures
- MFLOPS

What is a performance metric?

- Count
  - Of how many times an event occurs
- Duration
  - Of a time interval
- Size
  - Of some parameter
- A value derived from these fundamental measurements

Performance Measures

CPU Speed is measured as the Number of basic operations it can perform per unit time.

Ex. Typical basic operation of fixed point addition of the content of two registers R1 and R2 is:

R1:=R1+R2

Such operations are timed by a regular stream of signals(ticks or beats) issued by System clock.

Speed of Clock = Frequency (f) measured in Millions of ticks per second (MHz).

Clock Cycle or clock period (T_{clock}) = time required to execute the operation =I/f microseconds.

Ex. If Clock speed is 250 MHz can perform one basic operation in the clock period (T_{clock}) = 1/250=.004 μs.

NOTE: Operations such as division or floating point numbers requires more than one clock cycle to complete the execution.

CPU’s processing of an instruction involves several steps each of which requires at least one clock cycle:

1. Fetch the instruction from main memory M.
2. Decode the instruction's opcode.
3. Load from M any operands needed unless they are already in CPU registers.
4. Execute the instruction via register to register operation.
5. Store the result in M.

T=N/IPS

T= total program execution time

N= Actual no. of instruction executed.

IPS= Average number of instruction executed per second

CPI= (f * 10^6)/IPS

CPI= Average no of cycles per instruction.

f = CPU's clock frequency(MHz).

Hence T=N*CPI/ (f * 10^6)

MIPS(Millions of instruction executed per second)=IPS* 10^6 or

= f/CPI.

Equation T=N*CPI/ (f * 10^6) shows that the three separate factors Software, Architecture, and Hardware jointly determines the performance of CPU .

Software: Efficiency with which the programs are written and compiled Into object code influences N, the no. of instruction executed. Reducing N reduces the overall execution time T.

Architecture: The Efficiency with which individual instructions are Processed directly affects CPI. Reducing CPI reduces T.

Hardware: Speed of processor determines f , the clock frequency. Increasing f reduces T.

Note:*CISC processor's aim is to reduce N at the expence of CPI whereas RISC processors aim to reduce CPI at expence of N.*

MFLOPS

- Better definition of "distance traveled"
- 1 unit of computation (~distance) ≡ 1 floating-point operation
- *Millions of floating-point ops per second*
- MFLOPS = f / (T_e * 1000000)
  - f = number of floating-point instructions
  - T_e = execution time