LECTURE 13

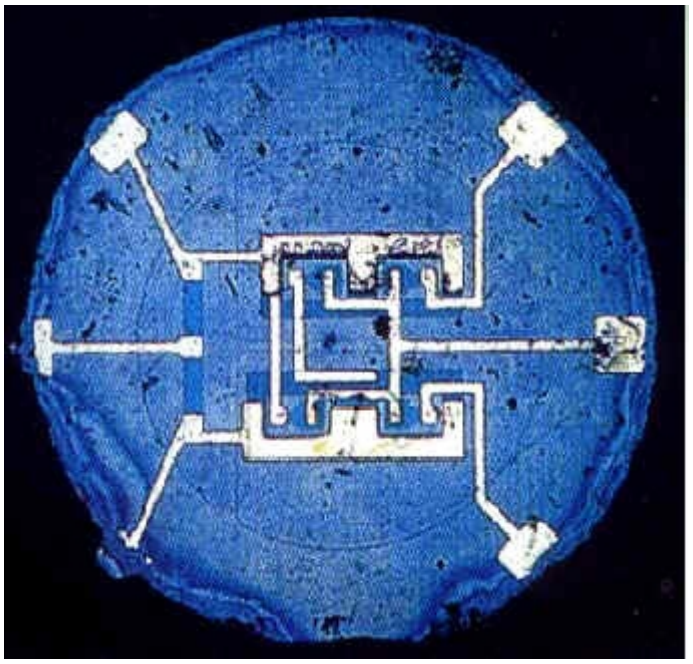
-Introduction to Planar Technology

Topics to be covered

- Planar Technology
- Fabrication Methods

Planar technology invented

- Kilby's invention had a serious drawback, the individual circuit elements were connected together with gold wires making the circuit difficult to scale up to any complexity.
- By late 1958 Jean Hoerni at Fairchild had developed a structure with N and P junctions formed in silicon. Over the junctions a thin layer of silicon dioxide was used as an insulator and holes were etched open in the silicon dioxide to connect to the junctions.
- In 1959, Robert Noyce also of Fairchild had the idea to evaporate a thin metal layer over the circuits created by Hoerni's process.
- The metal layer connected down to the junctions through the holes in the silicon dioxide and was then etched into a pattern to interconnect the circuit. Planar technology set the stage for complex integrated circuits and is the process used today.

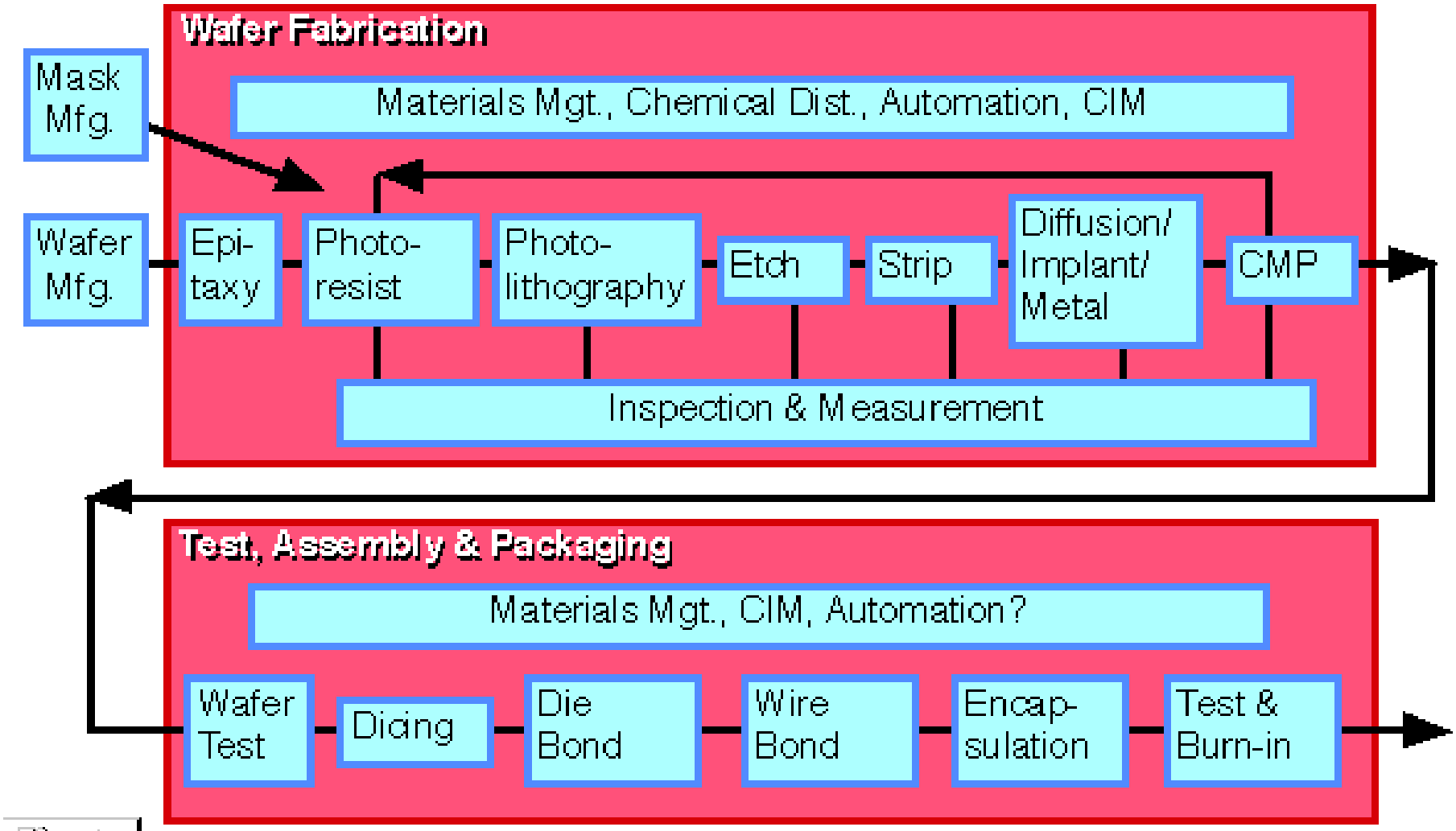


Planar technology

IC Fabrication Technology: History (cont.)

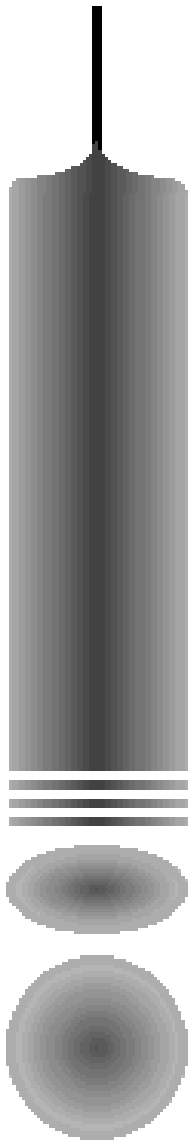
- **1960 - Epitaxial deposition developed**
- Bell Labs developed the technique of Epitaxial Deposition whereby a single crystal layer of material is deposited on a crystalline substrate. Epitaxial deposition is widely used in bipolar and sub-micron CMOS fabrication.
- **1960 - First MOSFET fabricated**
- Kahng at Bell Labs fabricates the first MOSFET.
- **1961 - First commercial ICs**
- Fairchild and Texas Instruments both introduce commercial ICs.
- **1962 - Transistor-Transistor Logic invented**
- *1962 - Semiconductor industry surpasses $1-billion in sales*
- **1963 - First MOS IC**
- RCA produces the first PMOS IC.

The Chip-Making Process



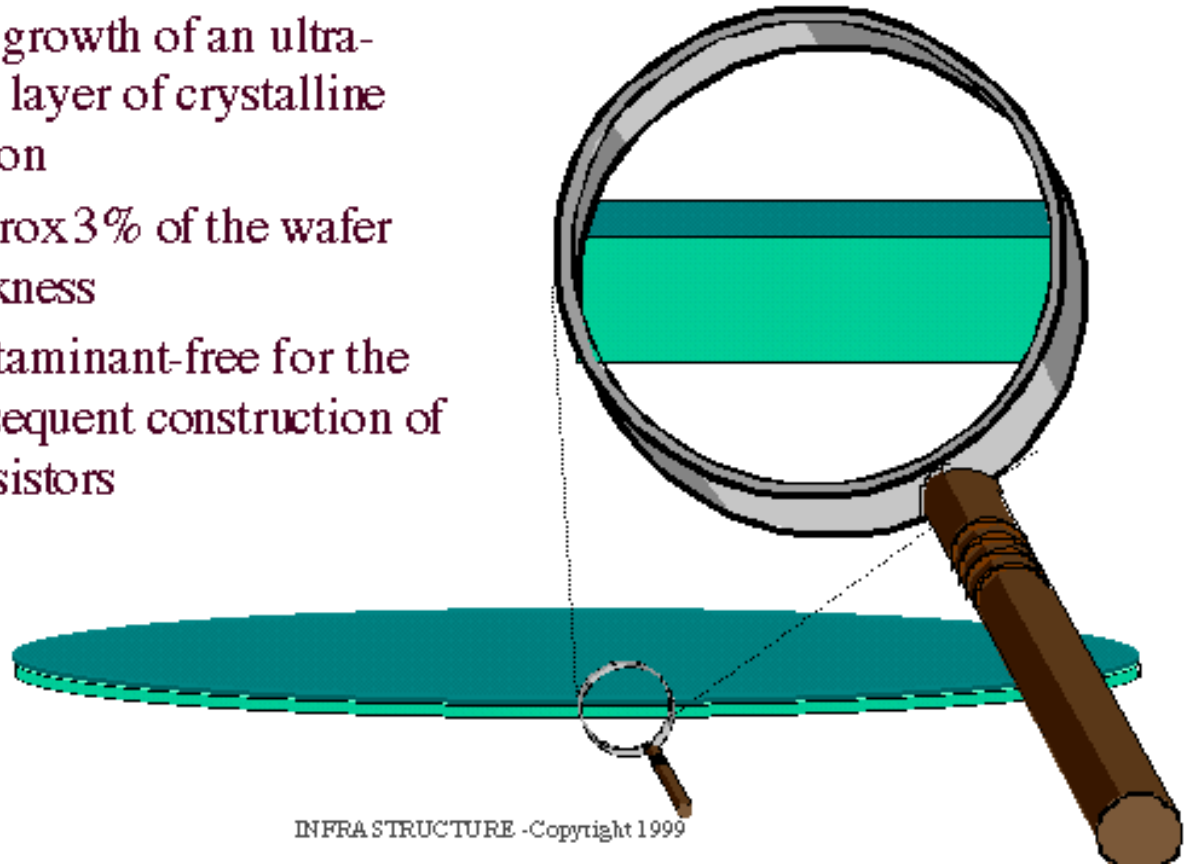
Making the Wafer

- The Process:
  - A seed crystal is suspended in a molten bath of silicon
  - It is slowly pulled up and grows into an ingot of silicon
  - The ingot is removed and ground down to diameter
  - The end is cut off, then thin silicon wafers are sawn off (sliced) and polished



Epitaxy

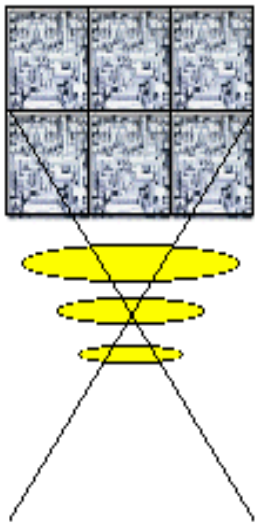
- The growth of an ultra-pure layer of crystalline silicon
- Approx 3% of the wafer thickness
- Contaminant-free for the subsequent construction of transistors

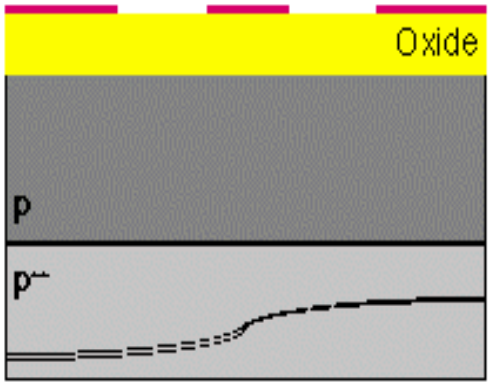


Crystalline or contaminate defects will kill the operation of an IC, so it is imperative that the silicon is ultra-pure. In order to create the best possible quality of silicon, a pure layer of silicon is grown on the raw wafer via an epitaxial growth process. This is known as the epi-layer.
This layer is very thin - approximately 3 percent or less of the wafer thickness. As device complexity grows, the need for epi-wafers increases.

Oxidation & Exposure

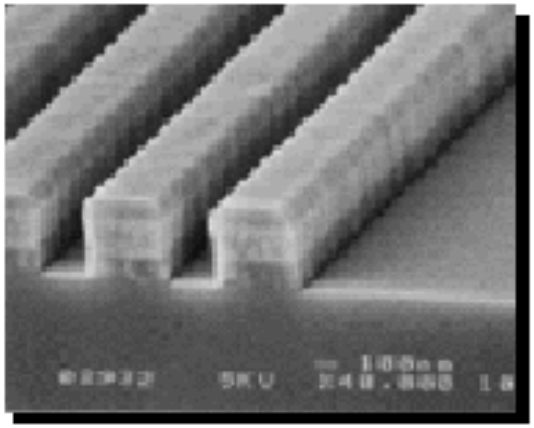
- The epi-wafer is exposed to high temperature to grow an oxide layer
- A layer of photoresist is spun onto the oxide
- The stepper exposes the pattern onto the photoresist
- The photoresist is then developed to leave the pattern on the wafer

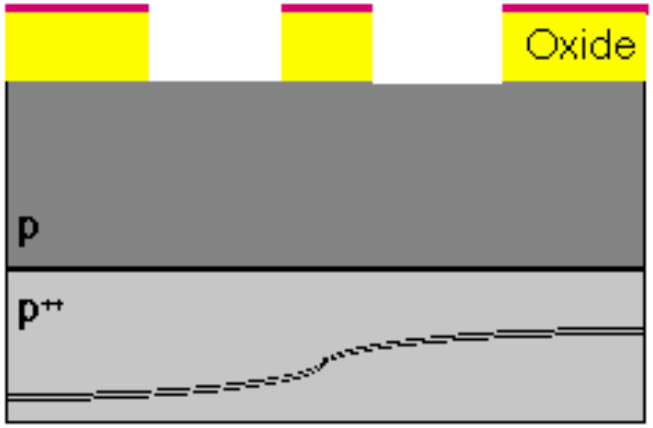




Etch & Strip

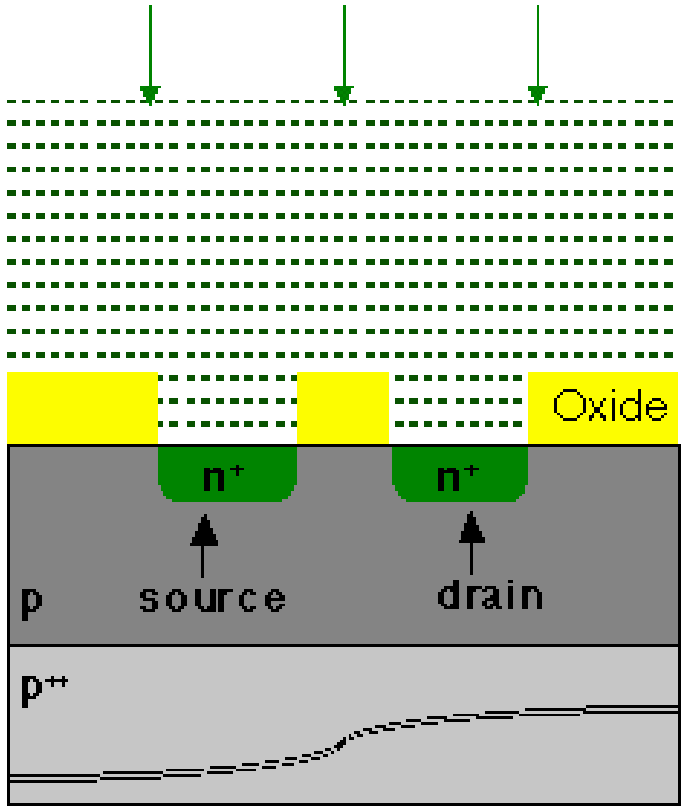
- An etch process (wet or dry) is used to remove the oxide where the photoresist pattern is absent
- The photoresist is then stripped completely off the wafer, leaving the oxide pattern on the wafer





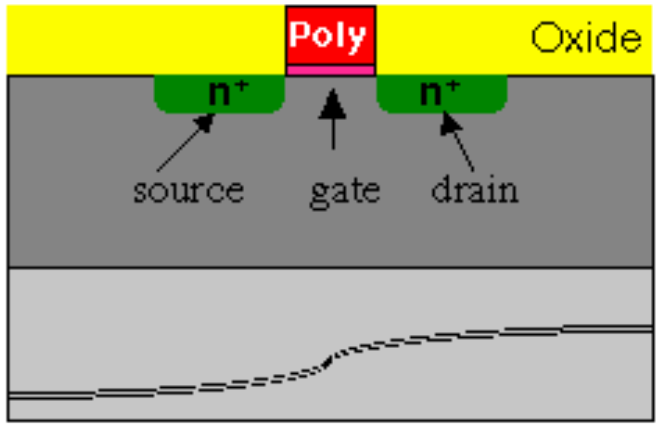
Diffusion & Implant

- The oxide acts as a barrier when dopant chemicals are deposited on the surface and diffused into the surface
- Alternatively, dopants may be bombarded into the silicon surface via an ion implant beam
- The induced ions create regions with different properties of the silicon semiconductor material
- These regions become the source and drain of the CMOS transistor



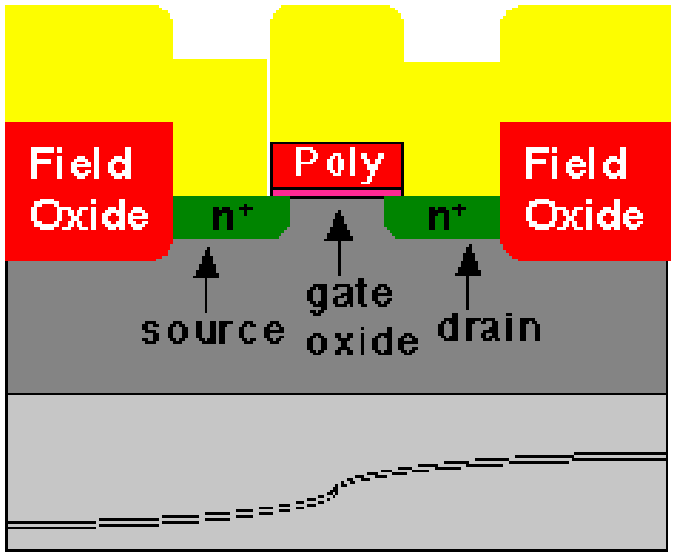
Deposition

- Using the same oxidation & photolithography process, an opening is made in the oxide to build the transistor's gate region
- A thin gate oxide or silicon nitride is deposited via CVD or Chemical Vapor Deposition process to act as an insulator between the gate and the silicon
- This is followed by Physical Vapor Deposition (PVD) or "sputtering" of a conductive polysilicon layer to form the transistor's gate region



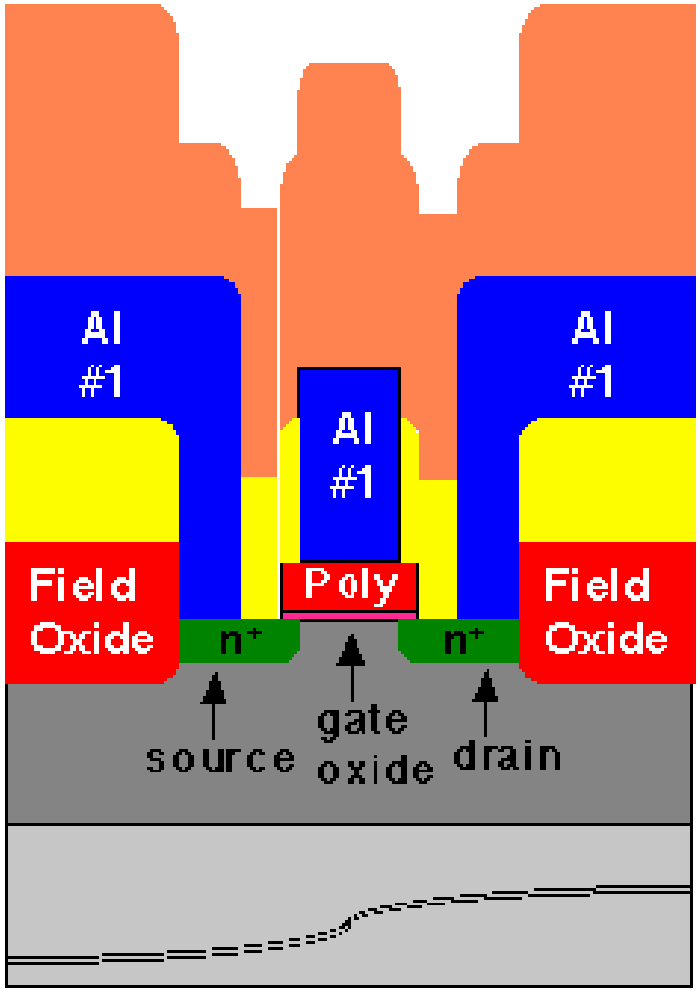
Oxidation

- Various oxides are grown or deposited to insulate or protect the formed transistors
- Deep Field Oxides are grown to isolate each transistor from its adjacent partners
- Dielectric isolation oxides are deposited to insulate the transistors from the interconnecting layers which will be built above
- Passivation oxides are later deposited on top of completed wafers to protect the surface from damage



Interconnect - Metallization

- A layer of aluminum is deposited on the surface and down into the via holes
- Excess aluminum is etched away after another photolithography process, leaving the desired interconnect pattern
- Another layer of dielectric isolation oxide is deposited to insulate the first layer of aluminum from the next one
- Note how the surface contours are developing with each process steps



Chemical Mechanical Planarization

- CMP (Chemical Mechanical Planarization) is an abrasive process using chemical slurries and a circular (sanding) action to polish the surface of the wafer smooth
- The smooth surface is necessary to maintain photolithographic depth of focus for subsequent steps and also to ensure that aluminum interconnects are not deformed over contour steps