Lecture Plan 1

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: A

S. No.	**Topic :-** Boolean Algebra	**Time Allotted:-**
1.	Introduction Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.	05 min
2	Division of the Topic ▪ Boolean Algebra ▪ Axioms ▪ Terminology ▪ N-bit boolean algebra ▪ Named theorems	30
3.	Conclusion Study and concepts of Boolean algebra were explained.	10

Assignment to be given: - What are the axioms?

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 2

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: A

S. No.	**Topic :-** Logic Gates	**Time Allotted:-**
1.	Introduction Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.	05 min
2	Division of the Topic ▪ NOT gate ▪ AND gate ▪ OR gate ▪ XOR gate ▪ What are digital circuits? ▪ NOR gate	30
3.	Conclusion Through understanding of all logic gates ,all axioms of Boolean algebra was given And k maps were discussed in details.	10

Assignment to be given: - How to make XOR gate from NAND?

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 3

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: A

S. No.	**Topic :-** Logic Gates	**Time Allotted:-**
1.	Introduction Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.	05 min
2	Division of the Topic Solving circuit expressions, examples	30
3.	Conclusion Examples of logic gates was discussed	10

Assignment to be given: - Nil

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 4

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: A

S. No.	**Topic :-** Combinational logic blocks	**Time Allotted:-**
1.	Introduction Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.	05 min
2	Division of the Topic ▪ NAND-only Logic circuits ▪ Integrated circuits ▪ An SSI chip contains independent NAND gates	30
3.	Conclusion Introduction to integrated circuits	10

Assignment to be given: - what are integrated circuits?

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 5

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: A

S. No.	**Topic :-** Combinational logic blocks	**Time Allotted:-**
1.	Introduction Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.	05 min
2	Division of the Topic ▪ Examples of Combinational circuits ▪ Decoder ▪ 2:4 Decoder ▪ 3:8 Decoder ▪ Combinational Circuit Design with Decoders ▪ Multiplexers	30
3.	Conclusion Introduction to Combinational logic blocks	10

Assignment to be given: - Draw 3:8 decoder truth table.

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 6

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: A

S. No.	**Topic :-** Sequential logic blocks	**Time Allotted:-**
1.	Introduction Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.	05 min
2	Division of the Topic ▪ Overview ▪ Sequential Circuits ▪ Cross-coupled Inverters ▪ S-R Latch with NORs ▪ S-R Latch with NANDs ▪ D Latch ▪ Symbols for Latches	30
3.	Conclusion Introduction to Sequential logic blocks	10

Assignment to be given: - What are sequential circuits?

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 7

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: A

S. No.	**Topic :-** Sequential logic blocks	**Time Allotted:-**
1.	Introduction Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.	05 min
2	Division of the Topic ▪ Overview ▪ Register with Parallel Load ▪ Register with Load Control ▪ Shift Registers ▪ Parallel Data Transfer	30
3.	Conclusion Examples of Sequential logic blocks	10

Assignment to be given: - Explain shift registers by example

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 8

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: A

S. No.	**Topic :-** Stored Program Concept	**Time Allotted:-**
1.	Introduction Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.	05 min
2	Division of the Topic ▪ Stored program concept ▪ Design of the von Neumann architecture	30
3.	Conclusion Introduction to Stored Program Concept	10

Assignment to be given: - What is von Neumann architecture

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 9

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: A

S. No.	**Topic :-** Flynn's Classification	**Time Allotted:-**
1.	Introduction Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.	05 min
2	Division of the Topic ▪ Flynn's classification of computers ▪ SIMD Computer System ▪ MISD Computer System ▪ MIMD Computer System	30
3.	Conclusion Introduction to Flynn's classification of computers	10

Assignment to be given: - Differentiate SIMD and MISD.

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 10

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: A

S. No.	**Topic :-** Multilevel viewpoint	**Time Allotted:-**
1.	Introduction Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.	05 min
2	Division of the Topic ▪ Multilevel View Point of A Machine ▪ The Computer Level Hierarchy ▪ Hardwired Control ▪ Micro programmed Control ▪ Instruction Set Architecture (ISA) ▪ Actual Multilevel Computer	30
3.	Conclusion Introduction to Multilevel viewpoint	10

Assignment to be given: - What is ISA?

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 11

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: A

S. No.	**Topic :-** Multilevel viewpoint	**Time Allotted:-**
1.	Introduction Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.	05 min
2	Division of the Topic ▪ Operating System Machine ▪ What is an OS ▪ Goal of OS ▪ Instruction Set Representation ▪ Instruction Formats ▪ Registers ▪ CPU	30
3.	Conclusion Details of Multilevel viewpoint	10

Assignment to be given: - Nil

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 12

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: A

S. No.	**Topic :-** Performance Metrics	**Time Allotted:-**
1.	Introduction Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.	05 min
2	Division of the Topic ▪ What is a performance metric? ▪ Performance Measures ▪ MFLOPS	30
3.	Conclusion Details of Performance Metrics	10

Assignment to be given: - What are MFLOPS?

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 13

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: B

S. No.	**Topic :-** CISC	**Time Allotted:-**
1.	Introduction Instruction set based classification of processors (RISC, CISC, and their comparison); addressing modes: register, immediate, direct, indirect, indexed; Operations in the instruction set; Arithmetic and Logical, Data Transfer, Control Flow; Instruction set formats (fixed, variable, hybrid); Language of the machine: 8086 ; simulation using MSAM.	05 min
2	Division of the Topic ▪ Instruction Format ▪ Instruction Representation ▪ CISC ▪ CISC Attributes ▪ CISC Characteristics	30
3.	Conclusion Introduction to CISC architecture	10

Assignment to be given: - Nil

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 14

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: B

S. No.	**Topic :-** RISC	**Time Allotted:-**
1.	Introduction Instruction set based classification of processors (RISC, CISC, and their comparison); addressing modes: register, immediate, direct, indirect, indexed; Operations in the instruction set; Arithmetic and Logical, Data Transfer, Control Flow; Instruction set formats (fixed, variable, hybrid); Language of the machine: 8086 ; simulation using MSAM.	05 min
2	Division of the Topic ▪ What is RISC? ▪ OVERLAPPED REGISTER WINDOWS ▪ CISC versus RISC	30
3.	Conclusion Introduction to RISC architecture	10

Assignment to be given: - Compare CISC and RISC

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

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Lecture Plan 15

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: B

S. No.	**Topic :-** Addressing modes	**Time Allotted:-**
1.	Introduction Instruction set based classification of processors (RISC, CISC, and their comparison); addressing modes: register, immediate, direct, indirect, indexed; Operations in the instruction set; Arithmetic and Logical, Data Transfer, Control Flow; Instruction set formats (fixed, variable, hybrid); Language of the machine: 8086 ; simulation using MSAM.	05 min
2	Division of the Topic ▪ Central Processing Unit Addressing modes ▪ Numerical example ▪ Immediate Mode ▪ Indirect Mode ▪ Indexing Mode ▪ Relative Mode	30
3.	Conclusion Introduction to addressing modes	10

Assignment to be given: - Explain indirect addressing

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 16

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: B

S. No.	**Topic :-** Instruction Set Formats	**Time Allotted:-**
1.	Introduction Instruction set based classification of processors (RISC, CISC, and their comparison); addressing modes: register, immediate, direct, indirect, indexed; Operations in the instruction set; Arithmetic and Logical, Data Transfer, Control Flow; Instruction set formats (fixed, variable, hybrid); Language of the machine: 8086 ; simulation using MSAM.	05 min
2	Division of the Topic ▪ Central Processing Unit Instruction Formats ▪ Three address instruction ▪ Two address instruction ▪ One address instruction ▪ Zero address instruction	30
3.	Conclusion Introduction to Instruction Set Formats	10

Assignment to be given: - Nil

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 17

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: C

S. No.	**Topic :-** CPU Architecture Types	**Time Allotted:-**
1.	Introduction CPU Architecture types (accumulator, register, stack, memory/ register) detailed data path of a typical register based CPU, Fetch-Decode-Execute cycle (typically 3 to 5 stage); microinstruction sequencing, implementation of control unit, Enhancing performance with pipelining. The need for a memory hierarchy (Locality of reference principle, Memory hierarchy in practice: Cache, main memory and secondary memory, Memory parameters: access/ cycle time, cost per bit); Main memory (Semiconductor RAM & ROM organization, memory expansion, Static & dynamic memory types); Cache memory (Associative & direct mapped cache organizations.	05 min
2	Division of the Topic ▪ (Central Processing Unit) CPU Introduction ▪ CPU Organization Accumulator based CPU ▪ CPU Organization Register based CPU ▪ CPU ▪ CPU General Register Organization ▪ Stack organisation	30
3.	Conclusion Introduction to CPU Architecture Types was given	10

Assignment to be given: - Explain stack organisation

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 18

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: C

S. No.	**Topic :-** Fetch decode execute cycle	**Time Allotted:-**
1.	Introduction CPU Architecture types (accumulator, register, stack, memory/ register) detailed data path of a typical register based CPU, Fetch-Decode-Execute cycle (typically 3 to 5 stage); microinstruction sequencing, implementation of control unit, Enhancing performance with pipelining. The need for a memory hierarchy (Locality of reference principle, Memory hierarchy in practice: Cache, main memory and secondary memory, Memory parameters: access/ cycle time, cost per bit); Main memory (Semiconductor RAM & ROM organization, memory expansion, Static & dynamic memory types); Cache memory (Associative & direct mapped cache organizations.	05 min
2	Division of the Topic ▪ Instruction cycle ▪ Fetch and decode ▪ Register reference instructions ▪ Memory reference instructions ▪ Flowchart for memory reference instructions ▪ Input-output and interrupt	30
3.	Conclusion Introduction to Fetch decode execute cycle was given	10

Assignment to be given: - Nil

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 19

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: C

S. No.	**Topic :-** Fetch decode execute cycle	**Time Allotted:-**
1.	Introduction CPU Architecture types (accumulator, register, stack, memory/ register) detailed data path of a typical register based CPU, Fetch-Decode-Execute cycle (typically 3 to 5 stage); microinstruction sequencing, implementation of control unit, Enhancing performance with pipelining. The need for a memory hierarchy (Locality of reference principle, Memory hierarchy in practice: Cache, main memory and secondary memory, Memory parameters: access/ cycle time, cost per bit); Main memory (Semiconductor RAM & ROM organization, memory expansion, Static & dynamic memory types); Cache memory (Associative & direct mapped cache organizations.	05 min
2	Division of the Topic ▪ Program controlled data transfer ▪ Input-output instructions ▪ Program-controlled input/output ▪ Interrupt initiated input/output ▪ Flowchart for interrupt cycle ▪ Register transfer operations in interrupt cycle	30
3.	Conclusion Introduction to Fetch decode execute cycle was given	10

Assignment to be given: - Nil

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 20

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: C

S. No.	**Topic :-** Memory hierarchy	**Time Allotted:-**
1.	Introduction CPU Architecture types (accumulator, register, stack, memory/ register) detailed data path of a typical register based CPU, Fetch-Decode-Execute cycle (typically 3 to 5 stage); microinstruction sequencing, implementation of control unit, Enhancing performance with pipelining. The need for a memory hierarchy (Locality of reference principle, Memory hierarchy in practice: Cache, main memory and secondary memory, Memory parameters: access/ cycle time, cost per bit); Main memory (Semiconductor RAM & ROM organization, memory expansion, Static & dynamic memory types); Cache memory (Associative & direct mapped cache organizations.	05 min
2	Division of the Topic ▪ Memory organization ▪ Memory hierarchy ▪ Main memory ▪ Memory address map ▪ Connection of memory to cpu ▪ Auxiliary memory ▪ Associative memory	30
3.	Conclusion Introduction to Memory hierarchy was given	10

Assignment to be given: - Nil

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 21

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: D

S. No.	**Topic :-** Parallelism	**Time Allotted:-**
1.	Introduction Goals of parallelism (Exploitation of concurrency, throughput enhancement); Amdahl's law; Instruction level parallelism (pipelining, super scaling –basic features); Processor level parallelism (Multiprocessor systems overview). Instruction codes, computer register, computer instructions, timing and control, instruction cycle, type of instructions, memory reference, register reference. I/O reference, Basics of Logic Design, accumulator logic, Control memory, address sequencing, micro-instruction formats, micro-program sequencer, Stack Organization, Instruction Formats, Types of interrupts; Memory Hierarchy.	05 min
2	Division of the Topic ▪ Goals of Parallelism ▪ Exploitation of Concurrency ▪ Types of Parallelism ▪ Instruction Pipeline ▪ Four segment CPU Pipeline ▪ Timing of Instruction Pipeline ▪ Pipeline Conflicts ▪ Instruction-level parallelism (ILP) ▪ Processor Level Parallelism	30 10
3.	Conclusion Introduction to parallelism was given	

Assignment to be given: - What are the Goals of Parallelism

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 22

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: D

S. No.	**Topic :-** Amdahl's Law	**Time Allotted:-**
1.	Introduction Goals of parallelism (Exploitation of concurrency, throughput enhancement); Amdahl's law; Instruction level parallelism (pipelining, super scaling –basic features); Processor level parallelism (Multiprocessor systems overview). Instruction codes, computer register, computer instructions, timing and control, instruction cycle, type of instructions, memory reference, register reference. I/O reference, Basics of Logic Design, accumulator logic, Control memory, address sequencing, micro-instruction formats, micro-program sequencer, Stack Organization, Instruction Formats, Types of interrupts; Memory Hierarchy.	05 min
2	Division of the Topic ▪ Amdahl's law ▪ Basic Page Replacement ▪ Modes of transfer ▪ Programmed I/O ▪ Interrupt Initiated IO ▪ Types of Interrupt ▪ DMA (Direct Memory Access)	30
3.	Conclusion Introduction to Amdahl's Law was given	10

Assignment to be given: - Nil

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 23

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: D

S. No.	**Topic :-** Control Unit	**Time Allotted:-**
1.	Introduction Goals of parallelism (Exploitation of concurrency, throughput enhancement); Amdahl's law; Instruction level parallelism (pipelining, super scaling –basic features); Processor level parallelism (Multiprocessor systems overview). Instruction codes, computer register, computer instructions, timing and control, instruction cycle, type of instructions, memory reference, register reference. I/O reference, Basics of Logic Design, accumulator logic, Control memory, address sequencing, micro-instruction formats, micro-program sequencer, Stack Organization, Instruction Formats, Types of interrupts; Memory Hierarchy.	05 min
2	Division of the Topic ▪ Control unit ▪ Timing and control ▪ Timing signals ▪ Pipelining and vector processing ▪ Parallel processing ▪ Pipeline and multiple function units ▪ Instruction cycle	30
3.	Conclusion Introduction to control unit was given	10

Assignment to be given: - Nil

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 24

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: D

S. No.	**Topic :-** Memory reference	**Time Allotted:-**
1.	Introduction Goals of parallelism (Exploitation of concurrency, throughput enhancement); Amdahl's law; Instruction level parallelism (pipelining, super scaling –basic features); Processor level parallelism (Multiprocessor systems overview). Instruction codes, computer register, computer instructions, timing and control, instruction cycle, type of instructions, memory reference, register reference. I/O reference, Basics of Logic Design, accumulator logic, Control memory, address sequencing, micro-instruction formats, micro-program sequencer, Stack Organization, Instruction Formats, Types of interrupts; Memory Hierarchy.	05 min
2	Division of the Topic ▪ Common bus system ▪ Computer instructions ▪ Memory reference instruction ▪ Register reference instruction ▪ Input-output instruction	30
3.	Conclusion Introduction to memory reference was given	10

Assignment to be given: - What is Memory reference instruction?

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 25

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: D

S. No.	**Topic :-** Microinstruction sequencing	**Time Allotted:-**
1.	Introduction Goals of parallelism (Exploitation of concurrency, throughput enhancement); Amdahl's law; Instruction level parallelism (pipelining, super scaling –basic features); Processor level parallelism (Multiprocessor systems overview). Instruction codes, computer register, computer instructions, timing and control, instruction cycle, type of instructions, memory reference, register reference. I/O reference, Basics of Logic Design, accumulator logic, Control memory, address sequencing, micro-instruction formats, micro-program sequencer, Stack Organization, Instruction Formats, Types of interrupts; Memory Hierarchy.	05 min
2	Division of the Topic ▪ Microprogrammed control ▪ Comparison of control unit implementations ▪ Microinstruction sequencing ▪ Conditional branch ▪ Mapping of instructions ▪ Microprogram example	30 10
3.	Conclusion Introduction to Microinstruction sequencing was given	

Assignment to be given: - Nil

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 26

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: D

S. No.	**Topic :-** Microinstruction sequencing	**Time Allotted:-**
1.	Introduction Goals of parallelism (Exploitation of concurrency, throughput enhancement); Amdahl's law; Instruction level parallelism (pipelining, super scaling –basic features); Processor level parallelism (Multiprocessor systems overview). Instruction codes, computer register, computer instructions, timing and control, instruction cycle, type of instructions, memory reference, register reference. I/O reference, Basics of Logic Design, accumulator logic, Control memory, address sequencing, micro-instruction formats, micro-program sequencer, Stack Organization, Instruction Formats, Types of interrupts; Memory Hierarchy.	05 min
2	Division of the Topic ▪ Machine instruction format ▪ Microinstruction field descriptions ▪ Symbolic microinstructions ▪ Symbolic microprogram ▪ Design of control unit ▪ Microprogram sequencer ▪ Nanostorage and nanoinstruction	30
3.	Conclusion Introduction to Microinstruction sequencing was given	10

Assignment to be given: - Nil

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

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Lecture Plan 27

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: D

S. No.	**Topic :-** 8086	**Time Allotted:-**
1.	Introduction Goals of parallelism (Exploitation of concurrency, throughput enhancement); Amdahl's law; Instruction level parallelism (pipelining, super scaling –basic features); Processor level parallelism (Multiprocessor systems overview). Instruction codes, computer register, computer instructions, timing and control, instruction cycle, type of instructions, memory reference, register reference. I/O reference, Basics of Logic Design, accumulator logic, Control memory, address sequencing, micro-instruction formats, micro-program sequencer, Stack Organization, Instruction Formats, Types of interrupts; Memory Hierarchy.	05 min
2	Division of the Topic ▪ Features of 8086 Microprocessor ▪ 8086 microprocessor ▪ 20 bits address bus? ▪ 8086 INTERNAL ARCHITECTURE ▪ BIU and EU ▪ Pin diagram	30
3.	Conclusion Introduction to 8086 microprocessor was given	10

Assignment to be given: - What is BIU?

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Lecture Plan 28

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: D

S. No.	**Topic :-** 8086 registers	**Time Allotted:-**
1.	Introduction Goals of parallelism (Exploitation of concurrency, throughput enhancement); Amdahl's law; Instruction level parallelism (pipelining, super scaling –basic features); Processor level parallelism (Multiprocessor systems overview). Instruction codes, computer register, computer instructions, timing and control, instruction cycle, type of instructions, memory reference, register reference. I/O reference, Basics of Logic Design, accumulator logic, Control memory, address sequencing, micro-instruction formats, micro-program sequencer, Stack Organization, Instruction Formats, Types of interrupts; Memory Hierarchy.	05 min
2	Division of the Topic ▪ Registers ▪ Code segment ▪ Stack segment ▪ Data segment ▪ Extra segment ▪ Accumulator ▪ Base Register ▪ Count Register ▪ Data Register ▪ Index registers ▪ Flags	30 10
3.	Conclusion Introduction to 8086 registers was given	

Assignment to be given: - What is the function of code segment?

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

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Lecture Plan 29

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: D

S. No.	**Topic :-** 8086 instructions	**Time Allotted:-**
1.	Introduction Goals of parallelism (Exploitation of concurrency, throughput enhancement); Amdahl's law; Instruction level parallelism (pipelining, super scaling –basic features); Processor level parallelism (Multiprocessor systems overview). Instruction codes, computer register, computer instructions, timing and control, instruction cycle, type of instructions, memory reference, register reference. I/O reference, Basics of Logic Design, accumulator logic, Control memory, address sequencing, micro-instruction formats, micro-program sequencer, Stack Organization, Instruction Formats, Types of interrupts; Memory Hierarchy.	05 min
2	Division of the Topic ▪ 8086 instruction set ▪ Addressing modes ▪ Data Transfer Instructions ▪ Logical Instructions ▪ Shift and Rotate Instructions ▪ Arithmetic Instructions ▪ Transfer Instructions ▪ Loop Control ▪ String Instructions ▪ Repeat instructions ▪ Processor Control Instructions	30 10
3.	Conclusion Introduction to 8086 instructions was given	

Assignment to be given: - Nil

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes

Doc. No.: DCE/0/15
Revision: 00

Lecture Plan 30

Faculty: Parul Bansal Semester: IV Class: ECS Course Code: CSE-210-F

Subject: Computer Architecture and Organization Section: D

S. No.	**Topic :-** 8086 timing & control	**Time Allotted:-**
1.	Introduction Goals of parallelism (Exploitation of concurrency, throughput enhancement); Amdahl's law; Instruction level parallelism (pipelining, super scaling –basic features); Processor level parallelism (Multiprocessor systems overview). Instruction codes, computer register, computer instructions, timing and control, instruction cycle, type of instructions, memory reference, register reference. I/O reference, Basics of Logic Design, accumulator logic, Control memory, address sequencing, micro-instruction formats, micro-program sequencer, Stack Organization, Instruction Formats, Types of interrupts; Memory Hierarchy.	05 min
2	Division of the Topic ▪ Microprocessors-8086 ▪ Microcomputer ▪ 8086 buses ▪ Machine cycle ▪ Timing sequence ▪ Read cycle ▪ Write cycle	30 10
3.	Conclusion Introduction to 8086 timing & control was given	

Assignment to be given: - Draw read & write cycles.

Reference Readings:-

- Computer system architecture by Morris Mano.
- Computer architecture and organization by John P Hayes